

## PROGRAMMABLE LOGIC APPLICATION NOTES

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter will continue a series of notes concentrating on analysis techniques with this issue's section discussing Digital Timing Analysis Tools and Techniques. If you have information that you would like to submit or an area you would like discussed or researched, please give me a call or an e-mail.

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### MAPLD International Conference

Kossiakoff Conference Center  
JHU/Applied Physics Laboratory  
Laurel, Maryland

The 3<sup>rd</sup> annual Military and Aerospace Applications of Programmable Devices and Technologies Conference was held September 26-28, 2000 and featured oral and poster presentations, tours of NASA, NSA, and APL, an Industrial Exhibit, and invited talks. Conference Proceedings will be published in January, 2001 with select papers published in the *AIAA Journal of Spacecraft and Rockets*.

The 4<sup>th</sup> annual Military and Aerospace Applications of Programmable Devices and Technologies International Conference will be held September 11-13, 2001. This year's Conference will emphasize logic, processor, and DSP design. For central processor units, papers on FPGA, ASIC, and custom microcircuits will be accepted. <http://rk.gsfc.nasa.gov/richcontent/MAPLDCon01/MAPLDCon01.html>

The first call for papers has been released and is available at: [http://rk.gsfc.nasa.gov/richcontent/MAPLDCon01/MAPLDCon01\\_1CallForPapers.html](http://rk.gsfc.nasa.gov/richcontent/MAPLDCon01/MAPLDCon01_1CallForPapers.html).

There are several new features being planned for the 2001 MAPLD International Conference. One of these is tutorial courses. Please see [http://rk.gsfc.nasa.gov/richcontent/MAPLDCon01/MAPLDCon01\\_1CallForPapers.html](http://rk.gsfc.nasa.gov/richcontent/MAPLDCon01/MAPLDCon01_1CallForPapers.html) for more information and suggestions, please send e-mail to [mapld2001@knet-linux.gsfc.nasa.gov](mailto:mapld2001@knet-linux.gsfc.nasa.gov).

## What's New?

A large amount of data, reports, papers, application notes, and conference information are being stored on our companion Programmables Technology www site, <http://rk.gsfc.nasa.gov>. In order to make it easier to keep readers up to date, all new additions to the site are being listed, in chronological order on our "What's New" page. This has recently been reorganized for faster loading: [http://rk.gsfc.nasa.gov/What's\\_New.htm](http://rk.gsfc.nasa.gov/What's_New.htm)

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### SX and SX-A Series Devices Power Sequencing

The RT54SX16 and the RT54SX32 are 0.6  $\mu\text{m}$  devices fabricated at MEC. Note that these devices differ from the A54SX series, which are 0.35  $\mu\text{m}$  devices fabricated at CSM. The A54SX-A series devices are either 0.25 or 0.22  $\mu\text{m}$  devices built at MEC and UMC, respectively. Current prototypes of the RT54SX-A series are built at MEC. Current prototypes of the SEU-hardened RT54SX32S device are derivatives of the MEC 0.25 $\mu\text{m}$  SX-A series microcircuits.

For SX-series devices, there has been a change to the data sheet and there are now requirements on how the power supplies must be sequenced, both for the power-on and power-off states. When powering up,  $V_{\text{CCR}}$  must come up first and then  $V_{\text{CCI}}$  and  $V_{\text{CCA}}$ . When powering the device down,  $V_{\text{CCI}}$  and  $V_{\text{CCA}}$  must power down before  $V_{\text{CCR}}$ .

For the SX-A series devices (0.25  $\mu\text{m}$  and 0.22  $\mu\text{m}$ ) and the SEU-hardened SX-S, there are no requirements or limitations on power sequencing.

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### JTAG and SX/SX-A/SX-S Series Devices

This note will provide an update to the white paper on JTAG and SX devices that was written in 1998. The discussion will be kept as general as possible, as other FPGAs, such as the XQR4000XL and the Virtex devices incorporate a JTAG interface. Please see the following url for the original paper:

[http://rk.gsfc.nasa.gov/richcontent/fpga\\_content/SX\\_Series/JTAG\\_SX\\_WhitePaper.PDF](http://rk.gsfc.nasa.gov/richcontent/fpga_content/SX_Series/JTAG_SX_WhitePaper.PDF)

### TRST\* Pin

Some models of the RT54SX series devices do not have the optional IEEE 1149.1 JTAG TRST\* pin. These are the so-called "Revision 0" devices. A check of the most recent data sheet does not show a

way to tell whether the TRST\* pin is in a particular device. Please check with the manufacturer to verify that your lot has this pin, if that is in your procurement specification. The lot number is marked on the back of the package and is different from the date code, marked on the lid. From current information, none of the commercial/industrial models of the A54SX incorporate the TRST\* pin.

For SX-series devices without the TRST\* pin, A54SX and RT54SX "Revision 0," one can not be guaranteed that the TAP controller will not be upset and the device may lose control. This has been demonstrated in ground-based heavy ion tests, where power cycling of the part was required to restore functionality, even with TMS held high and TCK running. Currents exceeding 800 mA have been observed.

Additionally, from current information, all models of the A54SX-A, RT54SX-A, and RT54SX-S do have the TRST\* pin. When biased at ground, the TRST\* pin will hold the JTAG TAP controller in the TEST-LOGIC-RESET state. Note that the IEEE requires that, left unconnected, the TRST\* pin pulls high, which is exactly the **WRONG WAY** from a fail-safe point of view. Verification for each microcircuit should include a check to ensure a good, solid pull-down to ground. A piece of wire or a routing trace is appropriate.

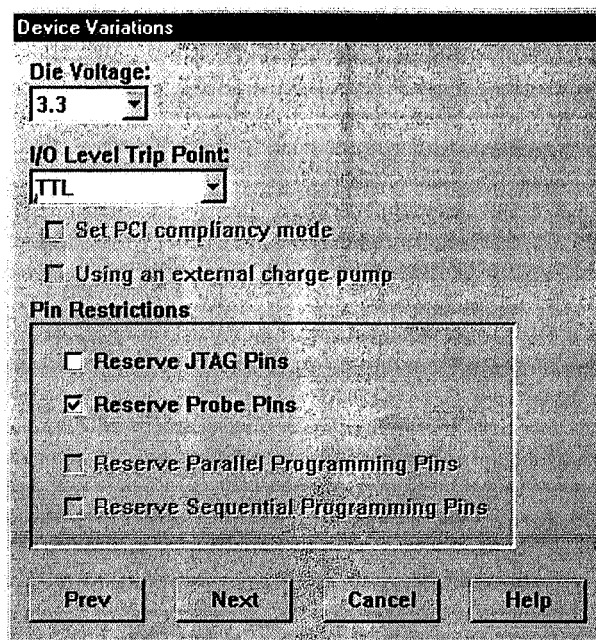
There is no known, simple way to verify that the TRST\* pin is active, as this pin can be used as an I/O in current versions of the devices. Simple, reliable verification processes are under investigation.

*TCLK Pin*

The IEEE 1149.1 specification is logically designed so that if TMS is held high, the TAP controller will be in the TEST-LOGIC-RESET state in no more than 5 cycles of the TCK. Verify that the driver into the TCLK pin is isolated and not connected to the system clock. If the two clocks are electrically the same signal, then if a "JTAG upset" occurs, the system clock pin can turn into an active output, shutting down the system clock. The part then can not recover into the TEST-LOGIC-RESET state.

*Design Database Configuration and Verification*

It is critical that the JTAG configuration be specified correctly in your design database. When a netlist is imported and the device set up, ensure that the **Reserve JTAG Pins** option is set. This is not the default with the current software and the special JTAG pins will be configured as normal I/Os. This



*R3-1998 Designer Screen Shot  
Note the default state is off for  
the JTAG Pins.*

includes the TRST\* pin! The JTAG TAP controller may lose control and circuit board level inputs can be ignored if this is not configured correctly. See the screen image from R3-1998 showing how the software defaults into this potentially dangerous condition.

You can verify that the part is specified correctly by doing a Reports => Status command and look at the layout variables:

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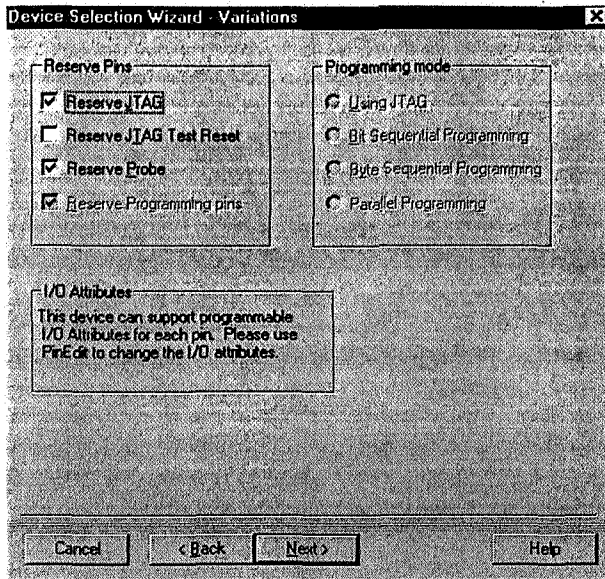
**** Layout Variables ****
Mode: STANDARD Incremental: OFF
Restrict JTAG Pins: YES Restrict Probe
Pins: YES
    
```

If the part is not configured correctly, then you can go back through the Options => Device Setup Wizard and get back to the Device Variations form above.

*R1-2000 SP1 Software*

The defaults have been changed with the R1-2000 SP1 software. For the RT54SX32-S and for RT54SX devices, for example, the **Reserve JTAG Pins** option is set by default. For the RT54SX-S only, it is noted that the reservation for the RESET pins is not set by default.<sup>1</sup> For commercial devices,

<sup>1</sup> This will make TRST\* unavailable unless checked.



*R1-2000 SPI Designer Screen Shot for RT54SX32-S*

*Note that the default state of the Reserve JTAG field is ON for this device; the default is OFF for the commercial devices. Both should be checked.*

the **Reserve JTAG Pins** option is not set by default. Each and every device must be checked carefully with every version of software!!

### Analysis Techniques

The following application note on Digital Timing Analysis Tools and Techniques was contributed by Dr. R. L. Barto of Spacecraft Digital Electronics. In 1991, Dr. Barto received the NASA Public Service Medal for the Galileo AACS design. This note is the first in a series on analysis techniques.

#### *Digital Timing Analysis Tools and Techniques*

##### *Abstract*

The timing analysis is a crucial part of a digital system's worst case analysis. Every latched device has timing requirements -- set-up times, hold times, etc. -- that must be met in order to guarantee correct system operation, and the goal of the timing analysis is to determine whether they are met. Because each device input can have many sources whose timing can vary with circuit operation mode, the timing analysis can be very complicated and time consuming. Thus, many attempts at automating the timing analysis task have been made. Nevertheless, the task is sufficiently complex that attempts to fully

automate it so far have had only limited success. This report examines several timing analysis methods, and discusses their strengths and weaknesses.

#### *What are the Requirements for Timing Analysis Tools?*

The goal of circuit analysis is proving correct circuit design. Therefore, the primary requirement for an analysis tool is that it be accurate in proving or disproving correctness. This means not only that the necessary calculations are performed correctly, but also that it be able to analyze a variety of design techniques. Other desirable features include timeliness and flexibility: the tool would be useless its result was available only after the design was fabricated, or if it was difficult to update the analysis to incorporate design changes.

#### *Logic Simulation as a Timing Analysis Tool*

Logic simulators model digital circuit operation in software, and those capable of modeling gate delays are often used to analyze timing. They are not guaranteed to produce a correct analysis because the time required to perform the simulation limits the number of input vectors and circuit operating modes, and the length of circuit operation that can be simulated. This results in portions of the circuitry being not exercised in the simulation. If the unexercised circuitry contains components having timing requirements that must be analyzed, the analysis will not be complete.

Other limitations of logic simulators arise from the difficulty of modeling effects such as capacitive loading, transmission lines, or the propagation delays of parts interfacing to out-of-family parts having different logic thresholds. These considerations make logic simulators a poor choice for timing analyses.

#### *Static Timing Verifiers*

Static timing verifiers are useful as timing analysis tools only. A verifier does not simulate the activity of the circuit, but rather constructs a directed graph from the circuit, assigns delay values to the nodes, then calculates the delay time between every pair of nodes that receive a clock, thus calculating the set-up and hold times of every clocked device in the circuit. Static verifiers are very fast relative to logic simulators, performing an analysis in minutes or hours.

Because there is no circuit simulation, the verifier has no knowledge of circuit operation and

hence calculates delay values for each circuit path whether or not the path will actually be exercised in circuit operation, causing the *false path problem*. The number of false paths, i.e., those that can never occur, may be very large, but the timing results for them will be reported, along with the results for true paths, unless they are suppressed. Suppressing false paths raises the possibility that some true paths may also be suppressed, thus decreasing the coverage of the analysis. Not suppressing false paths increases the amount of data the analyst must review, because every path reported as generating a timing violation must be individually verified to be either a true or a false path.

Timing verifiers are subject to the same modeling limitations as logic simulators. A particular verifier may not be able to handle all circuit design techniques, for example, be unable to calculate pulse widths for clocks, clears, etc., or handle designs that are not totally synchronous. Verifiers are an improvement over logic simulators from the performance and coverage standpoints, but are not a complete analysis solution in the general case.

#### *Hand Analysis and Other Computer Methods*

Hand analysis is the most complete and most time consuming of all the analysis methods. There is no circuit design technique, or unusual use of parts, that cannot be analyzed by hand. A hand-done analysis however, will be difficult to update for changing designs or parts parameters. Any change may ripple through the analysis causing considerable recalculation. Hand calculations can also be error prone. These limitations can be somewhat overcome by using appropriate software as an adjunct to the analysis process.

**Spread Sheets:** Spread sheets can be used to break the analysis into sections, storing intermediate results and parts parameters, and performing the calculations for the analyst. Accuracy and flexibility are thus increased.

**Custom Programs:** A program, TIMEANAL, written in 1988 has been useful on several projects. TIMEANAL is an interpreter which takes as input a text file describing the calculations to be performed, a file relating unit numbers to part types, and a parts parameter file. It can handle any design technique and can calculate the effects of differing logic thresholds, pull-up resistors, and capacitive loading. The output is a text file describing the calculations performed and noting whether the requirements

were met. Run time is only a few minutes for even a complex file, and updating for parts parameter changes is very easy. Updating for design changes requires editing the input file.

Performing a hand timing analysis with a computer aid allows the analyst to spend more time doing what people do better than computers, i.e., think, and has the computer do what it does better than people, i.e., table look-up and calculations.

#### *Use of Vendor Supplied Analysis Tools*

Parts vendors often supply timing analysis tools as part of a design package. Always use such tools and nothing else. It would be a rare engineer who could create a better analyzer than that supplied by a vendor who has written the tool specifically for his parts. And, even if a better analyzer could be devised, use of the vendor's analyzer should carry with it the guarantee that the parts will function properly if they pass the vendor's analysis. If another tool is used and no errors are found in the design, but the parts fail to function correctly, the analyst has no recourse with the vendor.

#### *Using Design Rules as a Prelude to the Analysis*

In the above discussion, the analysis tool is treated as something to be used after the design is completed. Since the designer's goal should be to have the system work when first powered on, it is best to do the analysis concurrently with the design. The final timing analysis would thereby be a formality and would not have the potential to cause redesign. Setting design rules at the start of the design essentially "pre-does" the analysis and makes the design easier. For example, limiting oneself to a fully synchronous design and noting how many gate delay levels are allowable between clock edges allows one to show set-up times are met by simply counting the gates in the delay chains. Avoiding difficult-to-analyze design techniques such as gated clocks and clears and unusual uses of parts makes the design more analyzable and increases the probability of design success.

In the event that one is required to use a particular analysis tool, learn what design techniques it can and cannot analyze and design with the use of the tool in mind. Designing outside the capabilities of the tool can lead to a false sense of security that the design has no timing errors when none are reported, or increase the amount of hand analysis that must be done in order to have a complete analysis.

*Conclusion*

Every digital circuit should be subjected to a timing analysis. Designing with the analysis task in mind and performing the analysis as the design progresses is the key to achieving every designer's goal: a system that functions correctly when first powered on and flawlessly completes its mission.

**Status of the  
Radiation Hard reconfigurable Field  
Programmable Gate Array Program**

*Overview*

The objective of the "RH rFPGA" program is the development of a radiation-hardened version of the Atmel AT6010, an SRAM-based FPGA. This program is a partnering effort between the NASA Goddard Space Flight Center, Sandia National Laboratories, Honeywell, Inc., and Atmel Corporation. The Honeywell-Atmel agreement was announced in July 1998 and the proposed development was the subject of "Radiation Hard Reconfigurable Field Programmable Array," MAPLD 1998.

The planned device, to be fabricated on a CMOS/SOI process, will have a 3.3V core. 5V-tolerant I/Os have been added, resulting in a superset of the commercial specification. Goals for the program include a total dose hardness of 200 krad(Si), no SEL, and a SEU LET<sub>TH</sub> > 30 MeV-cm<sup>2</sup>/mg for both user storage and configuration elements.

*Current Status*

The program has completed the first of four phases. Phase 1 consisted of license agreements, technical data transfer, cost/schedule/resource baselines, risk assessment planning, and a Phase 1 Results review. Phase 2 has recently been funded, with the following planned activities: core, configuration clock, and I/O design & layout, pre-layout simulation, and a preliminary design review (PDR). The PDR is scheduled before the end of calendar year 2000.

*Acknowledgement: Material contributed by Jack McCabe, NASA Goddard Space Flight Center*

**Input Transition Times***Introduction*

Inputs to most CMOS inputs have rise and fall time limitations for reliable operation. Although most if not all programmable logic devices have at least some hysteresis on their inputs, the transition time requirements vary considerably. Below is a table with input transition time requirements for many military and aerospace programmable logic devices.

The following are the symbols typically used for these parameters:

$t_R$  - rise time  
 $t_F$  - fall time  
 $t_T$  - transition time

Most specifications do not specify exactly how the waveform is measured. Generally, according to most data books, the time period recorded is between the 10% and 90% of the waveforms. Note that often a data sheet will specify that the parameter is listed as information only and are not tested. In laboratory measurements, especially for devices that are migrated to a faster process, it was shown that not all qualified devices fall within specification limits. Appropriate care should be taken with conservative margins.

If the input transition time requirement is not satisfied, generally two different effects can be seen. The first, more often seen in older technologies, is the ability to propagate non-logic levels. In the modern, faster technologies, the input stage will appear to oscillate. Based on the input stage design, the oscillation may not be directly observable on the input pin - making a simple scope measurement inadequate for design verification.

*Implications*

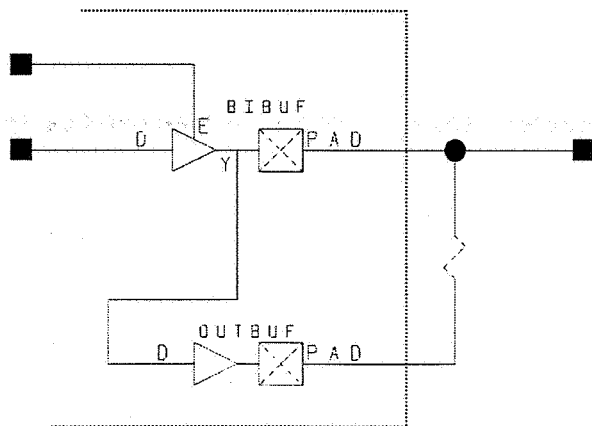
Normally, input transition time does not impact the design. However, there are several situations where appropriate care must be taken. Some of these are described below.

**Pull-up Resistors:** These are often used for tri-state or bi-directional busses. However, recall that the rise time of a pulled-up signal is  $\tau = 2.2RC$ , when measured between the 10% and 90% points on a waveform. For some of the devices, that is clearly significant. For example, suppose a bus signal has a capacitance of 50 pF and a pull-up resistor of 10 k $\Omega$  is used, to keep power dissipation reasonable. This RC product

results in a rise time of 500 ns. As seen in the chart below, this will violate the specifications of all of the recently introduced devices, with one device having a 10 ns requirement. One solution to this problem is simply not to use pull-up resistors and to utilize a bus hold or "keeper" circuit. This is easily constructed by connecting a resistor between the input and output of a buffer and connecting the buffer's input to the bus signal and ensuring proper voltage margins are maintained with the worst-case DC current draw. Often, this connection can be made using a spare FPGA I/O and a single device pin. Another alternative, used by the PCI protocol, is to actively drive the signal high before tri-stating the buffer. There is some level of risk for this circuit with various faults such as unexpected resets causing a driver, holding a line low, to tri-state.

**Filters:** Filters are often included on signals for a variety of reasons such as the elimination of noise, ESD protection, etc. The transition times of these signals must be examined. Often, a discrete hysteresis buffer should be employed to present a clean sharp edge to the FPGA input, particularly for clock signals.

**Interfacing with older logic families:** This can lead to problems. Examining typical data for the CD4000B CMOS NOR gate, for  $V_{DD} = 5V$ , the typical output transition time is 100 ns. For the CD4050B buffer, still in use to level-shift high voltage inputs, the room temperature,  $V_{DD} = 5V$  supply voltage condition yields a worst-case transition time of 160 ns! Use of a hysteresis buffer such as the 54AC14 would be recommended for certain applications.



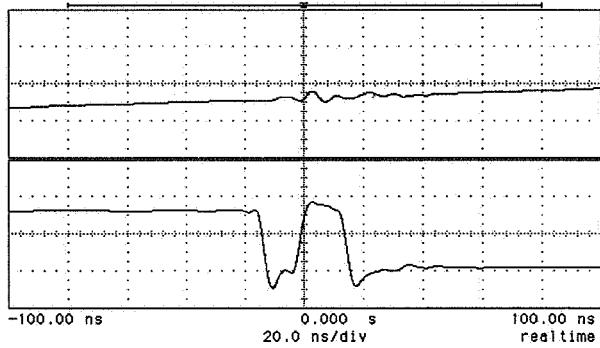
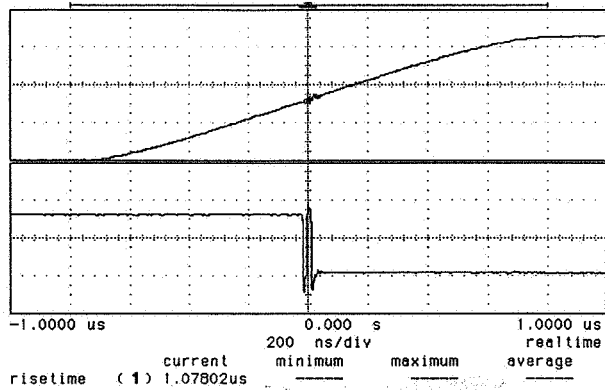
One Bus Hold Circuit

Manufacturer's Data

Input Transition Time Requirements for Military and Aerospace FPGAs and PALs

Part Number	Reference	$t_T$ max (ns)
A1020	1	500
A1020A	2	500
A1020B	3	500
RH1020	4	500
A1280	2	500
A1280A	4	500
RH1280	4	500
Act 3 - 0.8 $\mu$ m (5V)	-	500?
Act 3 - 0.8 $\mu$ m (3.3)	6	500
RT54SX16, 32	7	50
A54SX-A (32, 72)	8	10
RT54SXS	9	10
XQR4000XL	10	250
Virtex	11	250
UT22VP10	12	?
AT6010 (MIL)	13	50
AT6010 (3.3V)	14	50
Quicklogic	-	?

- [1] ACT™ 1 Field Programmable Gate Arrays, March 1991.
- [2] ACT 1 and ACT 2 Military FPGAs, April, 1992.
- [3] ACT™ 1 Series FPGAs, April 1996.
- [4] Radiation-Hardened FPGAs, v3.0, January 2000.
- [5] ACT™ 2 Series FPGAs, April 1996.
- [6] Accelerator Series FPGAs – ACT™ 3 Family, September, 1997.
- [7] 54SX Family FPGAs RadTolerant and HiRel, Preliminary V1.5, March 2000.
- [8] HiRel SX-A Family FPGAs, Advanced v.1, April 2000.
- [9] RT54SX-S RadTolerant FPGAs for Space Applications, Advanced 0.2, November, 2000.
- [10] QPRO XQR4000XL Radiation Hardened FPGAs, DS071 (v1.1) June 25, 2000.
- [11] QPRO™ Virtex™ 2.5V Radiation Hardened FPGAs, DS028 (v1.0) April 25, 2000 Advance Product Specification.
- [12] Not in data sheet.
- [13] Configurable Logic Data Book, Atmel, August 1995.
- [14] AT6000LV, Atmel, October 1999.



RT54SX16 output (bottom trace) with a slow rising input (top trace) which clocks a divide by two counter resulting in a "glitch." The clock input was provided by an HP8110A pulse generator.

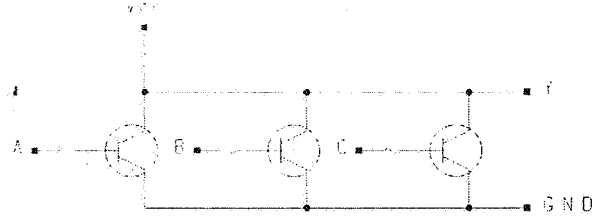
### Apollo Guidance Computer Logic Study

A study is underway to research the quality and long term reliability of logic<sup>2</sup> used for the Apollo Guidance Computer (AGC), which was designed by MIT's Instrumentation Laboratory. There were two versions of this computer built. Block I and Block II.<sup>3</sup> Block I units used, as a logic element, a single 3-input NOR function, with  $V_{CC} = 3V$ , packaged in a TO-47 can. Block II microcircuits, packaged in flat packs as shown in the image below, were dual 3-input NOR functions, with  $V_{CC} = 4V$ . Both types of circuits, which use direct coupled transistor logic (DCTL), had a fanout of six.

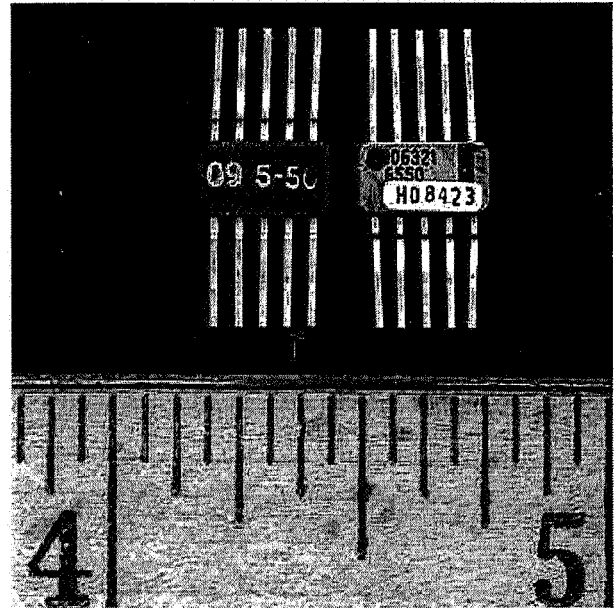
<sup>2</sup> Special thanks is given to Eldon C. Hall for supplying samples of the microcircuits, technical information, and support and encouragement for this project.

<sup>3</sup> For a technical history of the AGC, see **Journey to the Moon: The History of the Apollo Guidance Computer**, Eldon C. Hall, 1996.

It is planned to report progress of this study here and then formally publish the results.



Equivalent circuit for a Micrologic gate.



Two Apollo Block 2 microcircuits. Each microcircuit was a dual, 4-input NOR function.

### RT54SX32S Prototype Data Sets

#### Introduction

This device is a derivative of the A54SX32A and, as such, has a 2.5 V core. The current prototypes are processed in 0.25  $\mu m$  technology at MEC. One of the important features of this part is use of the K-Latch<sup>4</sup>; an asynchronous TMR-based logic circuit used to implement SEU-hardened latches for the construction of the R-Cell.

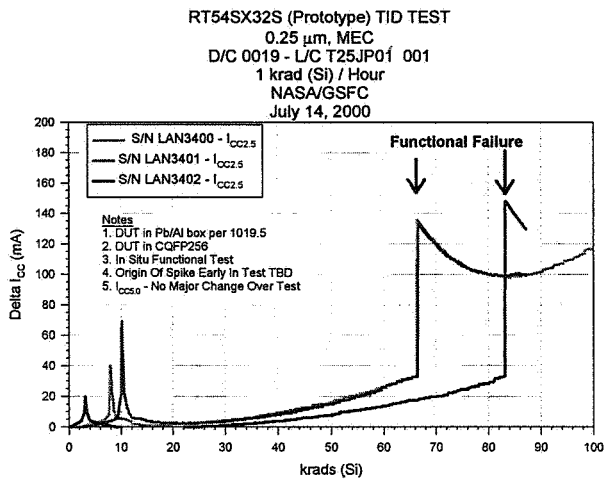
This note presents some background information as well as some of the recent test data. A complete set of the latest SEE data is on-line at

<sup>4</sup> The topology and logical design of the circuit was performed by K-Labs in 1998. The transistor level circuit design was performed by Actel Corporation.

[http://rk.gsfc.nasa.gov/richcontent/fpga\\_content/SXA\\_Series/BNL1000/SX-AS MEC/Test BNL1000 SX-AS MEC.htm](http://rk.gsfc.nasa.gov/richcontent/fpga_content/SXA_Series/BNL1000/SX-AS MEC/Test BNL1000 SX-AS MEC.htm)

*Total Dose*

Three prototype devices were irradiated at NASA Goddard Space Flight Center. Data was sampled every 5 minutes and *in situ* functional tests ran at the rate of once per hour and failure corresponded with the sharp increase in current. The bulk process used in this device utilizes shallow trench isolation. The results of the total ionizing dose test are shown below.



*Single Event Latchup*

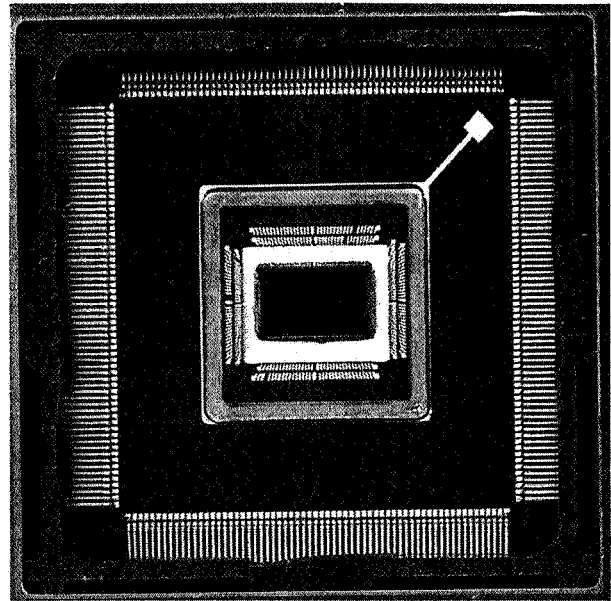
345 MeV I-127 ions were used for single event latchup testing. The LET of the ions was 104 MeV-cm<sup>2</sup>/mg. Two devices were used, S/N LAN3421 and S/N LAN3422. A fluence of 10<sup>7</sup> ions/cm<sup>2</sup> was used for each run

The devices were biased at 5.5VDC and 3.0VDC. Note that the bias applied to the core exceeds the maximum rated voltage of the part. Latchup was not detected.

*Antifuse Hardness*

345 MeV I-127 ions were used for single event antifuse hardness testing at normal incidence. The LET of the ions was 60 MeV-cm<sup>2</sup>/mg. Two devices were used, S/N LAN3421 and S/N LAN3422. A fluence of 10<sup>7</sup> ions/cm<sup>2</sup> was used for each run

The devices were biased at 5.5VDC and 3.0VDC. Note that the bias applied to the core exceeds the maximum rated voltage of the part. Antifuse rupture was not detected.



*Prototype RT54SX32S with hardened R-Cells. This device uses MEC 0.25  $\mu$ m technology and has a 5V core.*

*Single Event Upset*

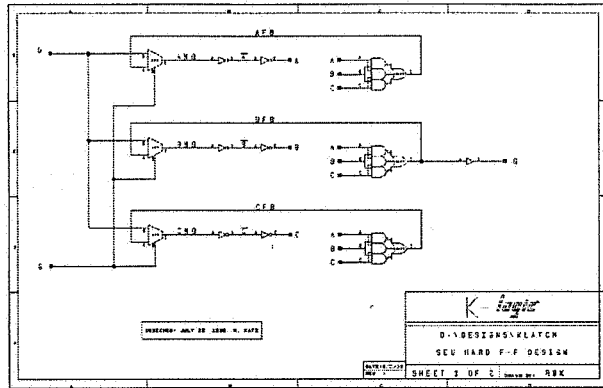
There were very few upsets detected with ion LETs ranging up to 104 MeV-cm<sup>2</sup>/mg. Please see the www site for the raw data and explanations and schematics of the DUT circuitry.

Most of the upsets detected in this test are in the "DOC" channel. This channel has a buffer between flip-flops in the shift register. Most if not all of the routes use direct connects. It was hypothesized that the direct connect, which is the fastest connection in this architecture (three different types, direct connect, fast connect, and routed) would be the most susceptible to transient upsets. This preliminary finding, subject to more analysis and data reduction, suggests that additional tests should be run. In this case the buffer should be placed and routed such that no direct connects are used but fast connects and routed signals are used for two of the channels and differences in upset rates measured. Additionally, although tests from low to moderate frequencies have not shown any significance, it is planned to conduct high-speed tests, exceeding 100 MHz.

Comparing DOH to DOVH strings, we see no errors on DOH but some on DOVH. DOVH has buffers hanging on the preset and clears. Note that the error monitor for DOVH [these two strings are TMR-hardened at the user level] had a few upsets. This suggests that the buffers had a small cross section for SETs.

Lastly, S/N LAN3422 had a few errors on DOS, a string of 200 flip-flops. No errors for this string were detected for S/N LAN3421.

The figure below shows the logic for the K-Latch. This forms the basis of the SEU-hardened R-Cell.



Logical structure of the K-Latch. This asynchronous TMR-based circuit does not require a free running clock to "scrub" SEUs.

As can be seen from the logical schematic, there are three latches and three voter circuits. This asynchronous configuration was designed such that there is no need to have a free running clock to "scrub" SEUs. For typical user-level TMR solutions, that is often a requirement. The implementation of the voter circuits ensures that the logic implementing the voters is hazard-free. This makes these TMR structures suitable for elements such as ripple counters or other applications where the output of the hardened circuit is used as a clock or other edge-sensitive input.

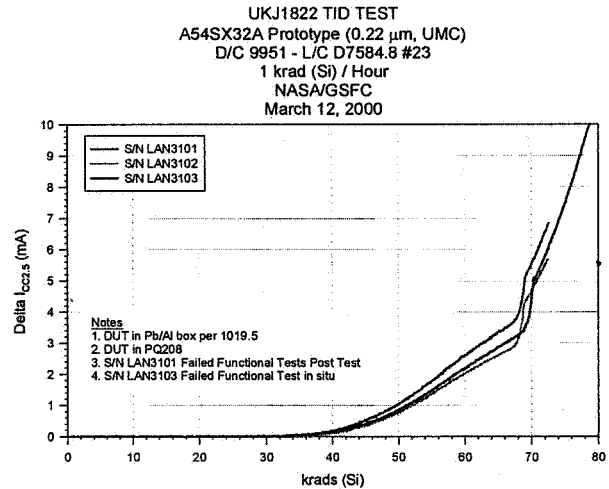
### A54SX32A - 0.22 μm/UMC Test Results

#### Introduction

This member of the SX-A series has a 2.5 V core. This variant, produced at UMC, is built with 0.22 μm technology. Note that other SX-A series devices are processed in 0.25 μm technology at MEC. SX-A devices from different foundries can not be considered the same device/design in all respects. As such, independent analysis and characterization is needed. This note will present some background information as well as some of the recent test data. A complete set of the latest SEE data is on-line at [http://rk.gsfc.nasa.gov/richcontent/fpga\\_content/SXA\\_Series/BNL1000/SX-A\\_UMC/Test\\_BNL1000\\_SX-A\\_UMC.htm](http://rk.gsfc.nasa.gov/richcontent/fpga_content/SXA_Series/BNL1000/SX-A_UMC/Test_BNL1000_SX-A_UMC.htm)

#### Total Dose

Three devices were irradiated at NASA Goddard Space Flight Center. Data was sampled every 5 minutes and *in situ* functional tests ran at the rate of once per hour. The bulk process used in this device utilizes shallow trench isolation. The results of the total ionizing dose test are shown below.



#### Single Event Latchup

345 MeV I-127 ions were used for single event latchup testing. The LET of the ions was 120 MeV-cm<sup>2</sup>/mg. These early prototypes had programming problems and "JTAG upsets" were observed. Further testing will confirm this and extend the SEL testing.

S/N LAN4001 was tested to a fluence of 3.9 x 10<sup>6</sup> ions/cm<sup>2</sup> before the apparent JTAG upset caused the run to be terminated. The device was biased at 5.5VDC and 2.75VDC. Latchup was not detected.

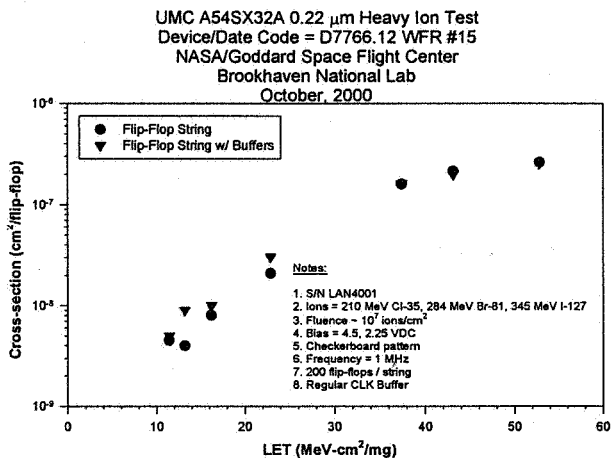
#### Antifuse Hardness

345 MeV I-127 ions were used for single event antifuse hardness testing at normal incidence. The LET of the ions was 60 MeV-cm<sup>2</sup>/mg. One device was used, S/N LAN4002. A fluence of 7 x 10<sup>6</sup> ions/cm<sup>2</sup> was used for each run. As described above, apparent JTAG upset caused the run to be terminated before a fluence of 10<sup>7</sup> ions/cm<sup>2</sup> could be achieved.

The device was biased at 5.5VDC and 2.75VDC. Antifuse rupture was not detected.

### Single Event Upset

SEU cross-section data is summarized in the chart below. The device was biased at the worst-case specified levels.



### Discussion

The flip-flop strings come in two pairs. The first pair, DOC and DOS, show little difference in SEU rates. The difference between these pairs is that the DOC shift register has a buffer between each shift register stage. In the SX/SX-A architecture, this leads to the use of a direct connect (in most cases, since the fanout from the C-Cell to the R-Cell is one) which would have the least capacitance, as compared to a fast connect (1 antifuse) and a regular connection (2 or more antifuses). There may be some residual upsets from the use of C-Cells and fast connect but they can not be seen at the frequencies tested so far. For the available frequency test data set, please see [http://rk.gsfc.nasa.gov/richcontent/fpga\\_content/SEU\\_Hardening/Test\\_BNL0800.htm](http://rk.gsfc.nasa.gov/richcontent/fpga_content/SEU_Hardening/Test_BNL0800.htm). It is planned to have a high-speed board built to further explore this issue.

The second pair of circuits are the two TMR-hardened strings. Both of these strings are hardened at the user level and not at the device level. No errors were detected on DOH. Note that DOVH differs from DOH since buffers are used to bias the presets and clears of the flip-flops and not tie-offs to a voltage rail. This SET detector is more sensitive than the one above since the asynchronous inputs to the flip-flop will catch and hold any transient of sufficient width to flip a memory element.

For the DOC/DOS strings, the glitch must be caught on a clock edge. However, the formulation of the DOC string results in the buffer having a fanout of one. Therefore, a worst-case direct connect (0 antifuses) can be used; the place and route software is

given the goal of using direct connects for each of the buffers in between sequentially adjacent flip-flops.

For the UMC 0.22  $\mu\text{m}$  SX-A FPGA, this can not be done for the DOVH string, since there must be a fanout of three for each buffer biasing either the preset or clear inputs. Obviously, if the fan out was reduced to one, this would maximize the number of SETs but make the number of errors from the TMR-hardened strings unchanged from the baseline version, since the upset would be voted out. However, the errors would be picked up on the error monitors. Since we are gathering our preliminary data, a different version of the test chip may be built for further testing and evaluation. Note, however, that the primary application of presets and clears for R-Cells use a rather heavy load, as most (but not all!) designs use this function for power-on initialization, and not "normal," operating logic. Some circuit applications, such as synchronizers, often make use of this input to clear out an incoming asynchronous signal.

---

### New FPGA Design Effort

An agreement between Aeroflex UTMC and Quicklogic was recently signed. Aeroflex UTMC has access to QuickLogic's ESP, FPGA, and metal-to-metal interconnect technologies. Technical progress will be reported here as results become available.

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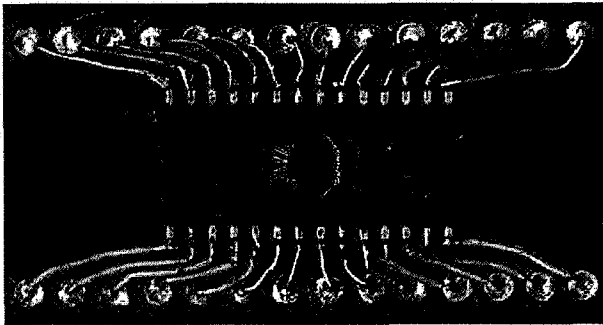
### Ramtron FM1608 FRAM

#### Summary

Two FM1608 devices were tested at the Brookhaven National Labs' Tandem Van de Graaff accelerator facility. Chlorine and Bromine ions were used and the device was dynamically biased. Both devices latched with Bromine. Device bias was a nominal 5.0V or a maximum 5.5V for all runs. Latchup currents exceeded the power supply's programmed current limit setting of 800 mA, with  $V_{CC} = 5.0V$ .

*Test Configuration*

Package: Plastic SOIC  
 Part Number: FM1608-120-S  
 Lot Code: MX4099938500  
 S/N: HOY20, HOY21  
 Bias:  $V_{CC} = 5VDC$  or  $5.5VDC$ . Part exercised continuously.  
 Ions  
 210 MeV Cl-35  
 284 MeV Br-81

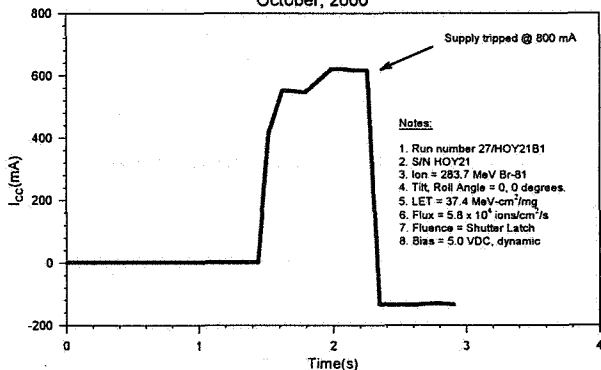


Ramtron FM1608 in an SOIC. SEL was not detected at an LET of  $22.9 \text{ MeV-cm}^2/\text{mg}$  at  $V_{CC}=5.5$  volts. SEL was detected at an LET of  $37.4 \text{ MeV-cm}^2/\text{mg}$  at  $V_{CC}=5.0$  volts.

*Test Results*

SEL was not detected at an LET of  $22.9 \text{ MeV-cm}^2/\text{mg}$  with a bias condition of  $V_{CC} = 5.5V$ . SEL was detected at an LET of  $37.4 \text{ MeV-cm}^2/\text{mg}$  with a bias condition of

Ramtron Heavy Ion Test  
 FM1608-120-S/MX4099938500  
 NASA/Goddard Space Flight Center  
 Brookhaven National Lab  
 October, 2000



*ICC strip chart of an FM1608 FRAM irradiated with Bromine. The device latched immediately when the shutter was opened, tripping the power supply' current limit.*

$V_{CC} = 5.0V$ . Some SEUs were recorded. For detailed test results, please see:

[http://rk.gsfc.nasa.gov/richcontent/MemoryContent/FRAM/FRAM1608\\_BNL1000/FM1608\\_BNL1000.htm](http://rk.gsfc.nasa.gov/richcontent/MemoryContent/FRAM/FRAM1608_BNL1000/FM1608_BNL1000.htm)

**Analysis of VHDL Code and Synthesizer Output**

The following is an excerpt from an analysis of a space flight design. This case study demonstrates two different design aspects. First, the HDL synthesizer, unknown to the design, generated an needlessly bulky structure for a simple TMR voter. Secondly, since the implementation of the voter is hidden from the user, it was not obvious that a single event upset (SEU) through the combinational logic could result in a glitch on the "hardened" clock signal.

Triple modular redundancy (TMR) is selectively used to effectively harden select flip-flops in the design. The detailed design of the logic is done by the Synplicity synthesizer, Revision 6.0. There are several issues with this circuit. For this examination, the output of the synthesizer was analyzed as well as the chip database, after "combining" and place and route operations. The Synplicity synthesizer outputs an EDIF netlist. For analysis purposes, this was first converted into a Viewlogic compatible netlist and from that format a schematic was generated. To analyze the final chip design, the Actel-compatible database was output into a VHDL structural netlist that was analyzed by hand. Both netlists represented the same logic function and correctly implemented the Boolean logic equations.

First, it was seen the TMR logic was needlessly bulky, using three C-Cells for the voter. This function can easily be realized by a single 4:1 mux<sup>5</sup>. The Synplicity-generated logic will slow the circuit and use more logic resources than are required. The figure below shows the output of the Synplicity logic synthesizer.

Secondly, one sample of logic showed that using the TMR structure resulted in a static hazard. Other sections of the logic must be examined for a similar fault.

<sup>5</sup> R. Katz, et. al., "SEU Hardening of Field Programmable Gate Arrays (FPGAs) for Space Applications and Device Characterization," IEEE Transactions on Nuclear Science, 1994.

The structure with the problem was a 2-bit synchronous counter with the output of the MSB being used to drive a ¼ speed clock.

```
-- Divide 25 MHz (40 ns) clock by 4
-- to produce 6.25 MHz clock (160 ns)
-- This clock should be placed on
-- an internal global buffer
```

```
clkint1: clkint
Port Map ( A => clk_div_cnt(1),
          Y => clk_div4
        );

clkdiv: Process (reset_n, clk)
Begin
  If reset_n = '0' Then
    clk_div_cnt <= "00";
  Elsif clk = '1' And clk'EVENT Then
    clk_div_cnt <= clk_div_cnt + 1;
  End If;
End Process clkdiv;
```

Since the output of the TMR voter is used as a clock, the combinational logic constituting the voter must be guaranteed to be hazard-free. Unfortunately, this can not be guaranteed at this time and the Actel product engineer is analyzing this particular situation.

In general, this is not a recommended circuit. The following warning was given in both a paper<sup>6</sup> and an application note<sup>7</sup> on the use of TMR:

Care is needed when using TMR circuits. First, the output of the voter may be susceptible to a logic hazard "glitch." This is not a problem if the TMR is feeding the input of another synchronous input. However, the TMR output should never feed asynchronous inputs such as flip-flop clocks, clears, sets, read/write inputs, etc.

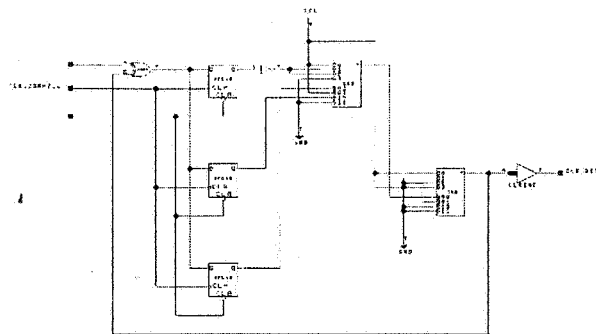
While this note was written for Act 1 and Act 2 devices, the logic discussion is in fact general.

### Startup Transients and Requirements

Many programmable logic devices have device-specific startup requirements and characteristics. Some can be quite subtle, such as the device's startup time. Others can be current requirements during the startup transient that are

<sup>6</sup> R. Katz, et. al., "SEU Hardening of Field Programmable Gate Arrays (FPGAs) for Space Applications and Device Characterization," IEEE Transactions on Nuclear Science, 1994.

<sup>7</sup> "Design Techniques for Radiation-Hardened FPGAs," September 1997, K. Hayes and R. Katz.



*Schematic of HDL-synthesized implementation of the MSB of a counter. Note that the synthesizer used 3 C-Cells to implement a voter. The voter can not be guaranteed to be hazard-free and its output is used as a clock.*

higher than the normal operating current for the device. In a previous edition of Programmable Logic Applications Notes<sup>8</sup> as well as several papers<sup>9</sup>, startup transient current characteristics were described.

Some manufacturers specify transient characteristics for their devices, guaranteeing operation under all environmental conditions and process corners. Other manufacturers do not specify startup current characteristics and requirements. In either case, conservative design practices are recommended to ensure reliable operation. This note presents some data on Actel RT54SX32 devices (0.6 µm, MEC) and reviews specifications for Xilinx XQR4000XL and Virtex 2.5V FPGAs. Note that measured data is for information purposes only - environmental conditions, operating history, input stimulus, etc., as well as part-to-part and lot-to-lot variations can effect the measurements. Many total dose evaluations now include samples of the startup current transients.

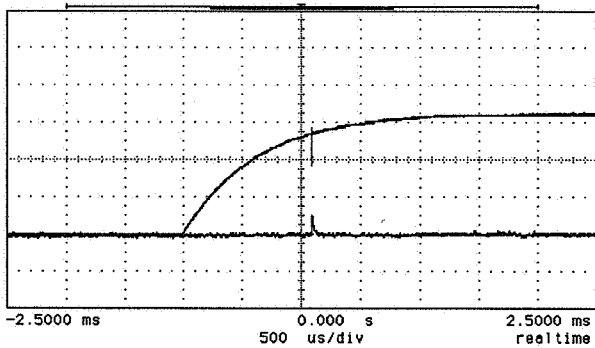
### Actel

The Actel SX and SX-A series devices are produced in different feature sizes and foundries. From a recent total ionizing dose test of 0.6 µm, MEC-produced RT54SX32s, one pair of startup transient current curves was selected at random. The

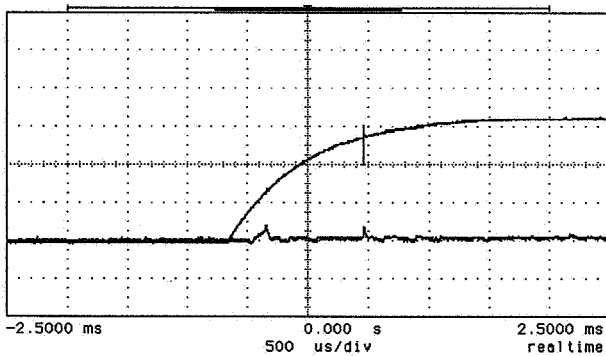
<sup>8</sup> See EEE Links, Programmable Logic Application Notes, July 1996 for startup transient current data on the A1280A.

<sup>9</sup> For example, Total Dose Response of Actel 1020B and 1280A Field Programmable Gate Arrays, RADECS 1995 and Total Dose and Dose-Rate Effects on Start-up current in Antifuse FPGA, RADEC 1999.

first curve was pre-irradiation; the second was after an exposure to 98 krad(Si). All tests were conducted at room temperature and under nominal voltage conditions. An HP 6629A power supply was used to drive the input. Voltage is scaled at 1 V/Div and current at 100 mA/Div. As can be seen from the charts, a second current peak appeared after irradiation. Note that all currents measured are approximately 50 mA or less.



*Startup current transient (3.3V supply) of an RT54SX32 pre-irradiation. Voltage at 1V/Div and current at 100mA/Div.*



*Startup current transient (3.3V supply) of an RT54SX32 post-irradiation (98 krad(Si)). Voltage at 1V/Div and current at 100mA/Div.*

**Xilinx**

There are two sets of requirements for the power-on transient for Xilinx XQR4000XL and Virtex 2.5V FPGAs. They are the rise time and current capability of the power supply. It should be noted that unlike Actel FPGAs where slower power supply rise times result in higher current values, in Xilinx devices, *faster* rise times result in higher current values. Lastly, the Xilinx devices have current rise time requirements.

The following is taken from the latest information<sup>10</sup> and will be updated as new specifications and application notes become available. Note that some of the specifications and characteristics, although on radiation hardened data sheets, reflect either commercial or industrial operating conditions. In some cases, information is not available on the radiation hardened data sheet and specifications are taken either from commercial data sheets or application notes.

*XQR4000XL*

The slowest power supply rise time for this series of parts is 50 ms. While many power supplies can meet this specification easily, note that some spaceborne power supplies may have longer rise times. Considerations for power supply designers include in-rush currents on capacitors as well as system-level EMC requirements.

The minimum current for XQR4000XL series devices is broken into two groups: XQR4013-36XL and the XQR4062XL and are shown on the chart. Note that according to the specification, the values refer to commercial and industrial grade products only, with the transition measured from 0 VDC to 3.6 VDC. *Actual* currents may be higher than the minimums specified.

Note 3 in the specification states that the duration of the peak current level will be less than 3 ms.

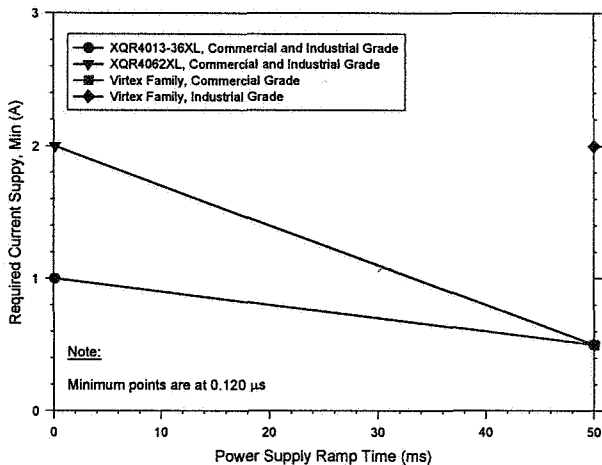
*Virtex*

Complete power supply requirements are not yet specified in the radiation hard data sheet. Some of the following information is taken from the commercial data sheet.

Similar to the XQR4000XL series above, the slowest power supply rise time for this series of parts is also 50 ms. The fastest suggested ramp rate is 2 ms. This is considered slow for some power supplies. The parameter measurement criteria on the radiation hard data sheet is from 1 VDC to 2.375 VDC.

<sup>10</sup> QPRO XQR4000XL Radiation Hardened FPGAs, DS071 (v1.1) June 25, 2000, Product Specification; QPRO Virtex 2.5V Radiation Hardened FPGAs, DS028 (v1.0) April 25, 2000, Advanced Product Specification; Virtex 2.5V Field Programmable Gate Arrays, DS003 (v2.2) May 23, 2000, Final Product Specification, Powering Virtex FPGAs, XAPP158 (v1.1), November 15, 1999.

The data sheet only specifies a minimum required current supply for Virtex devices at a power supply rise time of 50 ms. According to the non-military specification, it is 500 mA for commercial grade devices and 2 A for industrial grade parts. Additionally, shorter power supply rise times will result in higher currents. The duration of peak currents will be less than 3 ms.



**Nonvolatile, Reprogrammable FPGA Data**

ProASIC (Prototype) SEE TEST

Brookhaven National Labs

October 2000

*This is a summary of the third round of SEE testing on prototype ProASIC microcircuits. The first two test sessions used 252.5 MeV Br-81 ions and only limited data was obtained as a result of the device being highly susceptible to Shutter Latch™. This test used lower LET ions with the goal of obtaining a better understanding of the SEL and SEU characteristics of this part.*

The purpose of this test was to determine the approximate Single Event Latchup LET<sub>TH</sub> and make SEU cross-section measurements. Two runs were conducted. The A500K050 (prototype) device was from lot ZA934946/29104125 and was in a PQFP208 package. The device was biased at nominal voltage levels - 3.3V (I/O) and 2.5V (Core). 210 MeV Cl-35 were used for all runs.

During the first run, SEL was observed at a fluence of approximately  $2 \times 10^6$  p/cm<sup>2</sup>. The DUT was at an angle of 60 degrees with respect to the beam, giving an LET of 22.9 MeV-cm<sup>2</sup>/mg.

SEL was not detected during the second run. The fluence for the run was  $10^7$  p/cm<sup>2</sup>. The DUT was at an angle of 45 degrees with respect to the beam, giving an LET of 16.2 MeV-cm<sup>2</sup>/mg. A total of 385 upsets were detected. The test pattern has 400 flip-flops. At this LET, we can estimate the cross-section at  $9.6 \times 10^{-8}$  cm<sup>2</sup>.

Gatefield A500K050 Heavy Ion Test  
 Lot Code: ZA934946/29104125  
 NASA/Goddard Space Flight Center  
 Brookhaven National Lab  
 October, 2000

