Lithium Ion Battery (LIB) Charger

Spacesuit Battery Charger Design with 2-Fault Tolerance to Catastrophic Hazards

By

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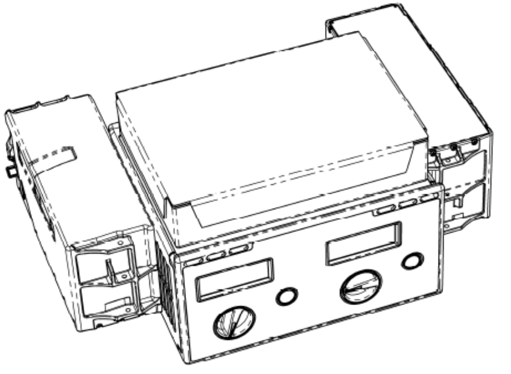
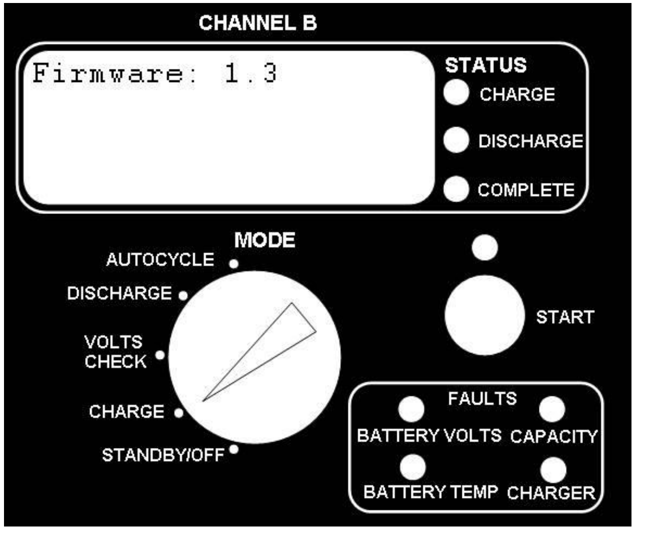
Charger Top Level Description

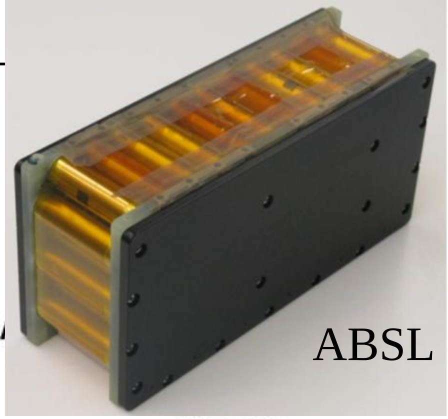


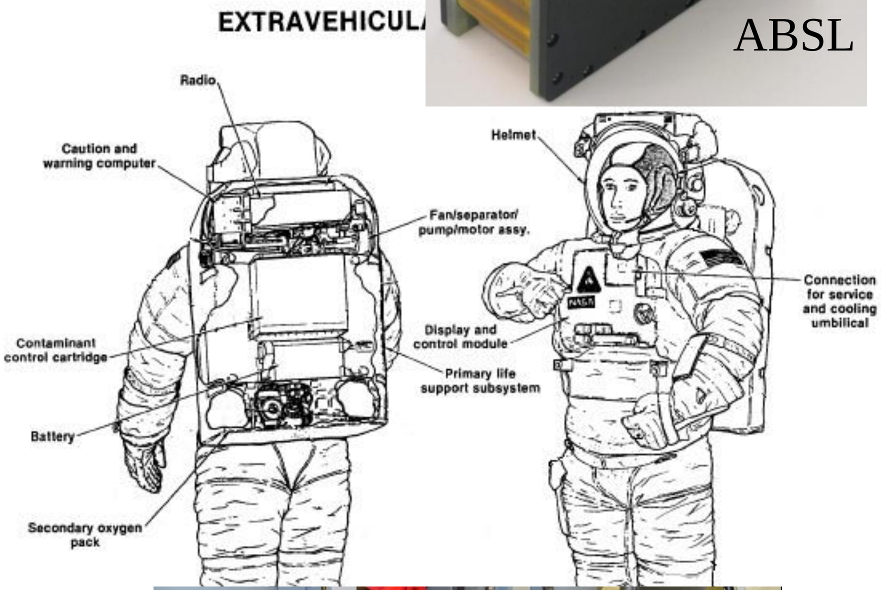
- 2 independent charger channels inside single enclosure
- Capable of servicing 2 EMU LLBs simultaneously and independently while operating inside Shuttle (28Vdc) and ISS (120Vdc) pressurized cabin
- Charge Modes
  - 5A to 20.6V terminating when cell banks OCV reach 4.09V during current taper phase (120Vdc)
  - 2.5A to 20.6V terminating when cell banks OCV reach 4.09V during current taper phase (28Vdc)
  - LLB cell bank balancing if needed
- Discharge
  - ~1.3A to 16.0V (or 3.0V/cell bank)
- Volts check
  - Measures cell bank OCVs
  - Measures battery CCV after 9A, 5s pulse
- Autocycle
  - Discharges remaining LLB capacity
  - Full recharge with cell bank balancing (if needed)
  - Full discharge to assess LLB capacity (health)
  - 10Ah recharge to put LLB at ~30% SoC for storage
- Mode, LLB parameters, and faults are displayed on each channel's LCD and LED
- Designed and built by Electrovaya



EMU Long Life Battery Description

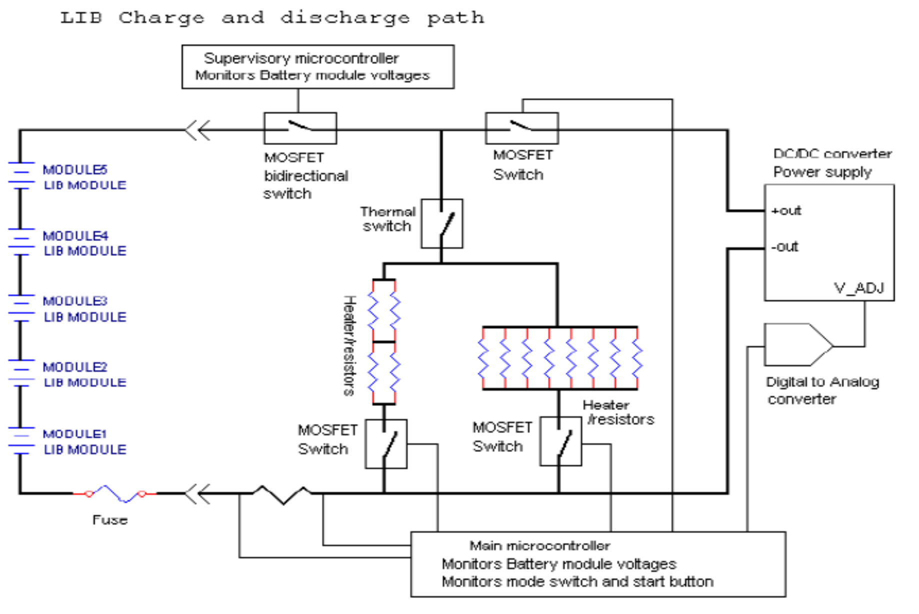
- Life limited pouch cell design abandon for longer life COTS cell approach
- Candidate 18650 Li-ion cell building block to be down-selected at CDR
  - MoliJ 2.4Ah (Apr-07 date code)
  - LV 2.15Ah (Apr-07 date code)
- Cell brick consists of 16P cell banks connected in series (5S) built by ABSL
- Interconnecting PCB provides
  - Fuse: 15A slow blow
  - PTC sense line current limiters for cell banks
  - Thermistor
- Housing and lid essentially unchanged from previous EMU LIB design





Top Level Charger Channel Electrical Schematic

- LLB has 5 cell banks (modules) in series with fuse in negative leg
- Main micro controls mode functions of each charger channel and will interrupt charge/discharge when faults conditions occur
- Supervisory micro independently measures cell bank voltages and can interrupt charge/discharge when faults conditions occur
- Discharge energy is dissipated through heater resistors



Charger Electrical Design and Safety Features

- Main Microcontroller Roles
  - Monitor the voltages of the 5 cell banks (modules)
  - Monitor and control the battery charge and discharge currents
  - Control cell bank equalization and charge/discharge termination
  - Managing the data buffer and sending display requests
- Supervisory Microcontroller Roles
  - Independently monitor cell bank voltages and battery current
  - Shuts down charger in case main μ malfunction (watchdog)
  - Independently votes on charge completion signal to be sent to display
- Display Microcontroller Roles
  - Drives the LED and LCD displays
  - Independently votes on appropriateness of charge completion signal
  - Transfers battery and cell bank voltages, battery current and temperature to USB
- USB Microcontroller Roles
  - Performs the one way USB serial communications

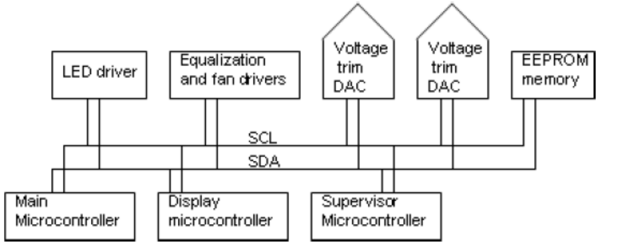


Figure 29: I2C bus block diagram

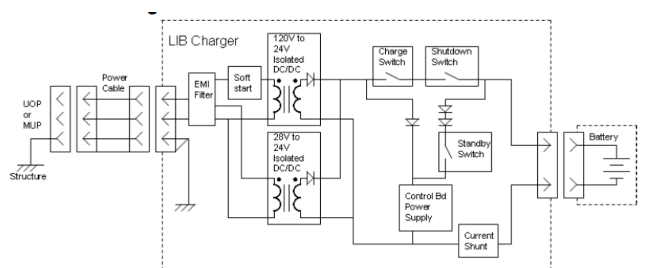


Figure 2: Charger power supply block diagram (one channel)

Charge Path and Algorithm

- Charge Algorithm
  - Bulk charge all 5 cell banks in series at 5A until first hits 4.09V under load (through cell bank sensing lines that are PTC device protected)
  - Interrupt charge for 2 minutes, measure cell bank OCVs, and resumes 5A charge
  - When the highest cell bank loaded voltage (CCV) reaches 4.12V, charger begins constant voltage taper charge mode
  - If highest bank OCV is more 8 mV from lowest other, pulse equilibration discharge of that module thru sense lines repeat until OCVs are within 8 mV mV
  - Restart bulk charging pulses to 4.12V until first cell bank OCV hits 4.10V, repeat equalization as necessary

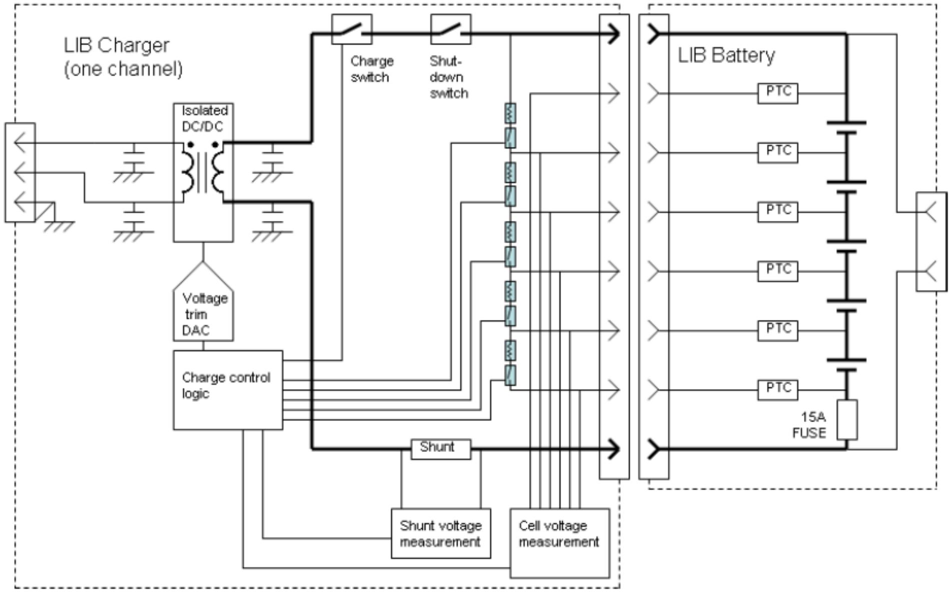


Figure 19: Block diagram of charge path

Over and Under Charge Controls

- >3 Levels of Overcharge Controls
  - Outputs of 120Vdc and 28Vdc converters are hardware limited to 22.0V (4.4V/bank)
  - Main micro firmware shuts down charge if bank voltages > 4.2V (TBV)
  - Supervisory micro firmware shuts down charge if bank voltages > 4.2V (TBV)
  - LLB cells and cell banks have been verified to benignly tolerate overcharging to 4.4V and reach a safe equilibrium
  - LLB cell Current-Interrupt-Device (CID) proven to prevent cell bank overcharge
- 3 Levels of Under Charge Control to protect against false "Go for EVA"
  - 3 microcontrollers (main, super, and display) measure voltages and must agree to display charge complete message (green LED)
  - Charge capacity achieved is displayed on the LCD and relayed to ground per FEMU-R

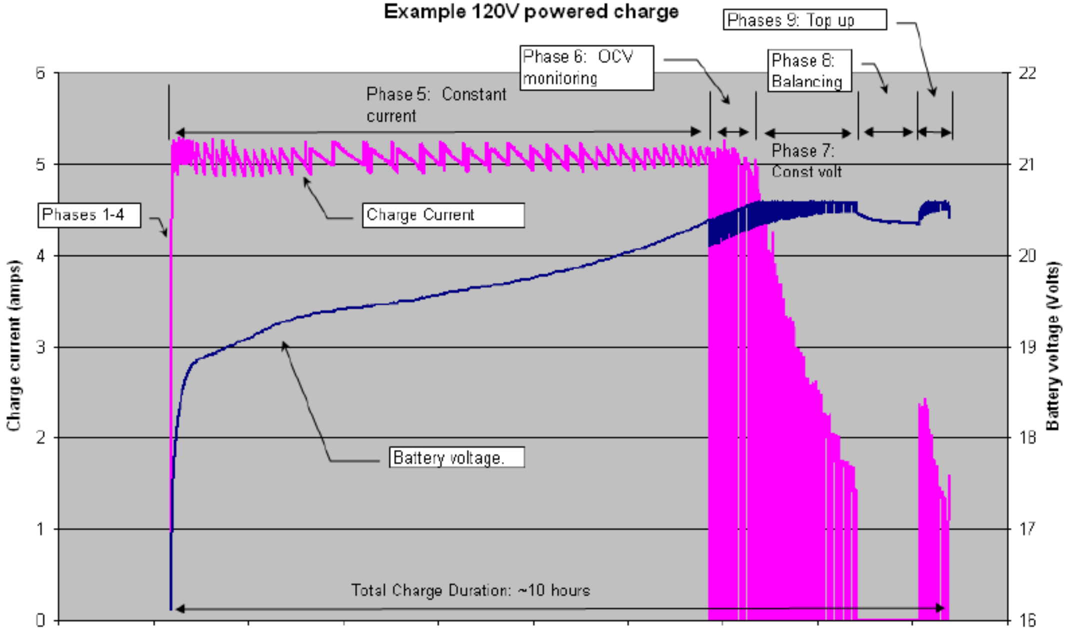
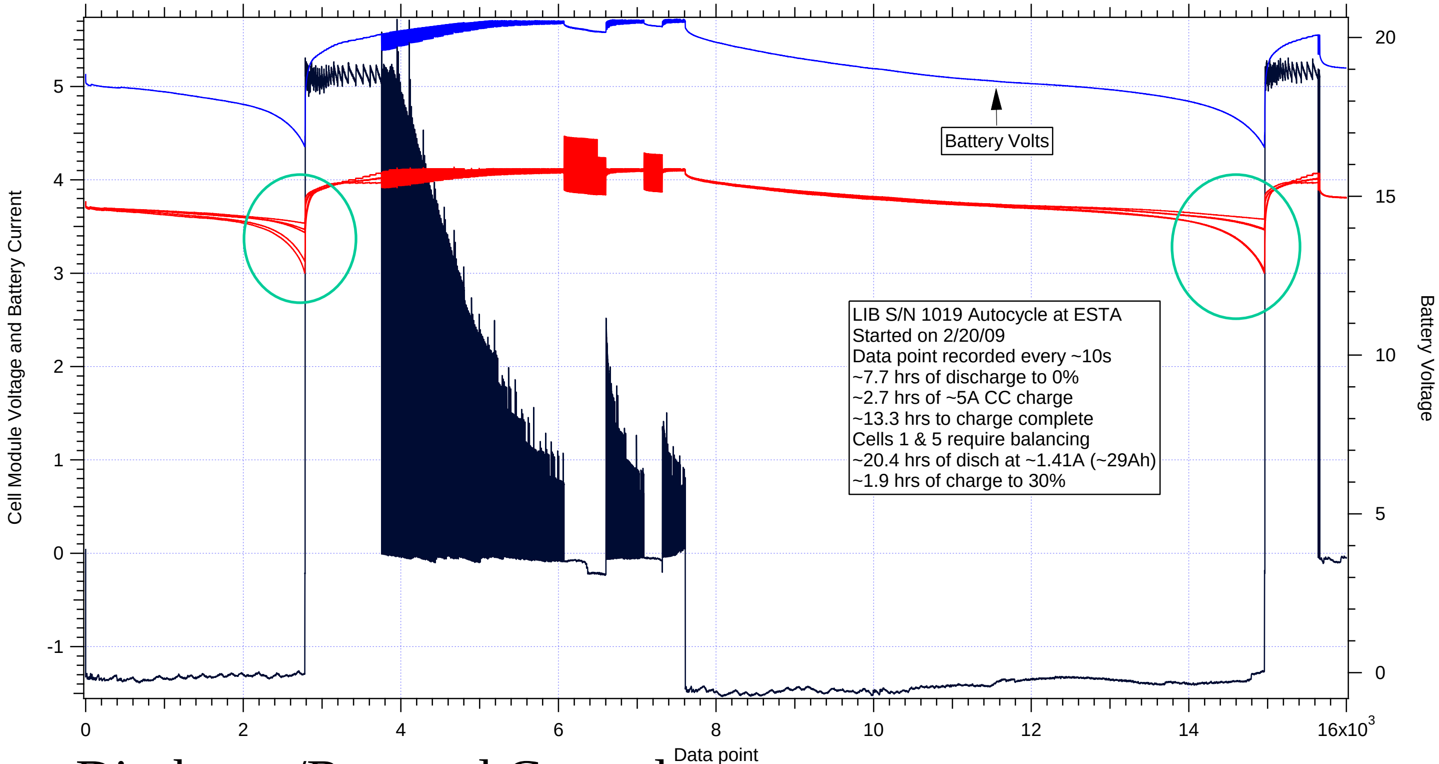


Figure 20: Example 120V powered charge

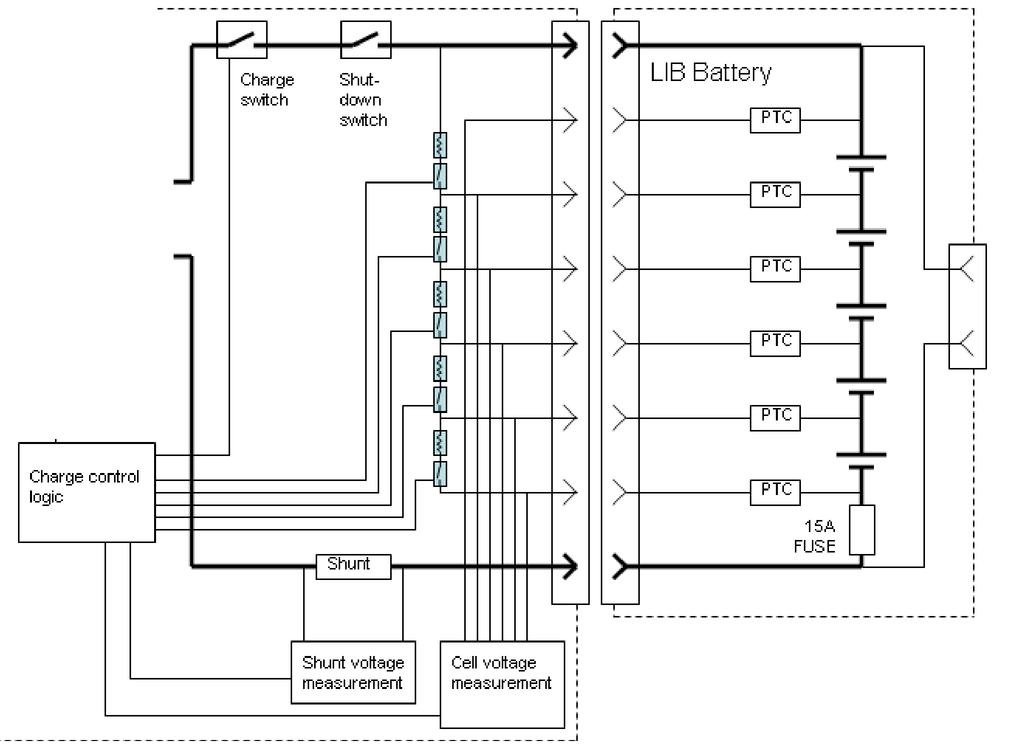
Over Discharge Controls

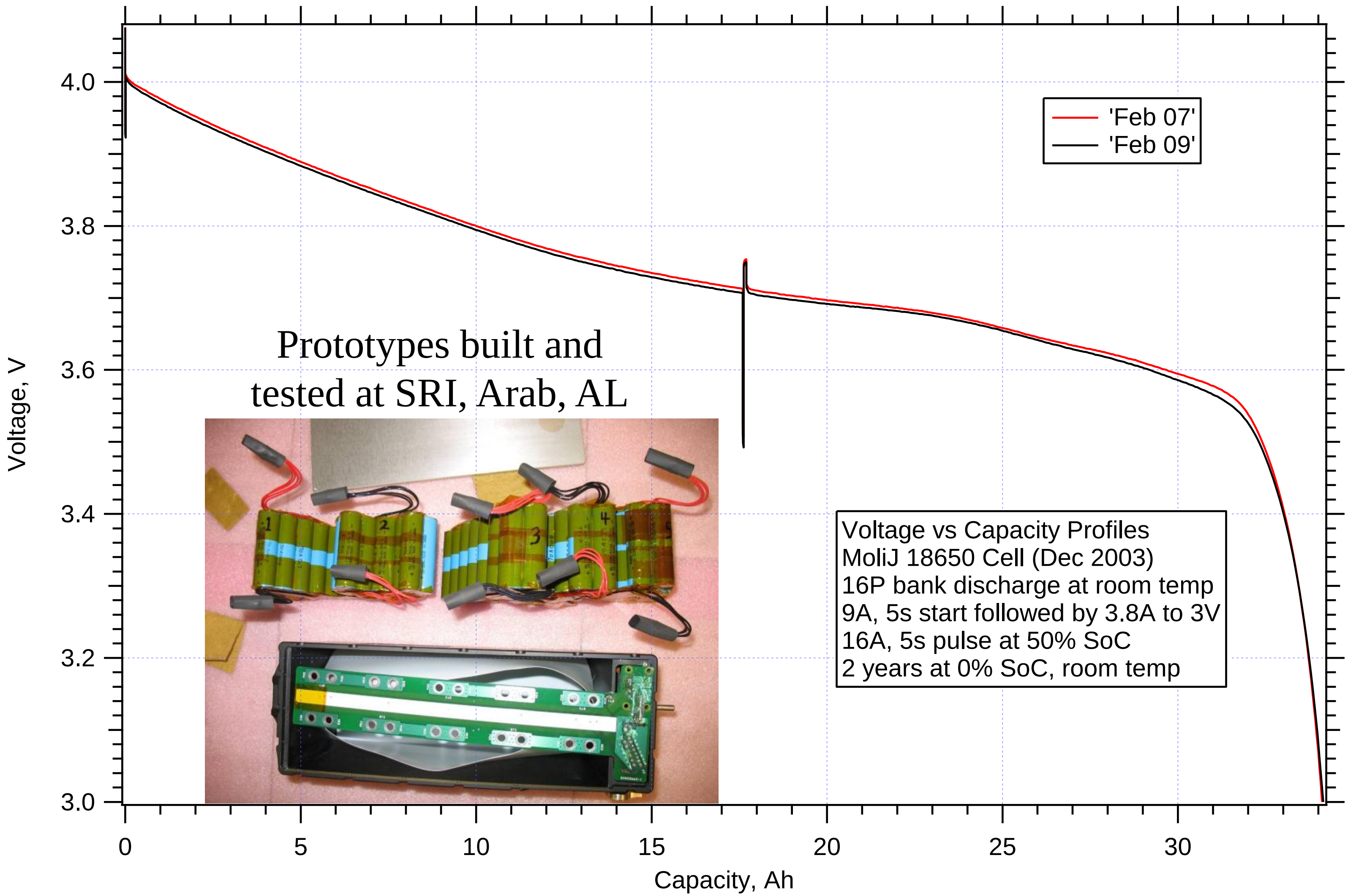


- Over-Discharge/Reversal Controls
  - Main micro firmware shuts down discharge if battery voltages < 16.0V
  - Main micro firmware shuts down discharge if any cell bank voltage <3.0V
  - Supervisory micro firmware shuts down charge if bank voltages > 4.2V
  - LLB cells and 16P banks proven to tolerate overdischarge into reversal without hazard

Cell Bank Balancing Circuits

- Cell Bank Balancing Algorithm
  - Triggered during constant current taper mode of charge
  - Each cell bank is connected to its own individual discharge resistor and switch in the charger
  - Cell banks with higher OCVs are bled down through MOSFET driven connection to a cartridge heater (~0.5A) for a 2 minute interval
  - Cell bank OCVs are re-measured for 2 minutes
  - Process repeats until OCVs are balanced enough to resume taper charge of all banks





Excellent storage life demonstrated with negligible degradation/variation.
8.9 hours of EVA runtime with 5+ year old cells at room temperature.

LLB Thermistor Circuit

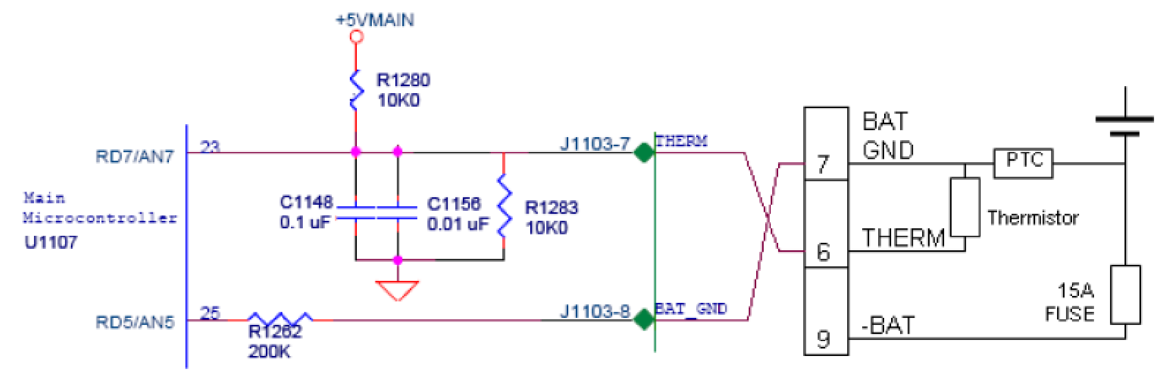
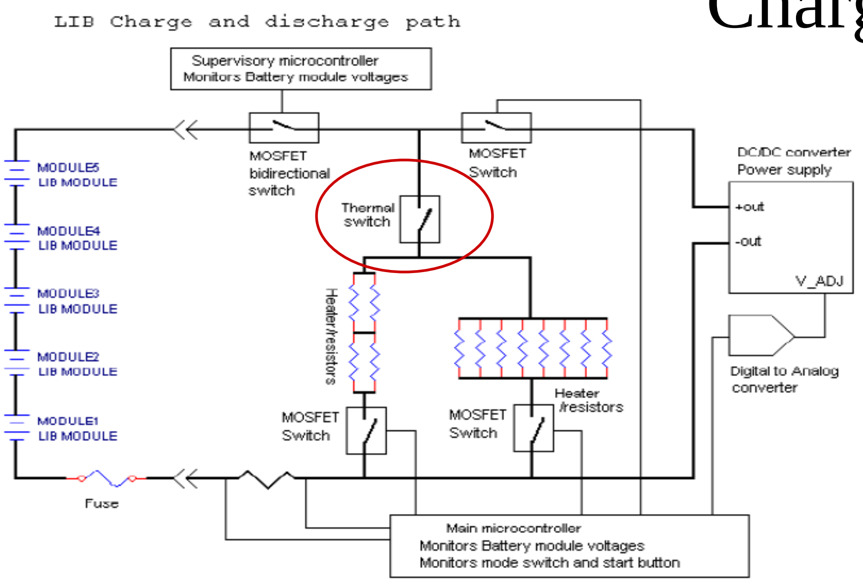


Figure 24: Battery thermistor sense circuit

- LLB thermistor resistance is converted into a voltage with above circuit
- Main micro firmware converts voltage to a temperature
- Temperature is displayed on charger channel LCD only during
  - Volt check mode when cell bank OCVs are displayed
  - When temperature is outside 10 to 45 C range (temp fault LED also triggered)
- Why isn't Temp Fault used to inhibit overheating LLB by electrical abuse?
  - 3+ controls already in place to prevent overcharge and overdischarge/reversal
  - LLB is already > 2 fault tolerant against external short circuit (fuse, bank separator, coatings)
  - Thermistor failure would permanently disable servicing of that LLB by the Charger
  - Inhibit would prevent servicing LLB during a cabin temperature (<10 and >45 C) anomaly

Charger Thermal Control

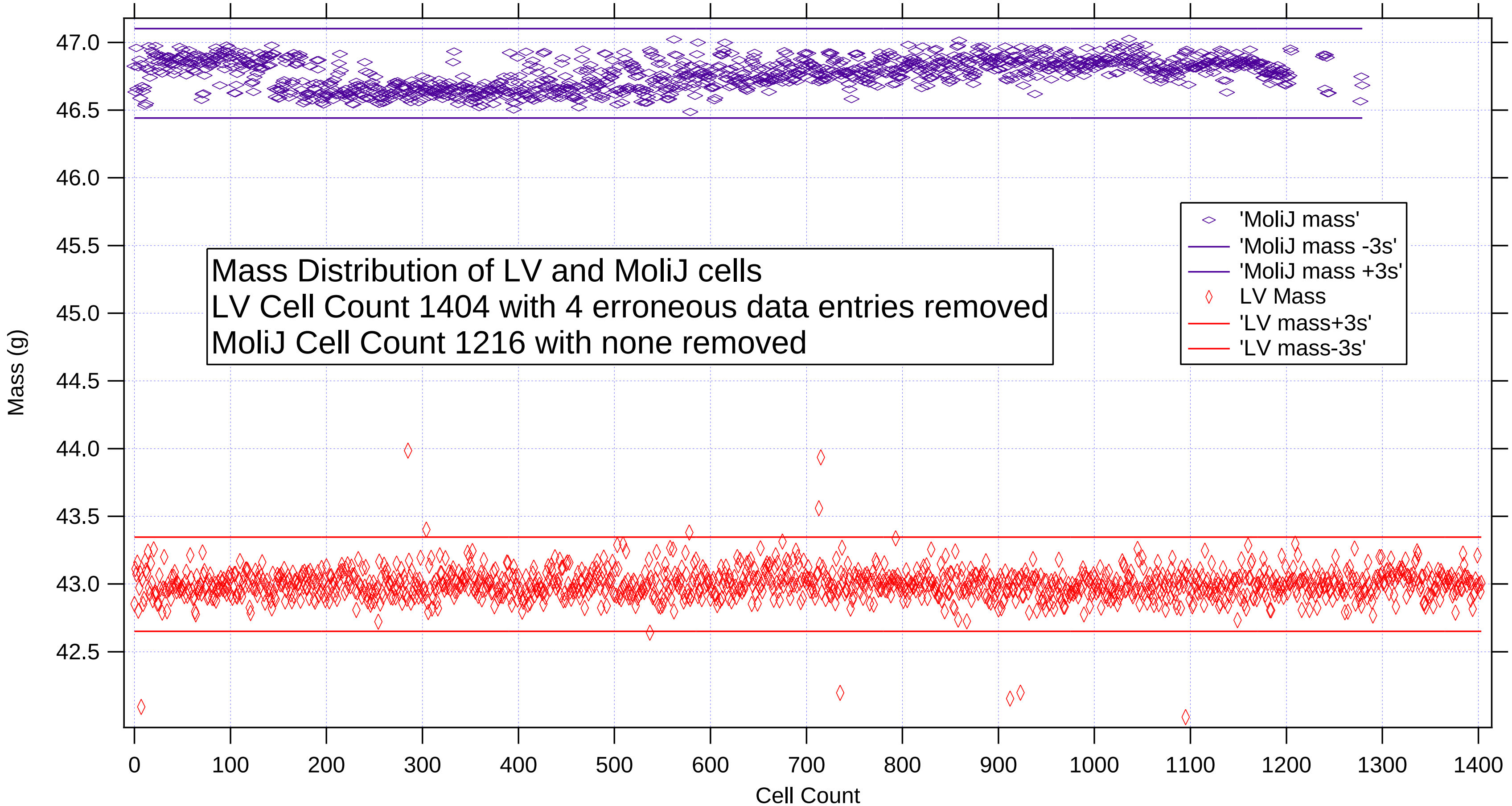


- Charger heat dissipating components are tied to heat sinks that are fan cooled
  - Maximum heat generation is during discharge (30W per channel)
- Fan cooled thermal control system proven with no natural convection environment of orbiting pressurized cabins
- Overheating of charger (after fan failure) is prevented by thermal switch (87 C) connected between banks of cartridge heaters
- Vicor power supplies will also shut down when overheated
- Firmware detects discharge current interruption and displays temp fault message on LCD and LED

18650 Cell Acceptance Procedure Outline

- Serialization and Receiving Inspection
  - Serialize each cell with bar code label
  - Strip cell shrink wrap for visual inspection
  - Mass and dimensional measurements
  - Populate trays with 128 cells
- Leak test batches of 256 cells (two 128 cell trays)
  - Thermal cycle
  - Vacuum cycle with Residual Gas Analysis
    - Quarantine any pair of trays with detectible electrolyte gases
- Electrochemical Testing (128 cell trays)
  - Cycle 1 (Initial OCV, AC Imp, Initial Charge, OCV, 7 day rest)
    - C/10 Charge
  - Cycle 2 (Discharge 1, Charge 2, Discharge 2)
    - C/10 Discharge and C/10 Charge
  - Report
    - Self-discharge Capacity = Discharge 2 – Discharge 1
    - DC resistance calculated at initial, 100% and 0% SoC
    - Reject any cell outside average   3 sigma range for all parameters

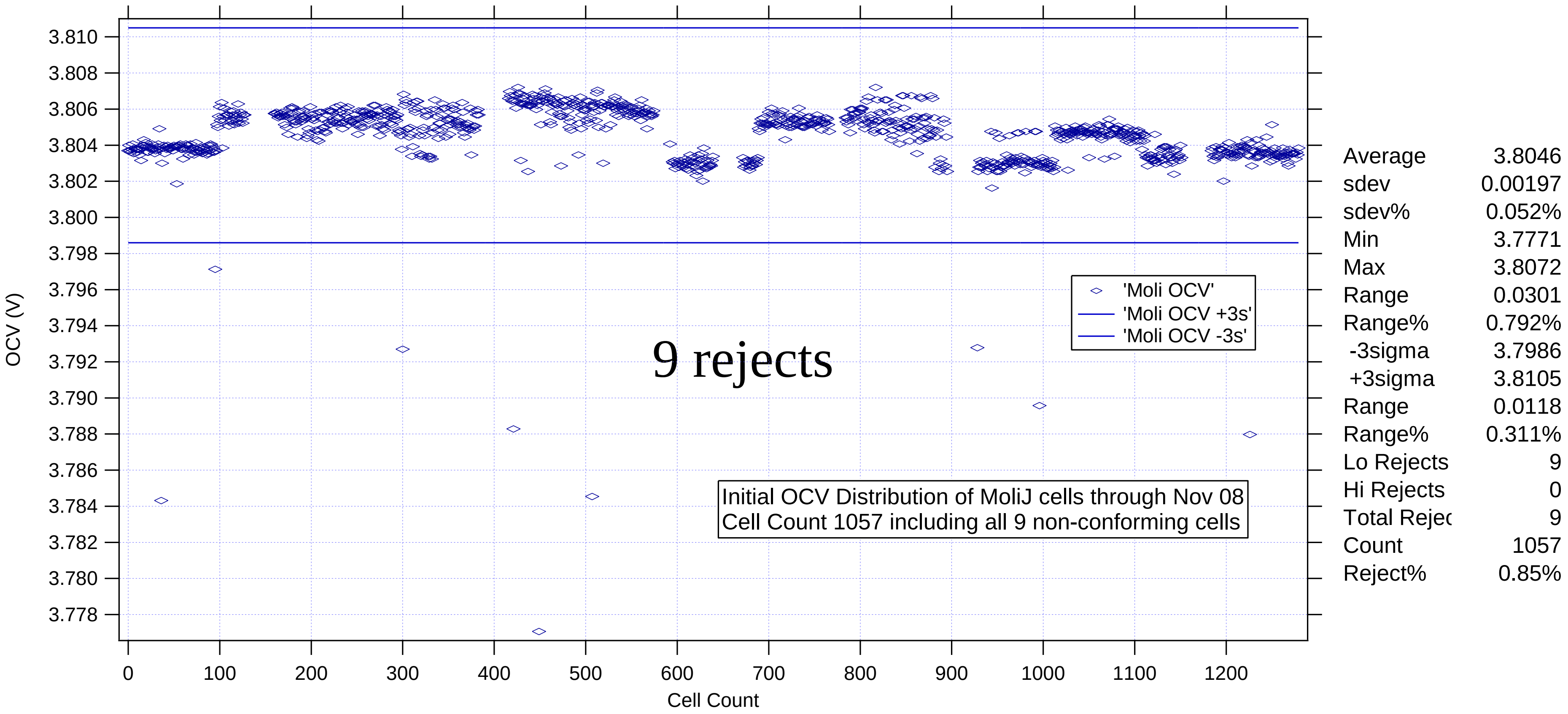
Comparison of Cell Mass Distributions



MoliJ 6σ range is 0.66g (1.4% of mean) without scrubbing

LV 6σ range is 0.57g (1.3% of mean) after 1st scrub of outliers

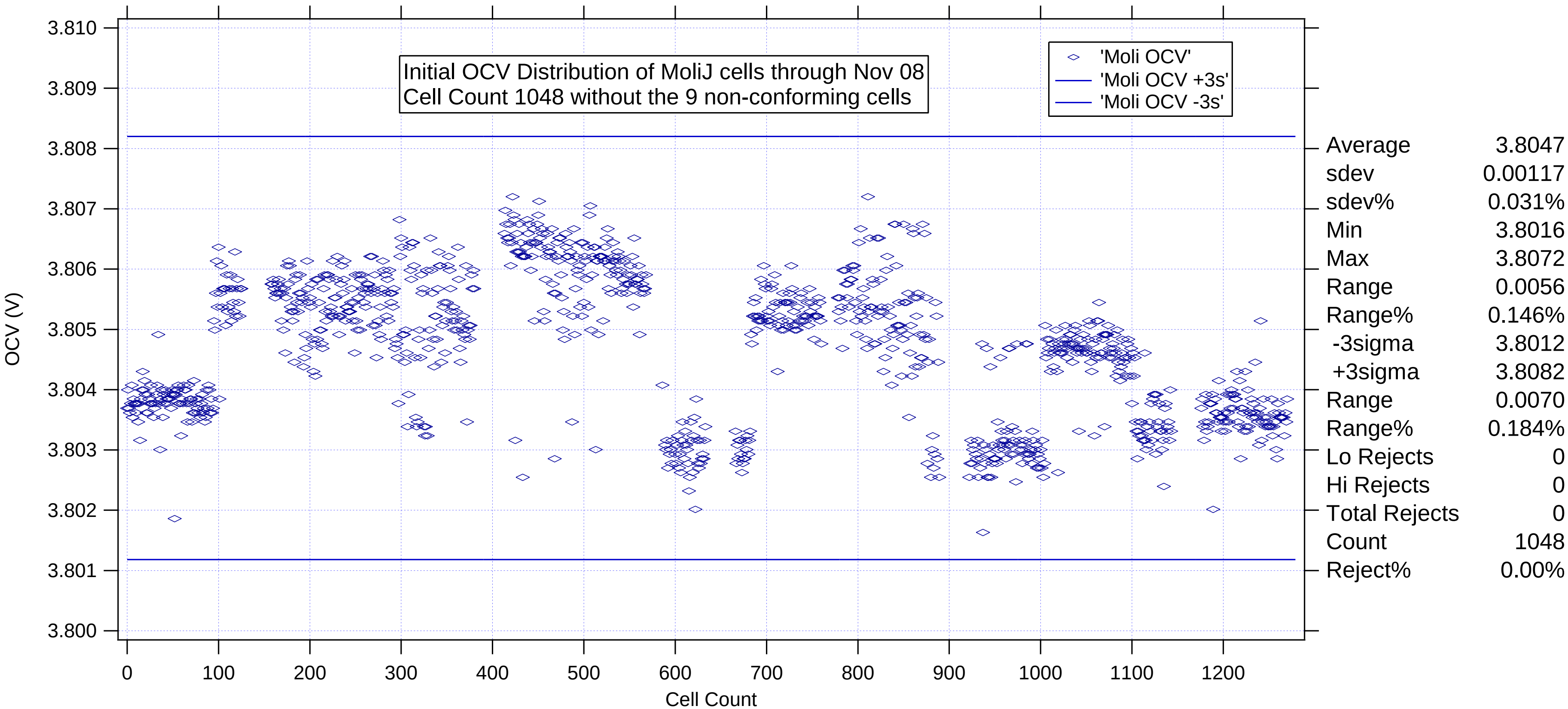
MoliJ Initial OCV



6σ range is 118 mV (0.311% of mean)

Note: Measurements taken in Sep 08 and cell date code is Apr 07 (17 months at 50% SoC, RT and 0°C)

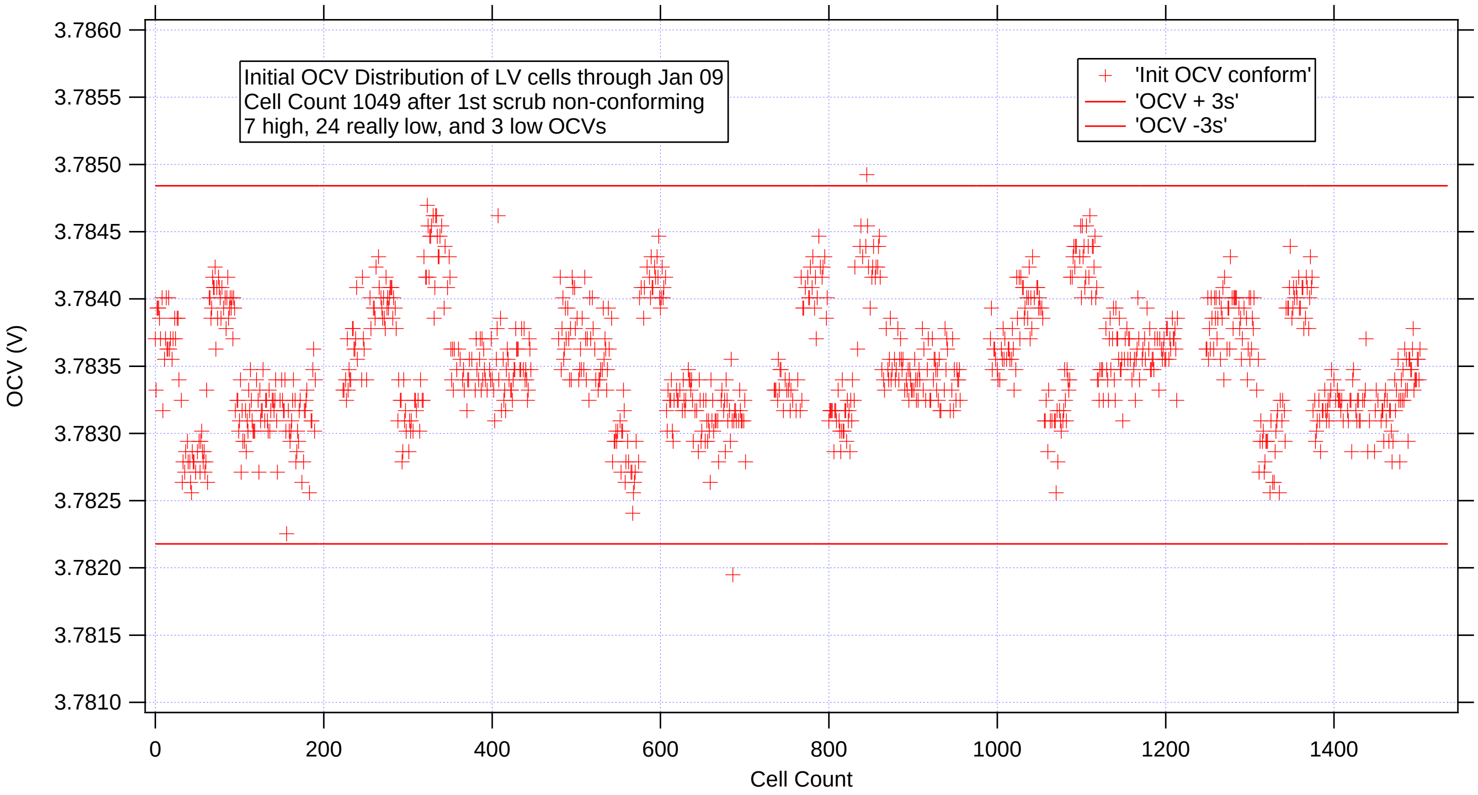
MoliJ Initial OCV after scrubbing the 9 cells



6σ range improves from 11.8 mV (0.311%) to 7 mV (0.184%)
No more outliers with this tighter 3σ range

LV initial OCVs scrubbed a 3rd and final time

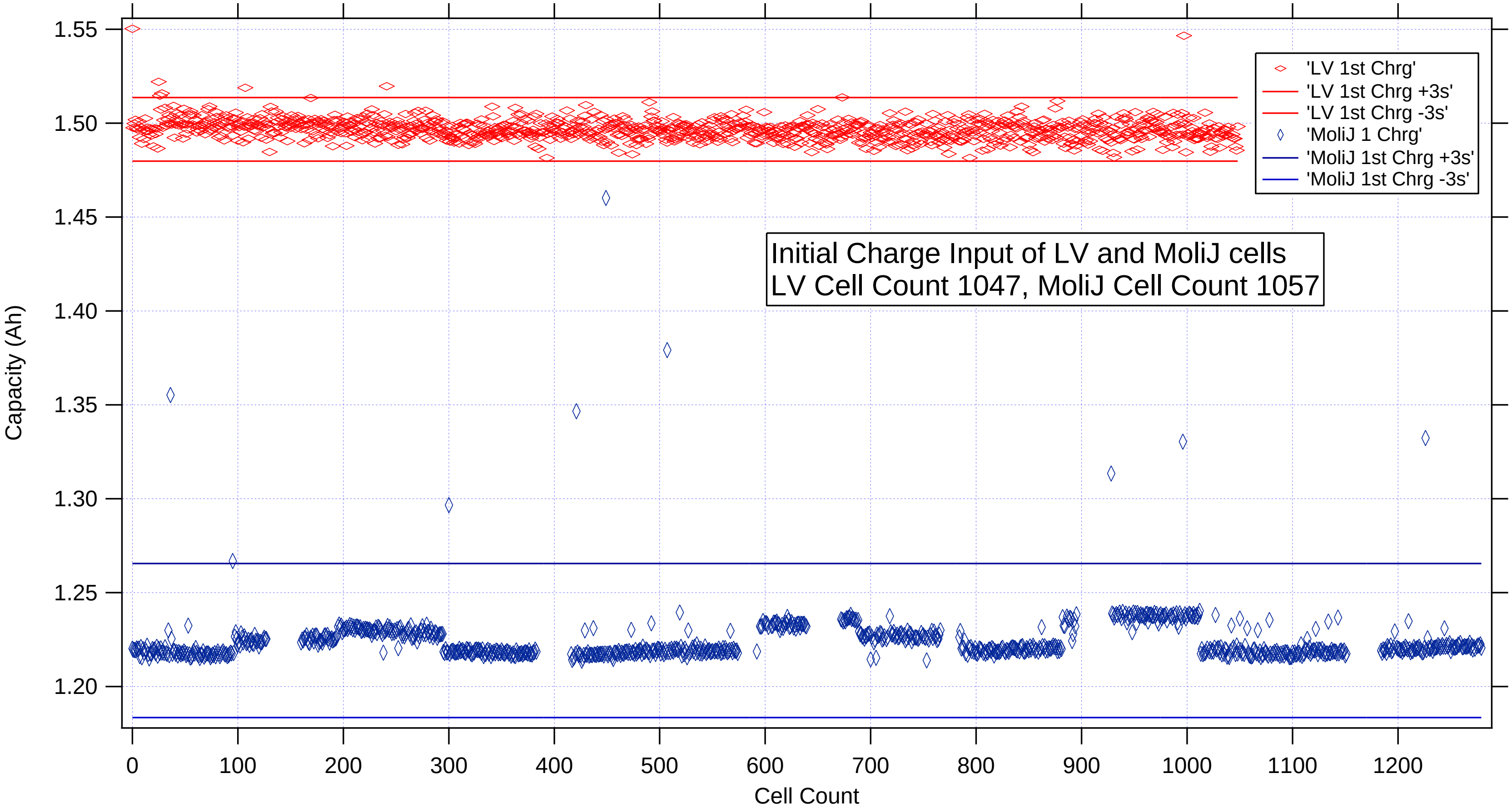
Stdev is at 0.4 mV (0.012%), which is better than 1.2 mV (0.031%) for Moli



Average	3.7835
sdev	0.0004
sdev%	0.012%
Min	3.7819
Max	3.7849
Range	0.0030
Range%	0.079%
-3sigma	3.7822
+3sigma	3.7848
3sRange	0.0027
3sRange%	0.070%
Low Rejects	1
High Rejects	1
Total Rejects	2
Count	1023
Reject%	0.10%

One more high and low OCV outlier exist, but 6σ range is 2.7 mV (0.07%) after 18 months!!

Comparison of Initial Cell Charge Capacity

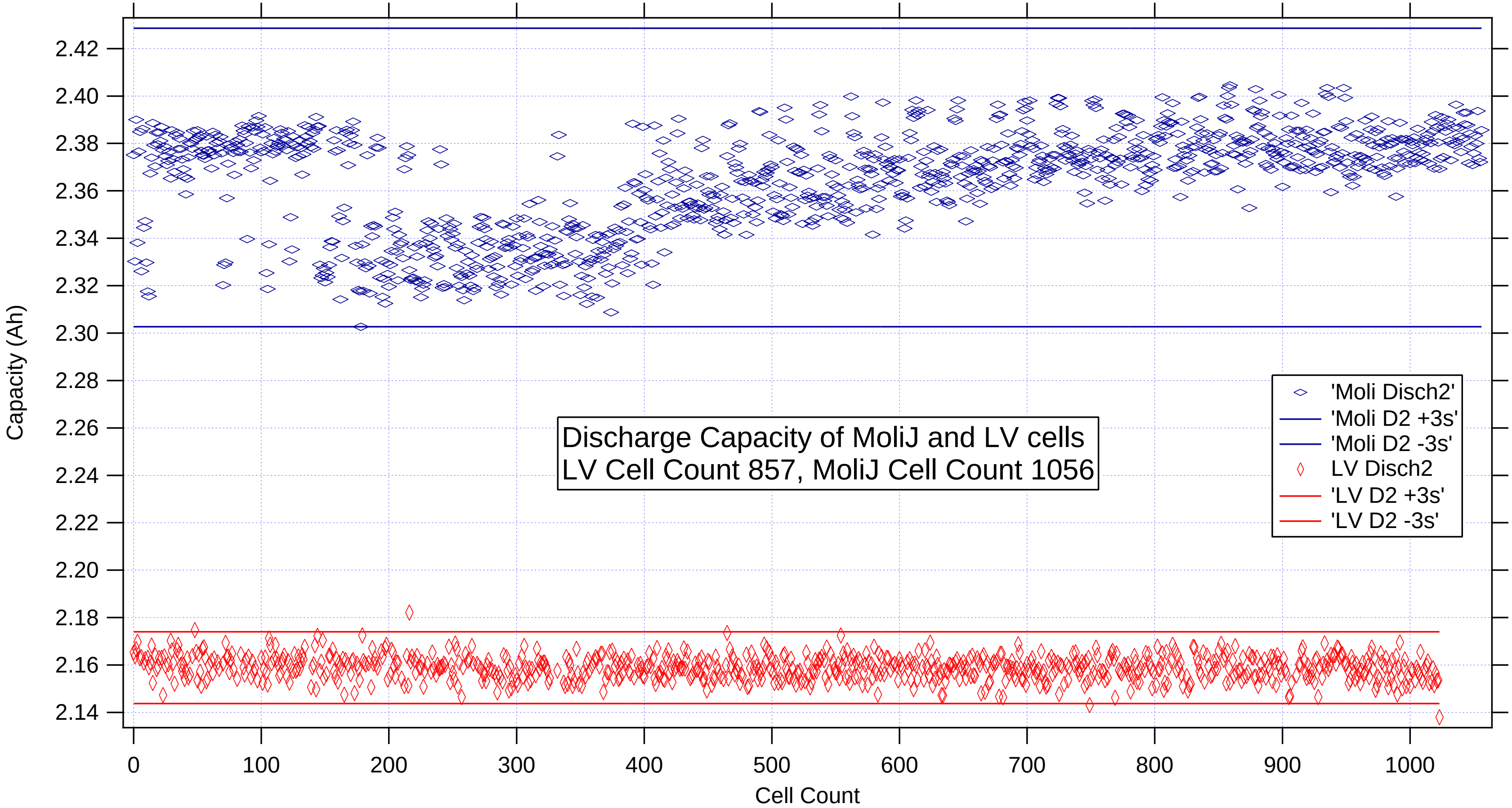


Both cells stored for > 17 months at incoming SoC prior to test

MoliJ 6σ range is 6.7% of mean (including all rejects)

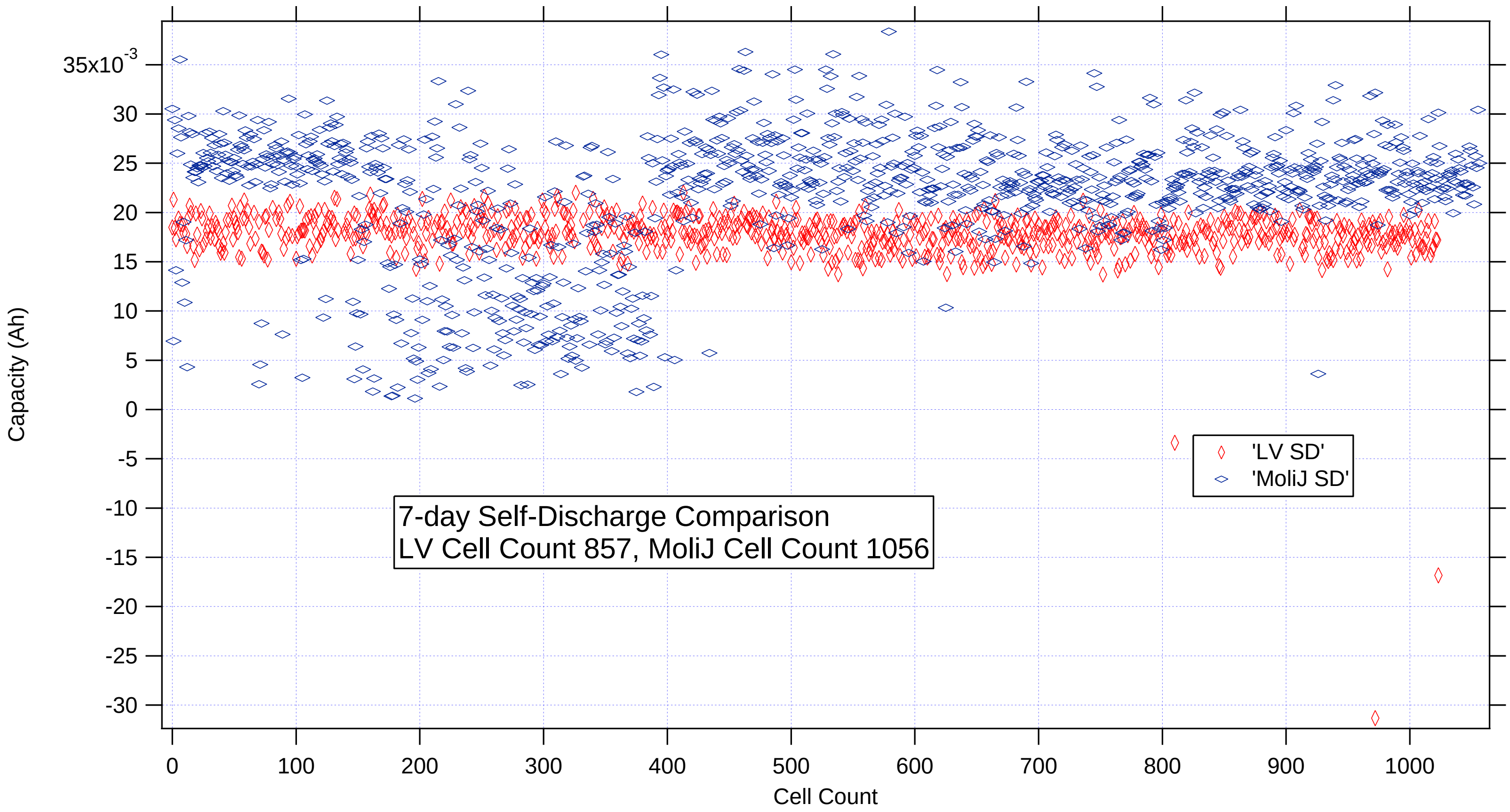
LV 6σ range is 2.3% of mean (excluding 26 cell outlying cluster)

Cell Discharge Capacity Comparison



MoliJ 6σ range is 5.4% of mean, LV 6σ range is 1.4% of mean

Cell Self-Discharge Comparison



Like MoliJ, no cells rejected, but LV stdev is twice as tight as MoliJ's on a % basis
Mean for MoliJ is 22 mAh (vs 18 mAh for LV)
Stdev for MoliJ is 6.7 mAh (vs 2.7 mAh for LV), Stdev for MoliJ is 31% of mean (vs 15% for LV)

Findings so far after ~1000 cell/lot

- Mass – Found over 11 LV rejects, none for MoliJ
  - Stdev for both are nearly equal % of avg (0.22%) however, with more scrubbing of 6σ LV outliers, that should change
- OCV – Found all sorts of strange (hi, lo) LV rejects
  - MoliJ rejects are all marginal low outliers
  - MoliJ stdev is 0.031% of mean with 1 scrub of outliers removed
  - LV stdev is 0.012% of mean with 3 scrubs of outliers removed
- Charge Input – LV uniformity is over twice better than MoliJ
  - MoliJ stdev is 6.7 mAh (0.55%) with all conforming cells
  - LV stdev is 5.6 mAh (0.38%) with more scrubbing of outliers due
- Discharge2 – LV uniformity is over 3 times better than MoliJ
  - MoliJ stdev is 21 mAh (0.9%)
  - LV stdev is 5 mAh (0.23%)
- Self-Discharge – LV uniformity is about twice that of MoliJ
  - MoliJ stdev is 31% of mean
  - LV stdev is 15% of mean

Summary & Conclusions

- Charger design that is 2-fault tolerant to catastrophic has been achieved for the Spacesuit Li-ion Battery with key features
  - Power supply control circuit and 2 microprocessors independently control against overcharge
  - 3 microprocessor control against undercharge (false positive: Go for EVA) conditions
  - 2 independent channels provide functional redundancy
  - Capable of charge balancing cell banks in series,
- Cell manufacturing and performance uniformity is excellent with both designs
  - Once a few outliers are removed, LV cells are slightly more uniform than MoliJ cells
  - If cell balance feature of charger is ever invoked, it will be an indication of a significant degradation issue, not a nominal condition

Acknowledgements

- Electrovaya (Mississauga, CA) for designing and manufacturing the charger
- Cell bank prototypes built and tested by SRI, Arab, AL
- Cell acceptance performed by ABSL teams in Longmont, CO and in Abingdon, UK