Digital Receiver Phase Meter

A commercial digital receiver is modified into a two-channel phase meter.

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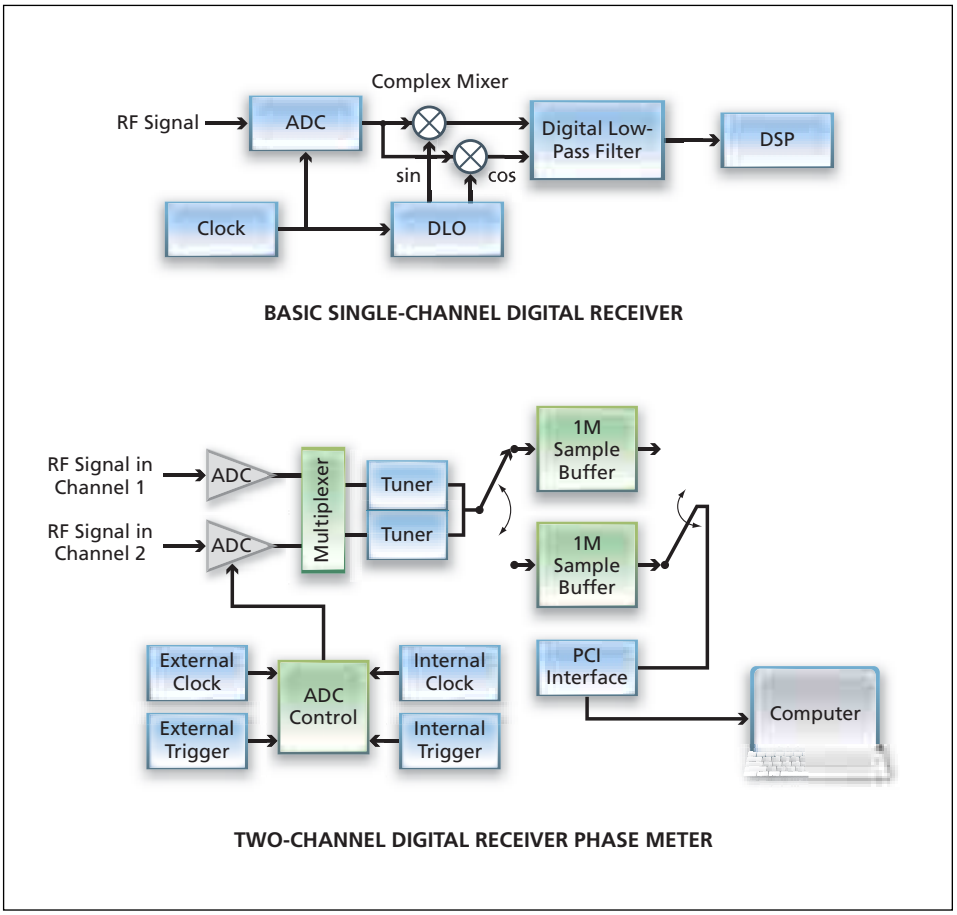
The software of a commercially available digital radio receiver has been modified to make the receiver function as a two-channel low-noise phase meter. This phase meter is a prototype in the continuing development of a phase meter for a system in which radio-frequency (RF) signals in the two channels would be outputs of a spaceborne heterodyne laser interferometer for detecting gravitational waves. The frequencies of the signals could include a common Doppler-shift component of as much as 15 MHz. The phase meter is required to measure the relative phases of the signals in the two channels at a sampling rate of 10 Hz at a root power spectral density <5 microcycle/$(\mathrm{Hz})^{1/2}$ and to be capable of determining the power spectral density of the phase difference over the frequency range from 1 mHz to 1 Hz. Such a phase meter could also be used on Earth to perform similar measurements in laser metrology of moving bodies.



These **Block Diagrams** depict the principles of operation of (1) a basic single-channel digital receiver and (2) the present two-channel digital phase meter, which utilizes the original hardware and modified software of a commercial two-channel digital receiver.

To illustrate part of the principle of operation of the phase meter, the figure includes a simplified block diagram of a basic single-channel digital receiver. The input RF signal is first fed to the input terminal of an analog-to-digital converter (ADC). To prevent aliasing errors in the ADC, the sampling rate must be at least twice the input signal frequency. The sampling rate of the ADC is governed by a sampling clock, which also drives a digital local oscillator (DLO), which is a direct digital frequency synthesizer. The DLO produces samples of sine and cosine signals at a programmed tuning frequency. The sine and cosine samples are mixed with (that is, multiplied by) the samples from the ADC, then low-pass filtered to obtain in-phase (I) and quadrature (Q) signal components. A digital signal processor (DSP) computes the ratio between the Q and I components, computes the phase of the RF signal (relative to that of the DLO signal) as the arctangent of this ratio, and then averages successive such phase values over a time interval specified by the user.

The specific commercially available two-channel digital receiver includes a dual-channel, 65-MHz, 14-bit peripheral component interface (PCI) bus data-acquisition card with a daughter board that contains a pair of narrow-band tuner integrated-circuit chips. The input stage of the card consists of two ADCs. In the tuner chips, input signals having frequencies up to 35 MHz can be translated to zero frequency, then digitally low-pass filtered to a bandwidth between 1 kHz and 1 MHz. The output samples of the tuner chips are fed to a two-part swap buffer. When each half of the swap buffer becomes filled up to a limit (e.g., 1M sample) specified by the user, the contents of the buffer are transferred, via PCI interface, to an external computer for further analysis.

The factory-supplied receiver software includes basic driver components and provides many options to control tuning frequencies, sampling rates, and other operational parameters. The phase-meter version of the software incorporates many of the basic driver components, but a significant effort was made in modifying other parts of the software to make the receiver function as a dedicated two-channel phase meter. In essence, the net effect of the modification is to cause the external computer to calculate differences between the phases in each successive pair of buffered samples from tuner chips and calculate the average phase difference over the time interval represented by the buffer contents.

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