TOWARD A III-V MULTIJUNCTION SPACE CELL TECHNOLOGY ON SI

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INTRODUCTION

High efficiency compound semiconductor solar cells grown on Si substrates are of growing interest in the photovoltaics community for both terrestrial and space applications. As a potential substrate for III-V compound photovoltaics, Si has many advantages over traditional Ge and GaAs substrates that include higher thermal conductivity, lower weight, lower material costs, and the potential to leverage the extensive manufacturing base of the Si industry. Such a technology that would retain high solar conversion efficiency at reduced weight and cost would result in space solar cells that simultaneously possess high specific power (W/kg) and high power density (W/m^2). For terrestrial solar cells this would result in high efficiency III-V concentrators with improved thermal conductivity, reduced cost, and via the use of SiGe graded interlayers as active component layers the possibility of integrating low bandgap sub-cells that could provide for extremely high conversion efficiency.[1] In addition to photovoltaics, there has been an historical interest in III-V/Si integration to provide optical interconnects in Si electronics, which has become of even greater relevance recently due to impending bottlenecks in CMOS based circuitry. As a result, numerous strategies to integrate GaAs with Si have been explored with the primary issue being the ~ 4% lattice mismatch between GaAs and Si.[2,3,4] Among these efforts, relaxed, compositionally-graded SiGe buffer layers where the substrate lattice constant is effectively tuned from Si to that of Ge so that a close lattice match to subsequent GaAs overlayers have shown great promise. With this approach, threading dislocation densities (TDDs) of ~ 1 x 10^6 cm^{-2} have been uniformly achieved in relaxed Ge layers on Si,[5] leading to GaAs on Si with minority carrier lifetimes greater than 10 ns,[6] GaAs single junction solar cells on Si with efficiencies greater than 18%,[7] InGaAs CW laser diodes on Si,[8] and room temperature GaInP red laser diodes on Si.[9] Here we report on the first high performance dual junction GaInP/GaAs solar cells grown on Si using this promising SiGe engineered substrate approach.

EXPERIMENTAL

Compositionally step-graded SiGe buffers were grown by ultra-high vacuum chemical vapor deposition (UHV-CVD) on Si substrates to a final composition of 100% Ge at an average grading rate of 10% Ge μm^{-1}. The grade is interrupted at the 50% Ge layer to perform a critical chemical mechanical polishing (CMP) step to remove the deepest "crosshatch" features that cause dislocation pinning and pileup formation,[5] and thus promote efficient dislocation glide without unnecessary nucleation of new dislocations. For the substrates used here, etch pit density (EPD) measurements revealed TDD values of 1.8 $\pm$ 0.2 $\times$ 10^6 cm^{-2} in the relaxed Ge top layer. Subsequently grown GaAs layers displayed identical TDD values, suggesting negligible TD nucleation due to growth of GaAs on the SiGe / Si substrates. Prior work has shown that the minority carrier lifetime of overgrown

GaAs ranges from 7.7 ns – 10.5 ns for TDD values from 2 to 1×10^6 cm^{-2}, respectively.[6] Both the SiGe and the control GaAs substrates used here were of (100) orientation, with each having a 6° offcut toward the {111} plane to eliminate potential anti-phase domain formation during III-V overgrowth.

All III-V layers were grown using solid source molecular beam epitaxy (MBE). Prior to the growth of device layers a combination of migration enhanced epitaxy (MEE) and annealing was used to create anti-phase domain (APD) - free material and minimize interdiffusion at the GaAs / Ge interface. More detailed description of the initiation conditions and APD-elimination can be found elsewhere.[10] Identical dual junction (DJ) $Ga_{0.51}In_{0.49}P$/GaAs solar cells of p+/n polarity, shown in Fig. 1, were subsequently grown on both SiGe and control GaAs substrates using conventional growth conditions. The p+n polarity was chosen based on earlier results showing it to be much less susceptible to TDD-related carrier lifetime reduction and depletion region recombination issues than n+/p cells.[11] All arsenic containing layers were grown at 615°C, with the exception of the GaAs tunnel junction (TJ) and cap layers grown at 550°C, while phosphorus containing layers were grown at 490°C. Growth rates were 1.0 μm/hr and 1.15 μm/hr for the GaAs and GaInP layers, respectively. The cross-sectional transmission electron microscope (X-TEM) image of a representative DJ cell grown on SiGe, seen in Fig 2, indicates the high structural quality obtained and abrupt interface control of the individual layers.

Since little has been reported regarding MBE growth and optimization of p+/n GaInP cells, much work went into its design. An $(Al_{0.7}Ga_{0.3})_{0.53}In_{0.47}P$ window layer, with a measured bandgap of 2.3 eV, was chosen in place of the AlInP window typical for n+/p cells, since it is difficult to obtain low resistivity p-type AlInP by MBE. The reduction in bandgap decreases the maximum short circuit current density (J_{SC}) obtainable for the top cell, however, separate evaluations of single junction GaInP test cells with either window reveal improved fill factor (FF) and efficiency (η) with $(Al_{0.7}Ga_{0.3})_{0.53}In_{0.47}P$. While work is ongoing to achieve low resistivity p-AlInP by MBE, the $(Al_{0.7}Ga_{0.3})_{0.53}In_{0.47}P$ window was chosen for this study.

The back surface field (BSF), which has a significant affect on operating voltage, was also modified from what has been reported for typical GaInP cells. For n+/p designs, dual layer p+ GaInP/p+ AlInP BSF layers are reported to be superior to either GaInP or AlInP single layer BSFs.[12] For the p+/n InGaP structure, we found a single layer $(Al_{0.7}Ga_{0.3})_{0.53}In_{0.47}P$ BSF to result in 5% higher J_{SC}, with no loss in voltage, compared to devices with a dual-layer BSF using identical base designs. This finding was also supported by quantum efficiency measurements showing improved long wavelength collection using the n-$(Al_{0.7}Ga_{0.3})_{0.53}In_{0.47}P$ BSF. Note that since we are using MBE, the ordered/disordered GaInP BSF structure common to metalorganic chemical vapor deposition was not available.[13] It should be mentioned at this point that all GaInP layers reported here were found to have a 300 K bandgap energy of 1.90 eV as measured by photoluminescence, consistent with the expected bandgap for disordered GaInP.

After growth, the wafers were processed into 4.4 mm^2 solar cells using conventional wet etching and photolithography. The front contact grid area was 10% of the total surface. A MgF_2 / ZnS / MgF_2 anti-reflection coating (ARC) was deposited after fabrication, decreasing average reflection to just below 10 % in the range of 400 to 900 nm. Other reports show average reflectivity of less than 2 % in this range,[12] so improvement in performance could be attained through optimization of the ARC design that is external to the core device.

RESULTS AND DISCUSSION

AM0 and AM1.5G lighted current voltage (LIV) and external quantum efficiency measurements (EQE) were made on tandem cells grown on SiGe and on GaAs substrates at standardized test facilities. Total area efficiencies of 15.3 % and 18.6 % for AM0 conditions and 16.8% and 20.0% for AM1.5G conditions were obtained for the cells grown on SiGe and GaAs, respectively. The LIV data for both spectra are shown in Fig. 3. The results for the cells grown on GaAs, shown in Table 1, are comparable to other reports of MBE grown DJ cells that used GaAs TJ's,[14] considering our high metal coverage and inefficient ARC.

Integration of the EQE data to obtain AM0 J_{SC} values for the cells on GaAs substrates reveals a close current match under AM0 conditions using the present top cell thickness. The total current of the tandem cells meets the target current of the single junction GaInP cells for which the DJ cells were designed, indicating good current collection. However, it can be expected that for AM1.5G illumination, the current would be somewhat limited by the upper cell due to the different spectral content. The efficiency reached under AM1.5G conditions could likely be increased through use of a slightly thicker top cell.

The high V_{OC} of 2.2 V, which is within 150 mV (~95%) of the control device Voc on GaAs, is attributed to the low TDD maintained throughout the entire DJ structure grown on SiGe/Si, and is indicative of low carrier recombination rates throughout the bulk and interface regions of the DJ cell. Separate measurements of GaAs and GaInP single junction cells grown on identical SiGe substrates display individual V_{OC} values of 0.95 and 1.28 V respectively, the sum of which closely matches the Voc output of the DJ cell, suggesting minimal voltage loss due to the thin interconnecting TJ in spite of growth on the crosshatched SiGe surface. This also indicates that the sub-cells did not suffer from the more complex DJ growth process compared to the simpler single junction cell growths. Further, filtered light I-V measurements made on the DJ/Si cell through a 1.24 eV low pass filter confirmed that no photovoltage was emanating from the GaAs/Ge interface region on the SiGe substrates, verifying that the high Voc is due to only the additive effects of the GaInP and GaAs subcells as desired and electrical control of the GaAs/Ge heterovalent interface was maintained.

CONCLUSION

The measured Voc value closely matches that expected for an InGaP/GaAs DJ cell with a TDD of 1.8 x 10^6 cm^{-2} using simple models, and thus as TDD continues to reduce with advances in the SiGe graded buffer, Voc and cell performance will continue to increase since other mismatch-related defects are not a primary factor in limiting cell performance via our approach, until the carrier lifetimes in each sub-cell reach a plateau at a TDD in the range of 10^5 to 10^6 cm^{-2}.[2] Since recent work has already shown that TDD of relaxed Ge layers on SiGe/Si has reached ~ 6-8 x 10^5 cm^{-2}, further improvements are expected.[15] However, the cells reported here can already benefit significantly when taking into account the limitation on light absorption and current output imposed by the high grid obscuration and reflectance in our prototype cells. Improvements in the metal coverage and reflection to more typical values, plus the use of a wide bandgap tunnel junction instead of the GaAs tunnel junction used here, all will substantially increase current response and thus overall efficiency. These results show the great potential of metamorphic SiGe buffers to enable a monolithically integrated multi-junction III-V cell technology on Si.

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p++ GaAs contact layer (1000 Å)	~1x10^{19}
p+ $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ window (300 Å)	~2 x10^{18}
p+ $In_{0.49}Ga_{0.51}P$ emitter (500 Å)	~2 x10^{18}
n $In_{0.49}Ga_{0.51}P$ base (5500 Å)	~7 x10^{16}
n+ $In_{0.47}(Al_{0.7}Ga_{0.3})_{0.53}P$ back surface field (300 Å)	~2 x10^{18}
n++ GaAs TJ (250 Å)	~2 x10^{19}
p++ GaAs TJ (250 Å)	~2 x10^{19}
p+ $In_{0.49}Ga_{0.51}$ window (400 Å)	~3 x10^{18}
p+ GaAs emitter (5000 Å)	~2 x10^{18}
n GaAs base (20,500 Å)	~2 x10^{17}
n+ $Al_{0.7}Ga_{0.3}As$ back surface field (1000 Å)	~2 x10^{18}
n+ GaAs buffer (2000 Å)	~2 x10^{18}
Ge (300Å)	uid
n+ SiGe substrate	~1 x10^{18}

Fig 1. Schematic illustration of the GaInP/GaAs p/n DJ solar cell structure shown on SiGe. This structure was used for both AM0 and AM1.5G LIV measurements.

	GaAs		SiGe	
	AM0	AM1.5G	AM0	AM1.5G
Jsc (mA/cm²)	13.08	10.9	12.66	10.48
Voc (V)	2.34	2.32	2.21	2.18
FF (%)	82.5	79.0	75.0	73.3
η (%)	18.6	20.0	15.3	16.8
η_a (%)	20.6	22.2	17.0	18.6

Table 1. LIV characteristics of GaInP/GaAs cells on GaAs and Si substrates under AM0 and AM1.5G spectra, including total area efficiency (η) and active area efficiency (η_a).

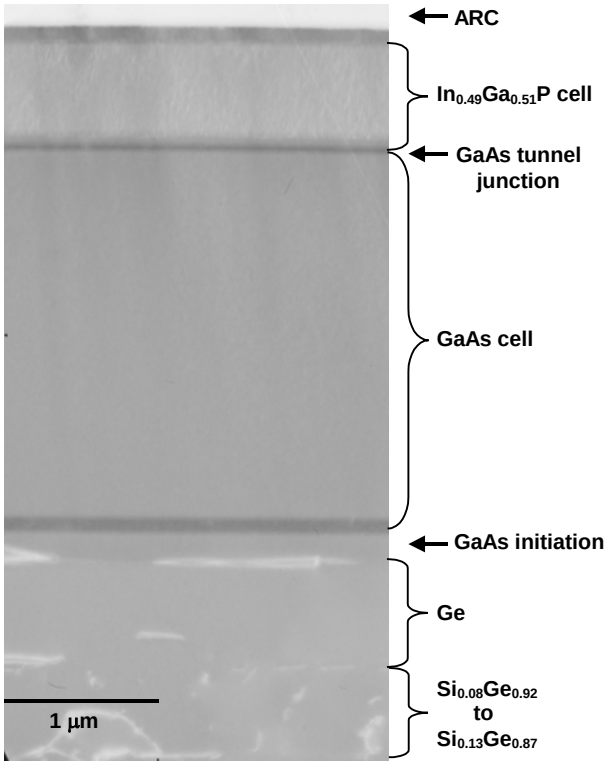

Fig 2. Cross sectional transmission electron microscopy image of the GaInP/GaAs DJ as grown on a SiGe/Si substrate. Higher resolution images of the GaAs/Ge interface show no evidence for APD nucleation.

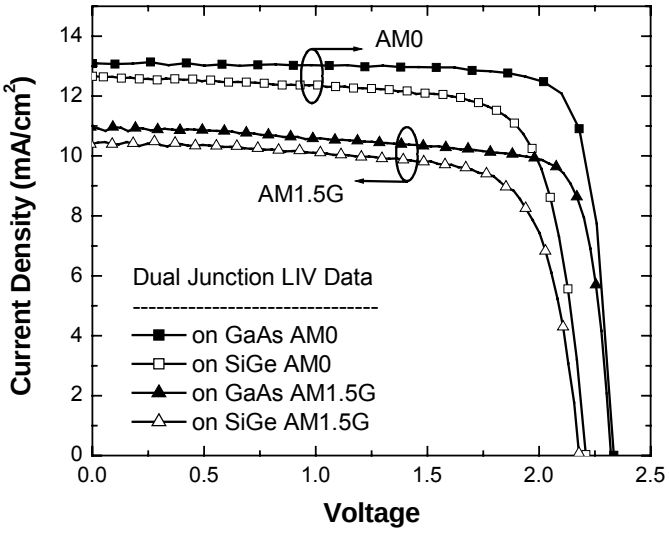

Fig 3. Current-voltage measurements under AM0 and AM1.5G illumination of GaInP/GaAs DJ solar cells on GaAs and SiGe substrates. These measurements were done at NASA Glenn Research Center (AM0) and NREL (AM1.5G).

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