Simulation of SRAM SEU Sensitivity at Reduced Operating Temperatures

S. Sanathanamurthy, V. Ramachandran, M. L. Alles, R. A. Reed, L. W. Massengill, Vanderbilt University; ***A. Raman, M. Turowski,*** CFD Research Corporation; ***A. Mantooth, B. Woods, M. Barlow,*** University of Arkansas; ***K. Moen, M. Bellini, A. Sutton and J. D. Cressler,*** Georgia Institute of Technology

Abstract: *A new NanoTCAD-to-Spectre interface is applied to perform mixed-mode SEU simulations of an SRAM cell. Results using newly calibrated TCAD cold temperature substrate mobility models, and BSIM3 compact models extracted explicitly for the cold temperature designs, indicate a 33% reduction in SEU threshold for the range of temperatures simulated.*

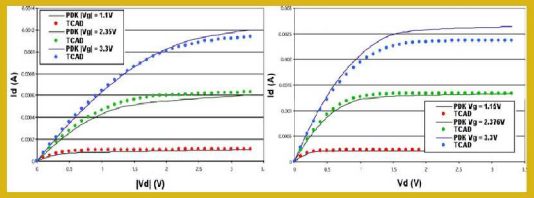
Motivation

- Limited available analyses indicate that single event response may be exacerbated by cold temperature[1-3]
- Desire to understand worst case SEU threshold of CMOS SRAM in mixed signal system designed using IBM 5AM SiGe BiCMOS[4] to know if higher level mitigation is sufficient approach

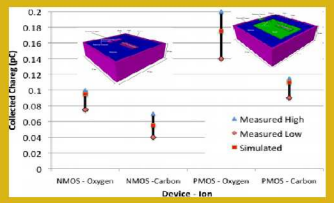
Methodology

- Calibrate 3D NanoTCAD model vs:

PDK/Spectre-generated IV curves



Charge collection measured on transistors[5]

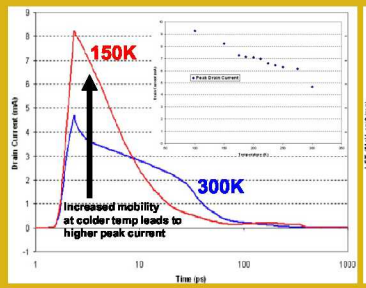


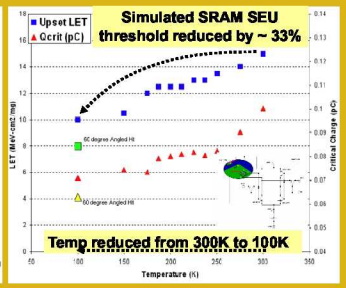
- Simulate the temperature dependence of SEU thresholds of SRAM cell using mixed-mode using:
  - A new NanoTCAD-to-Spectre interface
  - BSIM3 models extracted explicitly for the cold temp design
  - Newly calibrated TCAD cold temp substrate mobility models
    - Lombardi model[7] for MOSFETs with modifications to how internal values are calculated at low temperatures, based on the models in Selberherr[8].
    - Altermatt model[9,10] for incomplete ionization, that internally calls newer effective mass and bandgap model[11].

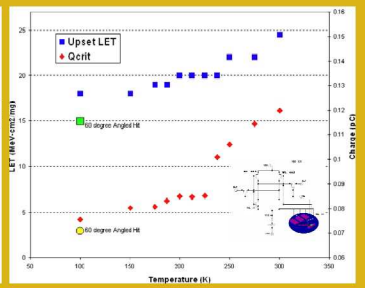
This work has been supported by DTRA SBIR Phase II, Contract No: HDTRA1-07-C-0037, subcontract to VU; and NASA ETDP: Radiation Hardened Electronics for Space Environments (RHESE), SiGe Integrated Electronics For Extreme Environments, Contract # NNL06AA29C. Charge collection data measurements supported by NASA GFSC.

Findings

- Peak SE-induced current increases with decreasing temperature
- Simulations indicate ~ 33% reduction in upset threshold for the range of temperatures simulated.
- The simulated minimum threshold, even for an angled (60°) strike, is well above the threshold for direct ionization by protons (equivalent to LET ~ 0.5 MeV-cm^2/mg).







Conclusions

- Use of common higher-level mitigation techniques for SEU is sufficient in this technology and design; no cell level hardening required
- Temperature should be considered when possible and appropriate in testing and analyses of single event effects[6]
- Capability to couple TCAD to Spectre allows mixed mode simulations using vendor supplied PDK compact models directly

[1] M. L. Alles et al., "Implications of Cold Temperature Environments for Single Event Radiation Effects", *GOMAC Proceedings*, March 2007.
[2] A. Sutton et al., "Proton-Induced SEU in SiGe Digital Logic at Cryogenic Temperatures", *Solid State Electronics*, vol. 52, no. 10, pp. 1652-59, Oct 2008, in press.
[3] D. Truyen et al., "Temperature Effect on Heavy-Ion Induced Parasitic Current on SRAM by Device Simulation: Effect on SEU Sensitivity," *IEEE Trans. Nucl. Sci.*, 54, 4, pp. 1025-1029, August 2007.
[4] http://www.mosis.com/ibm/5am/
[5] Private communications, unpublished data, J. A. Pellish, G. Vizkelethy, P. Marshall.
[6] V. Ramachandran et al., "In-situ Cryogenic SEE Testing of High-Speed SiGe BiCMOS Devices," *6th International Planetary Probe Workshop*, June 2008, Atlanta, Georgia, USA.
[7] Claudio Lombardi, et al, *IEEE TCAD*, Vol. 7, No. 11, Nov. 1988, pp. 1164-1171.
[8] Siegfried Selberherr, *IEEE Trans. Elec. Dev.*, Vol. 36, No. 8, Aug 1989, pp. 1464-1474.
[9] P.P. Altermatt, et al, *J. Appl. Phys.*, Vol. 100, 2006, pp. 113714-1 to 113714-10.
[10] P.P. Altermatt, et al, *J. Appl. Phys.*, Vol. 100, 2006, pp. 113715-1 to 113714-7.
[11] Martin A. Green, *J. Appl. Phys.*, Vol. 67, No. 6, 15 March 1990, pp. 2944-2954.