

Figure. 2. A schematic diagram of the **One Half of the Split-Block** for the broadband 1.5 THz dual-polarized, sideband-separating, balanced receiver shows the finline OMT, two first-stage and four second-stage quadrature hybrids, and the in-phase LO power splitter that will be fabricated using DRIE silicon etching process.

because of the smallness of their features and the tightness of their tolerances, quadrature hybrids and finline OMTs for terahertz frequencies cannot

be fabricated by conventional machining. However, recent advances in both electromagnetic-field-simulating software and microfabrication techniques

have made it possible to design and construct complexly shaped waveguide structures. The development of the proposed receiver is planned to include the use of a combination of optical lithography and a micro-machining process based on deep reactive ion etching (DRIE) of silicon. This combination is expected to enable the realization of micron-size waveguide features and sub-micron tolerances in fabricating the aforementioned critical components.

*This work was done by Goutam Chattopadhyay, John Ward, Harish Manohara, and Peter Siegel of Caltech for NASA's Jet Propulsion Laboratory.*

*In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:*

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*Refer to NPO-42935, volume and number of this NASA Tech Briefs issue, and the page number.*

## Modular Battery Charge Controller

**Distributed charge control and a masterless communication bus enhance this controller's robustness for use in battery energy-storage applications.**

*John H. Glenn Research Center, Cleveland, Ohio*

A new approach to masterless, distributed, digital-charge control for batteries requiring charge control has been developed and implemented. This approach is required in battery chemistries that need cell-level charge control for safety and is characterized by the use of one controller per cell, resulting in redundant sensors for critical components, such as voltage, temperature, and current. The charge controllers in a given battery interact in a masterless fashion for the purpose of cell balancing, charge control, and state-of-charge estimation. This makes the battery system invariably fault-tolerant.

The solution to the single-fault failure, due to the use of a single charge controller (CC), was solved by implementing one CC per cell and linking



A prototype of the 28-V, 60-A-h Lithium Ion Battery.

them via an isolated communication bus [e.g., controller area network (CAN)] in a masterless fashion so that

the failure of one or more CCs will not impact the remaining functional CCs. Each microcontroller-based CC digitizes the cell voltage ( $V_{cell}$ ), two cell temperatures, and the voltage across the switch ( $V$ ); the latter variable is used in conjunction with  $V_{cell}$  to estimate the bypass current for a given bypass resistor. Furthermore, CC1 digitizes the battery current ( $I_1$ ) and battery voltage ( $V_{batt}$ ) and CC5 digitizes a second battery current ( $I_2$ ). As a result, redundant readings are taken for temperature, battery current, and battery voltage through the summation of the individual cell voltages given that each CC knows the voltage of the other cells.

For the purpose of cell balancing, each CC periodically and independently transmits its cell voltage and stores the

received cell voltage of the other cells in an array. The position in the array depends on the identifier (ID) of the transmitting CC. After eight cell voltage receptions, the array is checked to see if one or more cells did not transmit. If one or more transmissions are missing, the missing cell(s) is (are) eliminated from cell-balancing calculations.

The cell-balancing algorithm is based on the error between the cell's voltage and the other cells and is categorized into four zones of operation. The algorithm is executed every sec-

ond and, if cell balancing is activated, the error variable is set to a negative low value. The largest error between the cell and the other cells is found and the zone of operation determined. If the error is zero or negative, then the cell is at the lowest voltage and no balancing action is needed. If the error is less than a predetermined negative value, a Cell Bad Flag is set. If the error is positive, then cell balancing is needed, but a hysteric zone is added to prevent the bypass circuit from triggering repeatedly near zero error. This

approach keeps the cells within a predetermined voltage range.

*This work was done by Robert Button of Glenn Research Center and Marcelo Gonzalez of Cleveland State University. Further information is contained in a TSP (see page 1).*

*Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18296-1.*

## Efficient Multiplexer FPGA Block Structures Based on G<sup>4</sup>FETs

**Fewer G<sup>4</sup>FETs than conventional transistors would be needed to implement multiplexers.**

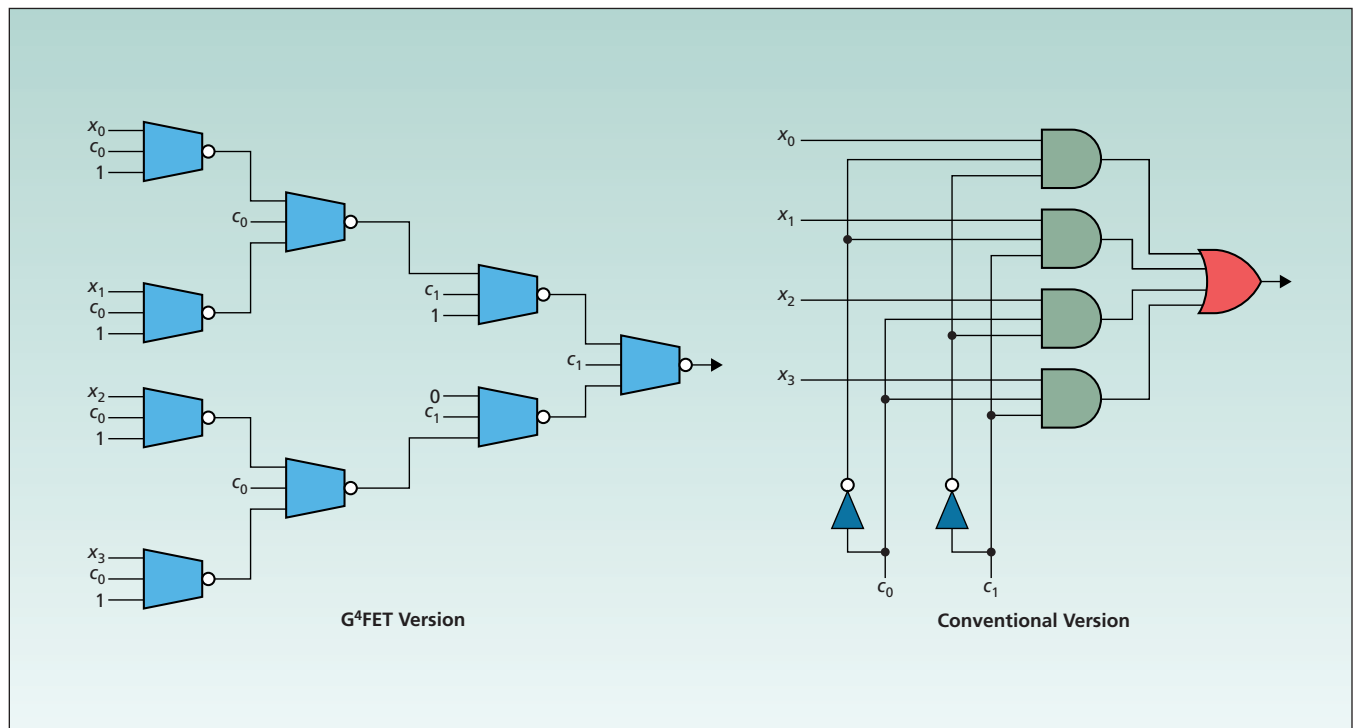
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Generic structures have been conceived for multiplexer blocks to be implemented in field-programmable gate arrays (FPGAs) based on four-gate field-effect transistors (G<sup>4</sup>FETs). This concept is a contribution to the continuing development of digital logic circuits based on G<sup>4</sup>FETs and serves as a further demonstration that logic circuits based on G<sup>4</sup>FETs could be more efficient (in the sense that they could contain fewer transistors), relative to functionally

equivalent logic circuits based on conventional transistors.

Results in this line of development at earlier stages were summarized in two previous *NASA Tech Briefs* articles: "G<sup>4</sup>FETs as Universal and Programmable Logic Gates" (NPO-41698), Vol. 31, No. 7 (July 2007), page 44, and "Efficient G<sup>4</sup>FET-Based Logic Circuits" (NPO-44407), Vol. 32, No. 1 (January 2008), page 38. As described in the first-mentioned previous article, a

G<sup>4</sup>FET can be made to function as a three-input NOT-majority gate, which has been shown to be a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer components than are required for conventional transistor-based circuits performing the same logic functions. The second-mentioned previous article reported results of a comparative study of NOT-majority-gate



A **Four-to-One Multiplexer** is a special case of a  $2^n$ -to-1 multiplexer, which can perform a variety of logic functions on  $2^n$  binary data inputs ( $x_0, \dots, x_{2^n-1}$ ), and  $n$  control (selection) inputs ( $c_0, \dots, c_{n-1}$ ). In this case,  $n = 2$ . The combination of the control inputs can be interpreted as a binary integer,  $c$ , in the range of 0 to  $2^n - 1$ .