(G^4FET)-based logic-circuit designs and equivalent NOR- and NAND-gate-based designs utilizing conventional transistors. [NOT gates (inverters) were also included, as needed, in both the G^4FET- and the NOR- and NAND-based designs.] In most of the cases studied, fewer logic gates (and, hence, fewer transistors), were required in the G^4FET-based designs.

There are two popular categories of FPGA block structures or architectures: one based on multiplexers, the other based on lookup tables. In standard multiplexer-based architectures, the basic building block is a treelike configuration of multiplexers, with possibly a few additional logic gates such as ANDs or ORs. Interconnections are realized by means of programmable switches that may connect the input terminals of a block to output terminals of other blocks, may bridge together some of the inputs, or may connect some of the input terminals to signal sources representing constant logical levels 0 or 1.

The left part of the figure depicts a four-to-one G^4FET-based multiplexer tree; the right part of the figure depicts a functionally equivalent four-to-one multiplexer based on conventional transistors. The G^4FET version would contains 54 transistors; the conventional version contains 70 transistors.

This work was done by Farrokh Vatan and Amir Fijany of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-44735, volume and number of this NASA Tech Briefs *issue, and the page number.*

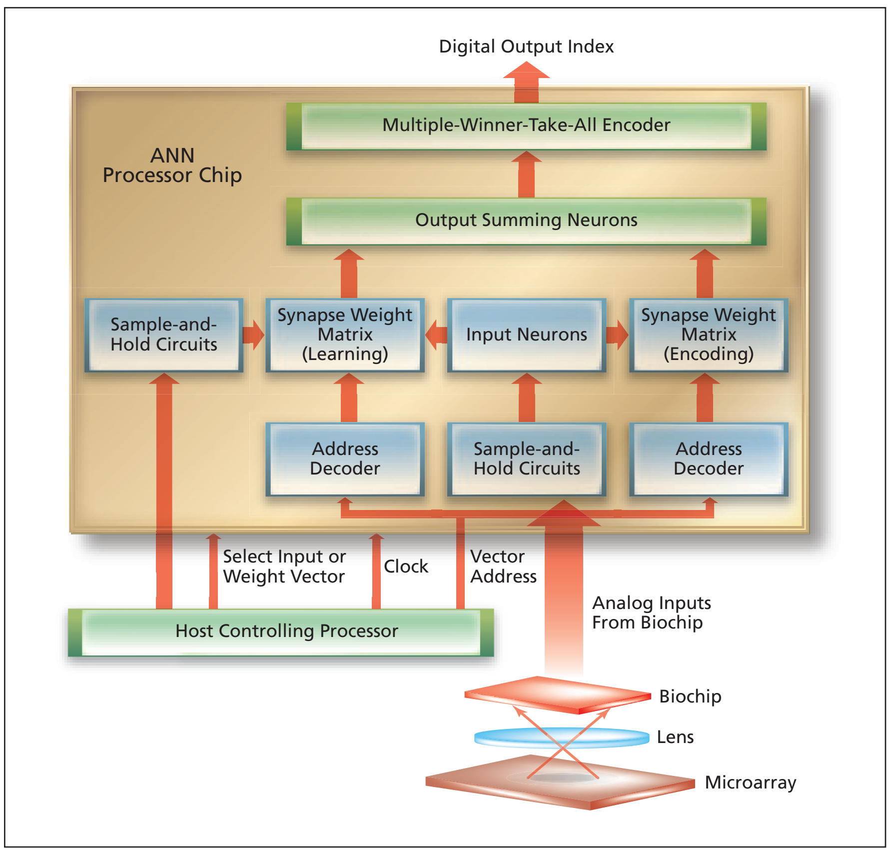
VLSI Microsystem for Rapid Bioinformatic Pattern Recognition

Rapid processing is made possible by a massively parallel neural-computing architecture.

NASA's Jet Propulsion Laboratory, Pasadena, California

A system comprising very-large-scale integrated (VLSI) circuits is being developed as a means of bioinformatics-oriented analysis and recognition of patterns of fluorescence generated in a microarray in an advanced, highly miniaturized, portable genetic-expression-assay instrument. Such an instrument implements an on-chip combination of polymerase chain reactions and electrochemical transduction for amplification and detection of deoxyribonucleic acid (DNA).

Commonly, the design of such an instrument provides for a sample and a reference channel, so that it can be used to perform a dual-label assay for identifying differentially expressed genes. A dual-label assay also reduces spurious variability attributable to aspects of spots in the microarray that affect both the sample and the reference specimen similarly. The logarithm of the relative intensities of the two fluorescent-dye-labeled specimens at each spot is calculated and used in analyzing the fluorescence image of the assay. Heretofore, analysis of the fluorescence image has typically involved sequential, pixel-by-pixel processing in a digital computer. Such processing does not enable real-time recognition of genetic patterns of interest — a significant drawback where, for example, it may be desirable or necessary to recognize dangerous microbes in the field. In contrast, a system like the one now being developed enables robust, real-time recognition.



The **Biochip Collects Fluorescence Inputs** from the microarray and feeds them to the ANN processor chip, which strives to recognize a bioinformatic pattern of interest.

The system (see figure) includes a chip, denoted a biochip, that contains VLSI circuitry for collecting the fluorescence inputs and generates analog signals proportional to the logarithms of the fluorescence-intensity ratios for the spots in the microarray. The outputs of the biochip are fed as inputs to another chip that contains a VLSI artificial neural network (ANN), which performs the processing for recognition of bioinformatic patterns of interest. The ANN design provides for a combination of massively parallel neural-computing interconnections and mixed-signal (a combination of analog and digital) circuitry characterized by feature sizes in the deep-submicron range, making it possible to implement the ANN as a single VLSI chip. One notable aspect of the design is the use of a parallel row/column data-flow architecture to connect all on-chip subsystems and eliminate data-flow bottlenecks of the type caused by bandwidth limitations in conventional data buses.

The ANN includes input neurons, programmable-weight synapses, summing and inner product cells, output neurons, and an output multi-winner-take-all encoder. The programmable synapse matrix is composed of $M \times N$ cells for $N \times M$-dimensional code vectors. There are N output summing neurons that execute a sigmoid-logarithmic (in contradistinction to a conventional sigmoid) transfer function. The synaptic weights are generated by an error-back-propagation supervised-learning algorithm executed by an off-chip host controlling processor. The outputs of the output summing neurons are fed to a multi-winner-take-all block that consists of N competitive circuit cells and uses binary codes to encode N classes.

This work was done by Wai-Chi Fang of Caltech and Jaw-Chyng Lue of University of Southern California for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
(818) 354-2240
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-44155, volume and number of this NASA Tech Briefs *issue, and the page number.*

Low-Noise Amplifier for 100 to 180 GHz

Noise temperature is lower than in the prior state of the art.

NASA's Jet Propulsion Laboratory, Pasadena, California

A three-stage monolithic millimeter-wave integrated-circuit (MMIC) amplifier designed to exhibit low noise in operation at frequencies from about 100 to somewhat above 180 GHz has been built and tested. This is a prototype of broadband amplifiers that have potential utility in diverse applications, including measurement of atmospheric temperature and humidity and millimeter-wave imaging for inspecting contents of opaque containers.

Figure 1 depicts the amplifier as it appears before packaging. Figure 2 presents data from measurements of the performance of the amplifier as packaged in a WR-05 waveguide and tested in the frequency range from about 150 to about 190 GHz. The amplifier exhibited substantial gain throughout this frequency range. Especially notable is the fact that at 165 GHz, the noise figure was found to be 3.7 dB, and the noise temperature was found to be 370 K: This is less than half the noise temperature of the prior state of the art.

This work was done by Pekka Kangaslahti, David Pukala, King Man Fung, and Todd Gaier of Caltech and Xiaobing Mei, Richard Lai, and William Deal of Northrop Grumman Corporation for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45178

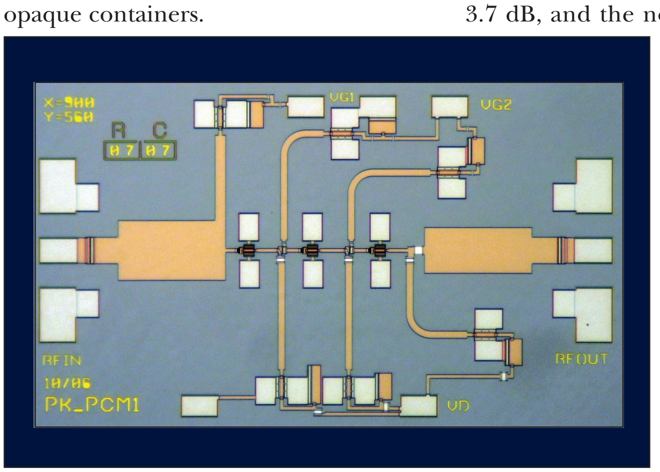


Figure 1. This **MMIC Amplifier** includes InP high-electron-mobility transistors (HEMTs) connected to microstrip transmission lines on a substrate of 2-mil (≈51-µm) thickness. Each HEMT has two fingers and a gate width of 15 µm, for a total gate periphery of 30 µm.

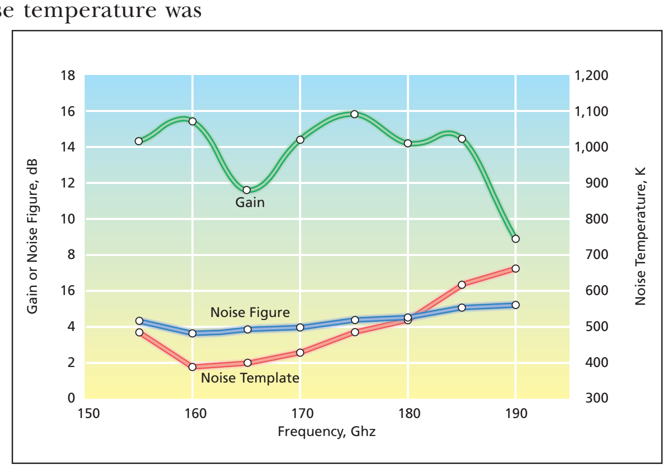


Figure 2. These **Plots of Performance Data** were derived from measurements on the amplifier as packaged in a WR-05 waveguide [a waveguide having a cross section of 0.0510 by 0.0255 in. (about 1.30 by 0.65 mm), nominally for the frequency range of 140 to 220 GHz].