received cell voltage of the other cells in an array. The position in the array depends on the identifier (ID) of the transmitting CC. After eight cell voltage receptions, the array is checked to see if one or more cells did not transmit. If one or more transmissions are missing, the missing cell(s) is (are) eliminated from cell-balancing calculations.

The cell-balancing algorithm is based on the error between the cell's voltage and the other cells and is categorized into four zones of operation. The algorithm is executed every second and, if cell balancing is activated, the error variable is set to a negative low value. The largest error between the cell and the other cells is found and the zone of operation determined. If the error is zero or negative, then the cell is at the lowest voltage and no balancing action is needed. If the error is less than a predetermined negative value, a Cell Bad Flag is set. If the error is positive, then cell balancing is needed, but a hysteretic zone is added to prevent the bypass circuit from triggering repeatedly near zero error. This approach keeps the cells within a predetermined voltage range.

This work was done by Robert Button of Glenn Research Center and Marcelo Gonzalez of Cleveland State University. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18296-1.

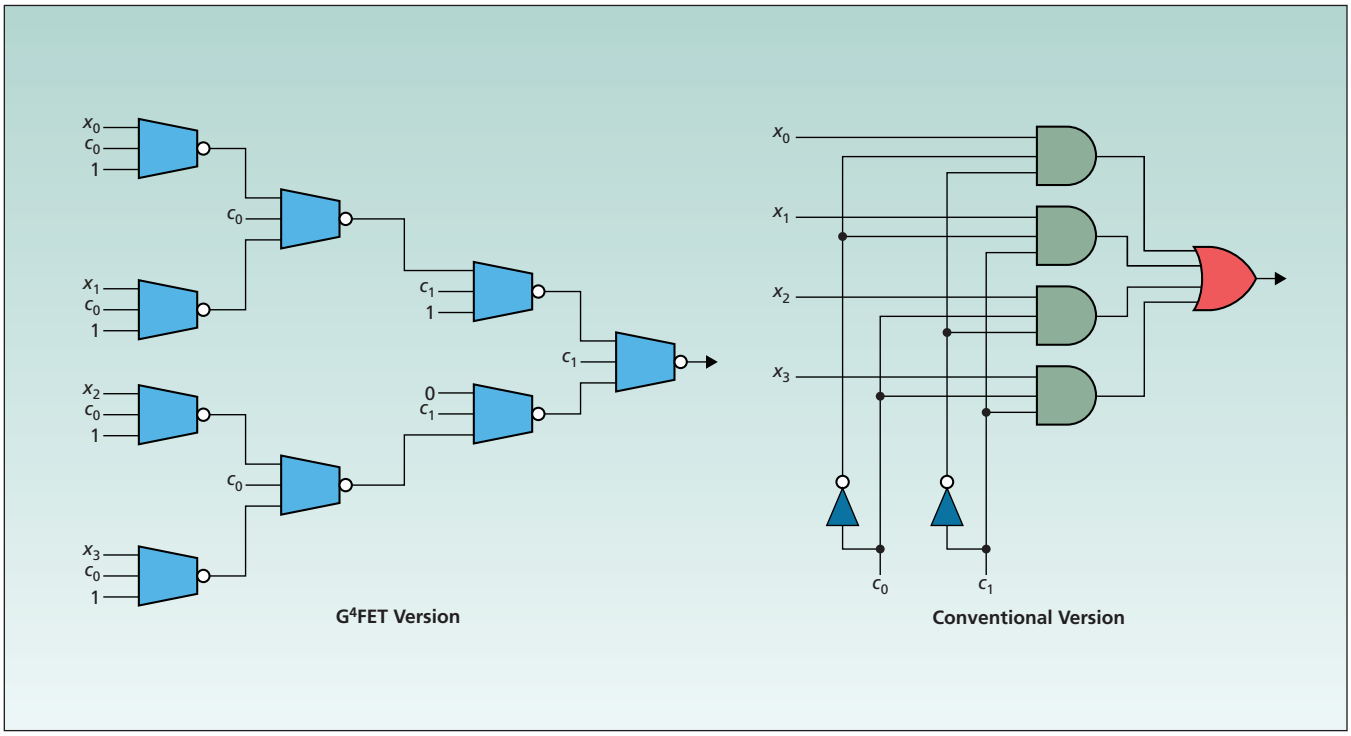
Efficient Multiplexer FPGA Block Structures Based on G^{4}FETs

Fewer G^{4}FETs than conventional transistors would be needed to implement multiplexers.

NASA's Jet Propulsion Laboratory, Pasadena, California

Generic structures have been conceived for multiplexer blocks to be implemented in field-programmable gate arrays (FPGAs) based on four-gate field-effect transistors (G^{4}FETs). This concept is a contribution to the continuing development of digital logic circuits based on G^{4}FETs and serves as a further demonstration that logic circuits based on G^{4}FETs could be more efficient (in the sense that they could contain fewer transistors), relative to functionally equivalent logic circuits based on conventional transistors.

Results in this line of development at earlier stages were summarized in two previous *NASA Tech Briefs* articles: "G^{4}FETs as Universal and Programmable Logic Gates" (NPO-41698), Vol. 31, No. 7 (July 2007), page 44, and "Efficient G^{4}FET-Based Logic Circuits" (NPO-44407), Vol. 32, No. 1 (January 2008), page 38 . As described in the first-mentioned previous article, a G^{4}FET can be made to function as a three-input NOT-majority gate, which has been shown to be a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer components than are required for conventional transistor-based circuits performing the same logic functions. The second-mentioned previous article reported results of a comparative study of NOT-majority-gate



A **Four-to-One Multiplexer** is a special case of a 2^n-to-1 multiplexer, which can perform a variety of logic functions on 2^n binary data inputs ($x_0,...x_{2^n-1}$), and n control (selection) inputs ($c_0,...c_{n-1}$). In this case, n = 2. The combination of the control inputs can be interpreted as a binary integer, c, in the range of 0 to $2^n - 1$.

(G^4FET)-based logic-circuit designs and equivalent NOR- and NAND-gate-based designs utilizing conventional transistors. [NOT gates (inverters) were also included, as needed, in both the G^4FET- and the NOR- and NAND-based designs.] In most of the cases studied, fewer logic gates (and, hence, fewer transistors), were required in the G^4FET-based designs.

There are two popular categories of FPGA block structures or architectures: one based on multiplexers, the other based on lookup tables. In standard multiplexer-based architectures, the basic building block is a treelike configuration of multiplexers, with possibly a few additional logic gates such as ANDs or ORs. Interconnections are realized by means of programmable switches that may connect the input terminals of a block to output terminals of other blocks, may bridge together some of the inputs, or may connect some of the input terminals to signal sources representing constant logical levels 0 or 1.

The left part of the figure depicts a four-to-one G^4FET-based multiplexer tree; the right part of the figure depicts a functionally equivalent four-to-one multiplexer based on conventional transistors. The G^4FET version would contains 54 transistors; the conventional version contains 70 transistors.

This work was done by Farrokh Vatan and Amir Fijany of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-44735, volume and number of this NASA Tech Briefs *issue, and the page number.*

VLSI Microsystem for Rapid Bioinformatic Pattern Recognition

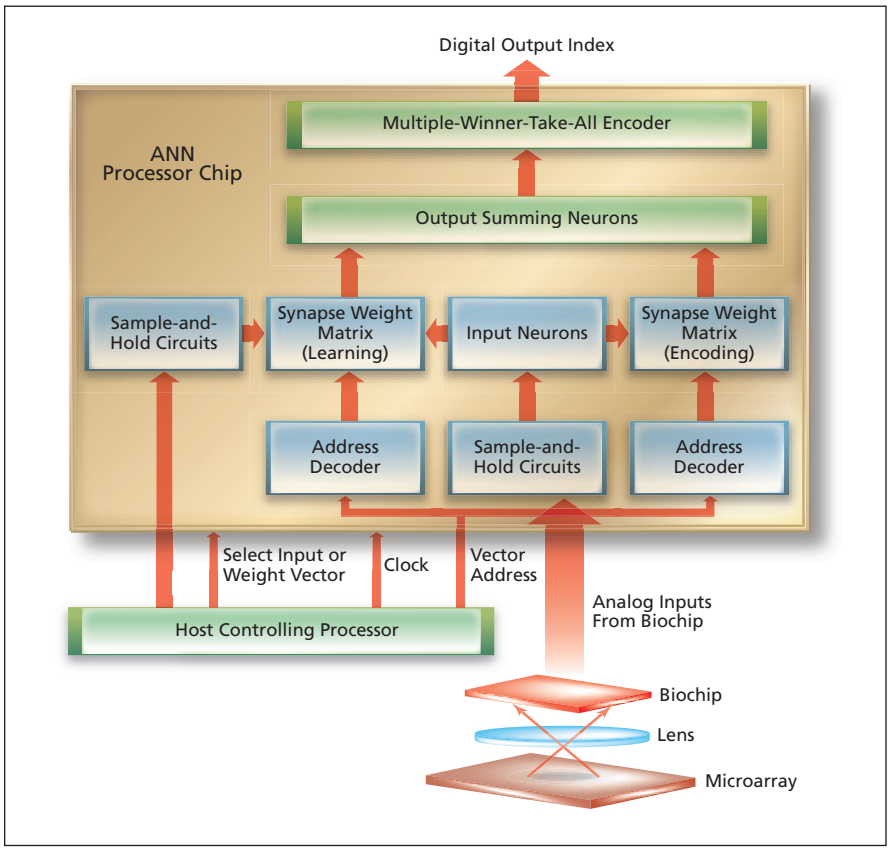
Rapid processing is made possible by a massively parallel neural-computing architecture.

NASA's Jet Propulsion Laboratory, Pasadena, California

A system comprising very-large-scale integrated (VLSI) circuits is being developed as a means of bioinformatics-oriented analysis and recognition of patterns of fluorescence generated in a microarray in an advanced, highly miniaturized, portable genetic-expression-assay instrument. Such an instrument implements an on-chip combination of polymerase chain reactions and electrochemical transduction for amplification and detection of deoxyribonucleic acid (DNA).

Commonly, the design of such an instrument provides for a sample and a reference channel, so that it can be used to perform a dual-label assay for identifying differentially expressed genes. A dual-label assay also reduces spurious variability attributable to aspects of spots in the microarray that affect both the sample and the reference specimen similarly. The logarithm of the relative intensities of the two fluorescent-dye-labeled specimens at each spot is calculated and used in analyzing the fluorescence image of the assay. Heretofore, analysis of the fluorescence image has typically involved sequential, pixel-by-pixel processing in a digital computer. Such processing does not enable real-time recognition of genetic patterns of interest — a significant drawback where, for example, it may be desirable or necessary to recognize dangerous microbes in the field. In contrast, a system like the one now being developed enables robust, real-time recognition.

The system (see figure) includes a chip, denoted a biochip, that contains VLSI circuitry for collecting the fluorescence inputs and generates analog signals proportional to the logarithms of the fluorescence-intensity ratios for the spots in the microarray. The outputs of the biochip are fed as inputs to another chip that contains a VLSI artificial neural network (ANN), which performs the processing for recognition of bioinformatic patterns of interest. The ANN design pro-



The **Biochip Collects Fluorescence Inputs** from the microarray and feeds them to the ANN processor chip, which strives to recognize a bioinformatic pattern of interest.