# ADVANCED DISTRIBUTED MEASUREMENTS AND DATA PROCESSING AT THE VIBRO-ACOUSTIC TEST FACILITY, GRC SPACE POWER FACILITY, SANDUSKY, OHIO—AN ARCHITECTURE AND AN EXAMPLE

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## **ABSTRACT**

A large-scale, distributed, high-speed data acquisition system (HSDAS) is currently being installed at the Space Power Facility (SPF) at NASA Glenn Research Center's Plum Brook Station in Sandusky, OH. This installation is being done as part of a facility construction project to add Vibro-acoustic Test Capabilities (VTC) to the current thermal-vacuum testing capability of SPF in support of the Orion Project's requirement for Space Environments Testing (SET). The HSDAS architecture is a modular design, which utilizes fully-remotely managed components, enables the system to support multiple test locations with a wide-range of measurement types and a very large system channel count. The architecture of the system is presented along with details on system scalability and measurement verification. In addition, the ability of the system to automate many of its processes such as measurement verification and measurement system analysis is also discussed.

**KEYWORDS:** Space Environments, Testing, Data Acquisition System, Vibration, Acoustics, Thermal Vacuum, Measurement Systems Analysis, Data Validation

## INTRODUCTION

NASA Constellation Program's Crew Exploration Vehicle (CEV) environmental testing goals require capabilities that are beyond any existing facilities within the United States. The CEV consists of the Orion Crew Module (CM), the Service Module (SM), fairings, and during the launch sequence the Launch Abort System (LAS), as shown in Figure 1. To meet CEV testing requirements, new spacecraft environment test facilities need to be constructed. These new facilities will simulate the spacecraft's mechanical vibration, acoustic vibration, thermal vacuum, and electromagnetic environmental effects. The data systems that measure, collect, store, process and transmit data must be robust, accurate, scalable, and dependable. The system must be flexible, adaptable, and able to support multi use facilities. In the case of environmental testing, data system inputs are interfaced with the test facility control system to aid in limit response control and test abort. This paper will describe the High Speed Data Acquisition System (HSDAS), which will be used at NASA Plum Brook's Space Power Test Facility to support CEV environmental testing.

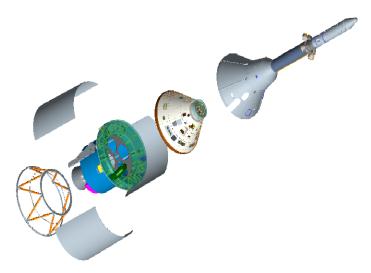


Figure 1. Crew Exploration Vehicle

The Space Power Facility (SPF) is located at NASA Plum Brook Station in Sandusky Ohio, shown in Figure 2. It houses the world's largest space environment simulation chamber measuring 100 ft. in diameter by 122 ft. high.

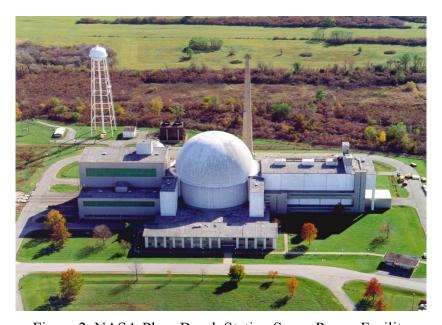


Figure 2. NASA Plum Brook Station Space Power Facility

This chamber will be used for CEV thermal vacuum testing. Figure 3 shows a test-specific cryoshroud and thermal heat flux system envisioned to provide the required thermal environment. The cryoshroud is composed of high-emissivity, gaseous-nitrogen-cooled panels. The thermal heat flux system is simulated by a combination of IR-lamps and resistance heaters mounted on a structure that envelopes the test vehicle. Additionally, Electromagnetic Environmental Effects (E3) testing will be conducted in the SPF chamber. Figure 4 shows a removable system of test-specific electronics that will provide the required electromagnetic environment for the CEV tests. The E3 facility will be used for both intra-system and inter-system tests.

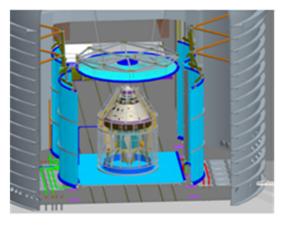


Figure 3. CEV Thermal Vacuum Testing

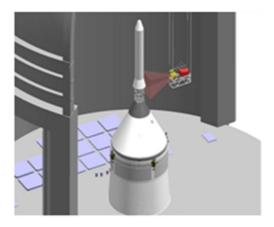


Figure 4. CEV (E3) Testing

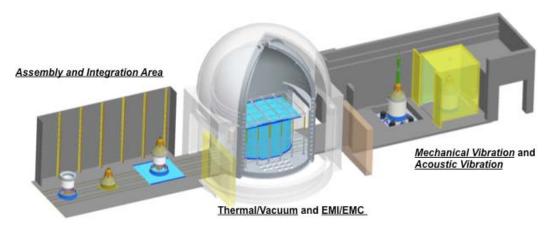


Figure 5. Space Environmental Testing (SET) Facility

The addition of the Vibro-Acoustics test capabilities to SPF is depicted in Figure 5. Described below, these unique test facilities, along with the SPF vacuum chamber, will be able to simulate all the environments encountered by the CEV, and future test customers. The SET project is envisioned to be a group of distinct test facilities that simulate a spacecraft's launch environment, as well as in-space environments.

The Multi Axis Vibration Test Facility (MVF), Figure 6, is a three-axis vibration system. It will apply vibration in each of the three orthogonal axes (not simultaneously) with one direction in parallel to the Earth-launch thrust axis (X) at 5-150 Hz, 0-1.25 g-pk vertical, and 5-150 Hz 0-1.0 g-pk for the horizontal axes. In addition to the sine vibe table, a Modal floor sufficient for the 20-foot diameter test article is planned.

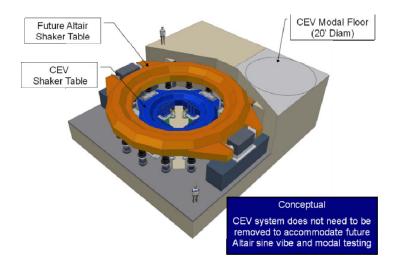


Figure 6. Multi-Axis Test Facility (MVF)

The Reverberant Acoustic Test Facility (RATF) is also located in the Disassembly Hi-bay. It consists of a reverberant-type acoustic test chamber, which is supported on a new, independent foundation from the original building. The RATF is designed to accommodate the CEV in its various configurations. The facility is being designed to provide a 163dB Overall Sound Pressure Level (OASPL). Figure 7 shows the relationship of the RATF to the MVF facility.

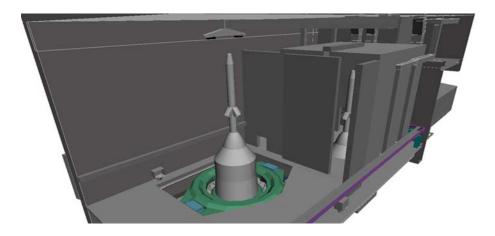


Figure 7. MVF in foreground, RATF with Doors Partially Open

## HSDAS ARCHITECTURE OVERVIEW

The SET's HSDAS is designed to meet the testing requirements of the Mechanical Vibration Facility, Reverberant Acoustic Test Facility, and Thermal Vacuum test facilities. The data acquisition system (DAS) includes the test article sensor interface cabling, the signal conditioners, data recording, storage, display, and archive systems.

The DSPCon Inc.\* Piranha III (P III) Data Acquisition System (DAS) that anchors the HSDAS is based entirely on Commercial Off The Shelf (COTS) hardware, and open hardware/software standards. The acquisition stations which house the analog to digital (A/D) converters, digital signal processor (DSP) board, Fibre channel (FC) interfaces, and G4 Power PC embedded processors are connected to RAID storage arrays by a storage area network (SAN) over fibre channel. This architecture, shown in Figure 8, allows the data stations to be located at the test facilities while appearing to be locally attached to the disk arrays and servers located in the main control room.

The FC/SAN guarantees deterministic data acquisition at designed bandwidth per channel. There are currently 1024 channels of A/D's arranged in 32-channel subsystems, with expansion designed to support 1536 channels.

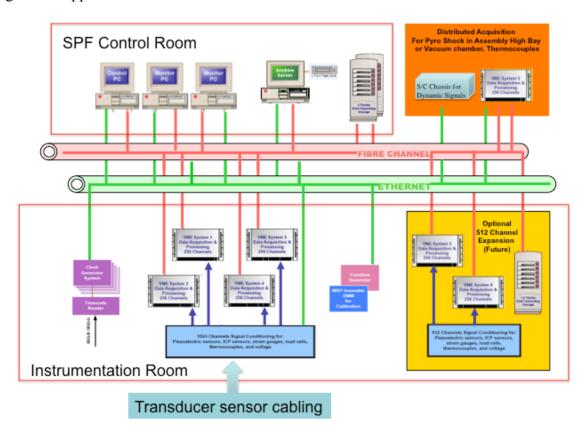


Figure 8. HSDAS Architecture

The system is required to provide a minimum 20 kHz analog bandwidth per channel, for up to 1536 analog channels.

Data is synchronized through a clock generator which is phase-locked to an externally supplied IRIG –B signal for accurate time stamping during long test durations.

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<sup>\*</sup>Trade names or manufacturers' names are used in this report for identification only. This usage does not constitute an official endorsement, either expressed or implied, by the National Aeronautics and Space Administration.

The P III data stations, fibre channel switches, and signal conditioners are housed locally to the MVF and RATF in a dedicated instrumentation room. This location minimizes the transducer cabling impedance, while protecting sensitive equipment from the environments produced by the test facilities.

The SPF control room houses the control, monitor, and archive workstations. The control workstation runs the application to configure the hardware, define the test parameters, and control access to the test data. There are four monitor workstations that run the visualization software for near real-time data display, as well as the limit check monitoring software. The archive server runs software to back up acquired data to mass storage and the Linear Tape-Open (LTO) magnetic tape library. The software has the capability to locate and serve archived data to other workstation clients for analysis, reduction or transmission. An on-line post processing workstation is available to define and automatically execute analyses on any number of channels once acquisition is complete.

The mass storage for the HSDAS consists of four, 3 Terabyte (TB) RAID (Redundant Array of Inexpensive Disk) arrays configured as RAID 1+0. This array architecture ensures that the array can continue to execute read and write requests to all of its virtual disks in the presence of any two concurrent disk failures. This array is sized to allow 12 data sets for all 1024 channels, at a 20 kHz analog bandwidth, for 40 minutes per test. A 9 TB tape library is available to archive data to magnetic tape.

## SIGNAL CONDITIONING

The HSDAS includes signal conditioners to condition response transducers used in vibration, acoustical and thermal vacuum tests. This would include Integrated Electronics Piezo Electric (IEPE) accelerometers, IEPE/charge microphones, 4 arm strain gauges, load cells, thermocouples, and voltage monitoring inputs. The Precision Filter 28000 Signal Conditioning System\* (PFI) provides up to 256 channels of fully programmable transducer conditioning per chassis, independent of the data stations. Hardware self-tests and calibrations traceable to National Institute of Standards and Technology (NIST) are possible.

Programming of the conditioning system via Ethernet is controlled through the Piranha III control computer using the Test Definition Editor. For configuration management purposes, all parameters associated with the measurement are contained in this test definition file. The system as currently envisioned is configured with 800 channels of IEPE conditioners, 40 channels of IEPE/Charge conditioners, 184 4-arm strain gage conditioners, and additional voltage amplifier conditioners. An additional 512 thermocouple signals will be acquired through a digital temperature scanner system, which will be detailed below.

The PF-28316C is a sixteen-channel IEPE accelerometer conditioner card with Long distance Transducer Electronic Datasheet (LTEDS) capability. The card supports programmable filtering, gain and IEPE supply current from 1 to 8 mA. For transducer health monitoring purposes, sensor open, short and bias level are monitored and reported.

The conditioners have a 4-pole programmable low-pass Butterworth filters (300 to 30 kHz, as well as Bypass mode), for spectral analysis, with low frequency high-pass filter at 0.25 and 10 Hz. This card has an additional buffered output per channel available on sixteen front panel connectors, which are available for MVF or RATF control system limit response/abort signals.

Four wire Triaxial IEPE sensors are planned for use in environments testing at the VTC. Some configurations of this transducer utilize a grounded input scheme, which could be susceptible to noise. Precision Filters has designed this card so that each channel has balanced differential current sources, with differential inputs, to minimize any ground loops normally associated with grounded transducers. This improved circuitry has been demonstrated to have approximately 30dB noise reduction improvement<sup>2</sup> over typical IEPE conditioners.

The PF-28104A is a quad channel bridge conditioner card for 1, 2 or 4 arm strain gage voltage bridge measurements. Gages can be connected in 2 to 10-wire configuration depending on the application. The card is capable of bridge auto balance and shunt calibration through voltage insertion or precision resistor applied as a shunt cal. The voltage excitation supply utilizes balanced voltage excitation to improve rejection of high frequency common-mode signals. There is a 4 pole programmable filter with flat amplitude response Butterworth characteristics for spectral analysis, or pulse mode response Bessel characteristics for time domain uses including transient (shock) and waveform analysis.

PF-27304 is a quad channel charge/IEPE conditioner with charge converters that cover full-scale charge from 2.5 pC to 160,000 pC. For IEPE sensors, the supply current range is 1 to 12.75 mA with a full-scale voltage range from 2.5 mV to 10.24 volts. A 2-pole High-pass filter with a -3.01 dB at 0.5 Hz attenuates DC voltages and low frequency noise.

Thermocouple measurements from the vacuum chamber will be conditioned with the Scanivalve\* DTS 3250 Temperature Digitizing System.<sup>3</sup> Each 64-channel unit has an integral Universal Temperature Reference (UTR) made up of an isothermal block with RTD's to measure the cold junction temperature. There is a low pass filter and 22 bit A/D converter per channel. The cold junction reference temperature correction and engineering unit conversion is done with an onboard microprocessor. NIST traceable lookup tables are used to convert the milivolt signal to engineering units specified. The stated accuracy for a type T thermocouple is  $\pm 0.25^{\circ}$  C, (excluding the thermocouple accuracy).

The data is sent over Ethernet to a switch that is connected to the P III DAS. In this manner an additional 512 channels of thermocouple channels will be added to the HSDAS to provide a complete solution for data acquisition at the SET facility. Theoretically, the HSDAS can be expanded to 2500 temperature measurements (4098 channels minus 1536 reserved for dynamic measurements at the VTC). The limiting factor will be the facility alloy feed-throughs that exist at the inner vacuum chamber and concrete shell that surrounds the chamber. Figure 9 shows the integration of multiple DTS 3250 units with the HSDAS, and a blown up functional diagram for a single unit.

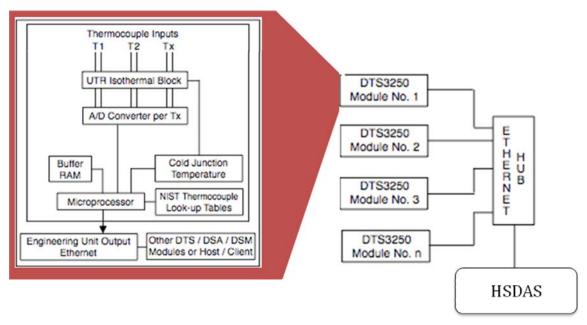


Figure 9. Thermocouple Conditioning System for Vacuum Chamber Test

## ANALOG ABORT / RESPONSE LIMITING

In addition to the MVF vibration control (Vcon) system's integral safety shutdown system, a redundant analog abort system is being developed. In the full configuration, this will be a 64-channel National Instruments\* CompactRIO system's FPGA with 64 high-speed inputs. Two-thirds of these inputs will have Trig Tek\* Model 530A tracking filters with the reference signal derived from the MVF controller. Inputs to the abort computer will consist of selected table control accelerometers, facility signals (pressures, temps, strains, etc.) and test article response signals (maximum number of 32 channels). Selected test article response signals are also available as inputs to the Vcon for response limiting inputs. All Vcon control signals will also be recorded in the HSDAS for correlation with the test article response signals.

Test article response signals will be routed to the control system via buffered outputs on the signal conditioners. Up to 64 channels can be routed to the controls/abort functions as needed.

## DATA COLLECTION AND STORAGE

While the functional role of the signal conditioning system in the HSDAS is to accurately process the analog portion of the signal chain, it is the commercial off the shelf (COTS) digitizing and data processing system and transducer interface cabling which completes the functional description of the VTC HSDAS system. There are many HSDAS requirements that relate strictly to the capabilities of a digital acquisition system (DAS), however, good system design places limitations on the location of hardware, cable lengths, transmission media, and data transport. Keeping the digitizers close to the signal conditioner outputs will minimize the cabling between the two systems, and reduce the risk of any un-wanted transmission line effects between the signal conditioning system's outputs and the digitizer system's inputs. While the benefit of this design choice is clearly recognized at the boundary between the two systems, the choice puts

additional requirements on the digitizing system to be selected; specifically, the ability to keep all of the individual digitizer sample clocks synchronized and the ability to transport the resulting data effectively. The challenge of meeting these requirements is evident when considering the total aggregate data rate in the system of 76,800,000 samples/second. This aggregate data rate is the whole system data bandwidth for data that must be recorded. It is a product of the whole system channel count of +1,500 channels and the required sample rate for a non-aliased measured data bandwidth requirement of 20 kHz for the complete HSDAS design.

To meet these challenging requirements, the P III DAS manufactured by DSPCon Inc. was selected.<sup>4</sup> The P III DAS provides a complete COTS turn-key data acquisition system solution with numerous state-of-the-art features, including the ability to provide complete control of the PFI signal conditioning system, in effect treating the signal conditioning system as a native part of the Piranha system. The Piranha III system also provides a non-aliased recorded channel bandwidth of up to 115 kHz. It offers inputs in 32-channel multiples on a single-board 6U VME brick. Multiple digitizer bricks can be operated independently or in concert to form more complex systems with larger channel counts. The digitizer bricks are joined together on a 4 Gbps Fiber-Channel Switched Fabric (FC-SW)<sup>5</sup> along with remote RAID units and Control PCs to form a Storage-Area Network (SAN). This architecture provides an unprecedented level of modularity and scalability that maximizes the versatility of the over-all system without compromising the system's high-speed capabilities. The PIII bricks are located in close proximity to the PFI signal conditioning modules, forming a complete Data Acquisition Subsystem. The Data Acquisition Subsystem can then be co-located or distributed anywhere within the SPF facility. Distributed acquisition of the HSDAS system is simply a matter of extending the FC-SW to the testing locations. Figure 10 shows the FC-SW SAN based distributed architecture of the combined PFI/PIII Data Acquisition Subsystems.

## ANALOG TO DIGITAL CONVERTERS

The P III solution uses 32 channel high-speed analog digitizing brick as the front-end of the system. The per-channel specifications are listed in Appendix A. Each digitizer brick requires an additional sample clock signal, that can either free run or be phase-locked to an IRIG-B signal for accurate time stamping even for long test. For the HSDAS this is provided through a DSPCon timing distribution component referred to as Time Central. This is a VME chassis, which contains four clock drivers, synchronized to IRIG-B. If necessary each of the four clock drivers can drive an independent sampling rate. Each A/D chassis is connected to one of the four clock drivers.

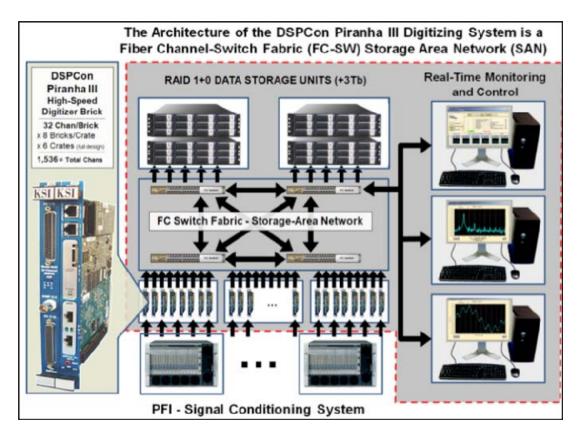


Figure 10. The FC-SW SAN Architecture of the Piranha III system

## **DATA TRANSPORT**

The VTC HSDAS is designed to support as many as 1,536 measurement channels of 16-bit data acquisition channels, each channel generating data with an maximum possible effective sample rate of 50 kHz. (Due to the use of Sigma-Delta A/D converters, the PIII digitizers are always oversampling at the maximum sampling rate possible at the hardware level. This method allows the PIII digitizer to use a DSP processor to filter and then decimate the data down to the sample rate that the system is requested to record at. This alias-free, decimated data stream is "effectively" the final sample-rate of the system even though the Sigma-Delta A/D converters are running as much as 256 times faster.) The calculation for the total system aggregate data collection rate is performed as follows:

Total Aggregate Data Rate = {Number of Channels}  $\times$  {data size}  $\times$  {Sample Rate}

Thus, for the VTC HSDAS this works out to be:

**153.6Mbytes/sec** =  $\{1,536 \text{ channels}\} \times \{2 \text{ bytes/sample}\} \times \{50,000 \text{ samples/sec/channel}\}$ 

Clearly, the task of transporting the aggregate data produced by the digitizers to a separate storage location is non-trivial. To accomplish this, the VTC HSDAS has been designed to use a 4 Gbit/second Fiber Channel (FC) switch fabric as the basis of a storage area network (SAN).

The choice of a Fiber Channel Switch Fabric Storage Area Network (FC-SW SAN) offers many advantages over traditional network topologies namely:

- Delivers sustained BW of 97 Mbytes/Sec for large File transfers.
- Support for distances up to 10 Km.
- Allows for shared storage.
- Provides a scalable network.
- Robust data integrity and reliability.
- Fast data access and backup.
- Provides the ability to connect many diverse processing and storage elements.
- Low transmission overhead.

The choice of a fiber channel (FC) switch fabric offers a number of advantages over a traditional TCP/IP Ethernet LAN. In particular, the FC data transport infrastructure is deterministic and has very low latencies (~10 microseconds) compared to Ethernet, which provides non-deterministic data transport and has data latencies that are typically on the order of a few milliseconds. Another advantage of the FC switch fabric is its ability to support the Small Computer System Interface (SCSI) protocol. Using this protocol allows the system to transport data across the switch fabric with protocol overhead of less than 5% versus the more than 20% protocol overhead of a TCP/IP switch fabric. This means that more of the total bits per second of the switch speed is utilized for the actual data and results in the ability to achieve higher sample rates from the system.

## **DATA STORAGE SYSTEM**

As a distributed system, the data produced by the digitizers is transported across the fiber channel switch fabric and written to a centralized system of storage disks. The data storage system for the HSDAS has been designed to support 8 hours of continuous data collection at the full system rate of 153.6 Mbytes/sec. The calculation of total disk storage is as follows:

Total Storage Size = {Aggregate Data Rate}  $\times$  {required test duration}

Thus, for the VTC HSDAS this works out to be:

 $4.5 \text{ Terabytes} \approx \{153.6 \text{ Mbytes/sec}\} \times \{8 \text{ hours} \times 3,600 \text{ seconds/hour}\}\$ 

In addition to providing adequate storage capacity for the full-system data acquisition, it is also essential that the data storage system be redundant in order to ensure that no data is lost in the event of a component (disk) failure. Traditionally, this has done by writing that data to two locations; the first is usually a data storage unit that is located near the test article and the second is a "copy" of that data that is being written to a geographically different location. Due to the speed of the 4 GBps Fibre Switch SAN, the HSDAS is able to write directly to one location. Redundancy is achieved by providing the data storage units in a RAID 1+0 configuration. This configuration was selected to ensure the integrity of the recorded data even in the event of two hard-drive failures in the data storage system, without compromising the maximum write speed of the system. Once a test is completed, data can be moved off the RAID units and on to other systems for post-processing, archiving, and delivery to the customer.

## **SCALABILITY**

The VTC HSDAS has been designed to provide for a minimum of 1,024 analog measurement channels available to the RATF, MVF and other test locations at the SPF Facility. The installation and design of the HSDAS have included provisions for a future expansion of the system to a total 1,536 measurement channels. The HSDAS system architecture could additionally support an even greater number of measurements. The practical and physical limits of how the HSDAS system can be scaled are divided into four separate functional areas: Signal Conditioning Scalability, Channel Count Scalability, Data Rate Scalability and Data Storage Scalability.

## **Signal Conditioning Scalability**

Cabling and signal conditioning of the transducers in the field is the first practical limit that must be addressed in any attempt to scale-up the system. The amount of rack space, conduit and cable tray capacity provided will support the upgrade path to 1,536 channels; larger channel counts would require additional paths. By design, the signal conditioning system is a modular component of the HSDAS, and as such it allows for the substitution of any other signal conditioning equipment that provides equivalent capabilities with a greater channel density. The result would be added channel capacity for the presently allocated physical space. DSPCon currently supports a wide variety of signal conditioning technologies. The majority of the PFI 28000 series signal conditioning products are already fully integrated into the DSPCon Piranha III system. Additional signal conditioning equipment and digitizers could be located near the test location in the facility. Including these remote components into the HSDAS would be simply a matter of extending the fiber-channel storage area network to that location. An example of this is the planned inclusion of the SPF thermal-vacuum chamber's temperature sensors. This plan will increase the HSDAS system channel count by an additional 512 channels to the 1,536 high-speed channels in the baseline design.

## **Over-all Analog Channel Count**

The Storage-Area-Network (SAN) architecture of the DSPCon Piranha III system provides nearly open-ended scalability with regards to the system's total channel count. The actual limit to the number of possible channels in the DSPCon Piranha III system is a function of the absolute physical limit of the number of logical channels supported by the Fiber-Channel Switch Fabric (FC-SW). The current HSDAS hardware uses a 4<sup>th</sup> Generation (4 Gbps) FC-SW fabric<sup>6</sup>, which supports 2<sup>12</sup> or 4,096 logical channels. Adding more channels to the Piranha III system is as simple as connecting additional digitizer bricks to the FC-SW SAN. In a practice, however, additional channels will reduce the average data-rate per channel of the system. This is determined by the bandwidth of the FC-SW and is discussed below.

## **Data Rate Scalability**

Once digitized, all data from the Piranha III digitizer bricks is transported to the data storage units across a Fiber-Channel Switch (FC-SW) fabric Storage-Area-Network (FC-SAN). The maximum aggregate sample rate of the HSDAS system able to be processed by the HSDAS is

directly determined by the speed of the FC-SW fabric. The HSDAS FC-SW fabric uses 4 Gbps Fiber Channel Switches that facilitate the SAN system data transport of the 51,200,000 aggregate samples collected by 1,024 measurement channels acquiring 16-bit data at 50 kHz. The 4 Gbps FC-SAN switches provide ample bandwidth to support the full 1,536 measurement channel upgrade. As faster FC switch components become available in the future, the FC-SAN fabric can be easily upgraded to achieve greater bandwidth, which directly translates to an increase in the total aggregate sample rate allowing increased measurement bandwidth.

## **Data Storage Scalability**

The data storage component of the HSDAS FC-SW SAN is provided by four rack-mounted RAID 1+0 data storage arrays. These components are configured by, and provided for, DSPCon as part of their turnkey design for the HSDAS system. The four units have been selected to facilitate the requirement of a 20 kHz recorded bandwidth for 1,024 channels running for 8 full-hours. This works out to be 3 terabytes of total storage capacity. Increasing the storage capacity to support higher aggregate sample rates, additional data channels and/or longer recoding times is straight-forward. The VTC HSDAS benefits from the pure-COTS availability and open-standards of the RAID and SAN technology to make scaling the data storage capability a simple matter of adding additional RAID arrays and re-configuring the system.

## **MEASURMENT SYSTEMS ANALYSIS**

A degree of uncertainty and variation exists in every measurement. It is an unavoidable part of the measurement process. While systematic errors can be eliminated by calibration, random errors can only be minimized through understanding the reason for the errors, minimizing their effects, and quantifying the residual errors for the test customer. The methodology for estimating the uncertainties in measurements and in the experimental results calculated from them must be structured to combine statistical and engineering concepts. The data acquisition end-to-end margin of error will define the measurement tolerances. The approach to quantifying the degree of uncertainty associated with any single measurement is mature, and there are currently accepted methods of standardizing the uncertainty. 8, 9

As system channel counts grow large and signal chain diversity increases (accelerometers, strains, voltages, pressures, temps, discretes, speed etc), it becomes challenging to ascertain the quantified level of measurement variability that exists in the data acquisition system. We refer to this process of characterizing the measurement variability of each channel in a system as Measurement Systems Analysis (MSA). Establishing the MSA data for a measurement system, and packaging it as a consistent deliverable to a test customer, is an issue faced at all major testing facilities. While the end-goal of an MSA for any system is the same, the processes involved vary greatly from facility to facility, as their exact form is determined by the technologies available at the site. In older, all-analog systems, and even in modern systems that are not integrated sufficiently, performing uncertainty calculations and quantifying the measurement quality can only be achieved at great costs of time and manpower. Given the large channel count, high-speed digitizing rates and diverse instrument types being supported by the VTC HSDAS, avoiding the potential difficulty in performing MSA activities for the whole system has been addressed at the earliest stages of the HSDAS design.

#### NIST TRACEABLE CALIBRATIONS AND REPORTING

The design of the VTC HSDAS benefits greatly from the use of a highly integrated, modular architecture where each component is selected to provide optimized network controllability and network status monitoring. Specific components have been incorporated into the HSDAS design to facilitate a nearly hands-free MSA. The PFI 28000 Test Subsystem<sup>10</sup> option is part of the signal conditioning system design. This subsystem consists of an Agilent 34410A Digital Multi-Meter and an Agilent 33220A Function generator, both of which are fully network controlled and integrated into the signal conditioning system by Precision Filters. This provides seamless NIST traceable calibrations for all of the analog signal components of the signal conditioning system. It also ensures that each element of the signal conditioning system is operating within its stated manufacturing tolerances. The PFI control software for the signal conditioning system allows operators to conduct fully automated Factory Acceptance Tests (FATs), which can be run before and/or after a test to ensure the integrity of the signal conditioning system. As purchased, the calibration capabilities of the PFI Test Subsystem are native to the Precision Filters 28000 series system. For the VTC HSDAS, the NIST traceable calibration capabilities of the PFI Test Subsystem are available to the P III DAS. This allows the P III DAS software to utilize the PFI Test Subsystem to extend the systems ability to calibrate the analog-to-digital converters, and has also been integrated into the P III DAS to provide complete NIST traceable calibrations to all analog signal-processing components in the entire system. The finished system is capable of performing highly automated remote-controlled calibrations. By adding the Long-Distance Transducer Electronic Datasheet (LTEDS) capability and the health monitoring features of the PFI signal conditioners, nearly fully automated reports can be generated to verify configuration management and setup of the vibration sensors.

## MEASUREMENT UNCERTAINTY AND DATA QUALITY

Central to the goal of the MSA is the task of quantifying the "normality" of the data acquired and providing a high level report which clearly shows the quality of the data from each channel across the whole system. Using consistent criterion, the MSA software calculates the mean, standard deviation, skewness and kurtosis for each channel. Each of these values is then compared to a pass/fail threshold limit from which assures the normality of the channel and allows for the direct calculation of the uncertainty limits. From this the more commonly understood values of accuracy and precision can be derived. In addition to a whole system, passfail report, the MSA software algorithm provides detailed graphs for each channel of data across the entire system in the form of a simple, easy to read summaries of the acquired data. For diagnostic purposes, the data normality tests for each channel can be graphed for individual inspection. Figure 11 shows an example of a presentation of a single channel's data, which is typical of what is provided for all channels in the system. Anomalies in the data can be quickly and easily identified not only by viewing the data as a time series but also by viewing the results of the normality tests in traditional analytic ways such as the FFT power spectrum, lag plots, histograms and  $\chi^2$  (Chi-Square) "goodness of fit" tests. While the time-series presentation of the data is unrevealing, the basic normality is observed in the histogram (second frame). Here we see the straight histogram with a Gaussian curve over-laid as determined from the mean and standard deviation calculations for the data. Additional presentations of the power density spectrum and lag plots are provided for to reveal any high frequency or low frequency abnormalities. Figure 12 shows a summary for all the channels sampled.

The data for the channel shown is preliminary and was taken from an un-calibrated P III digitizer brick that was not connected to the finished system. The combined capabilities of the features and characteristics of this HSDAS system in combination with the automated MSA processes, the NIST traceable calibrations and the measurement system uncertainty analysis for the HSDAS provide the SPF Facility with highly efficient method of conducting Data System Validation and Verification exercises.

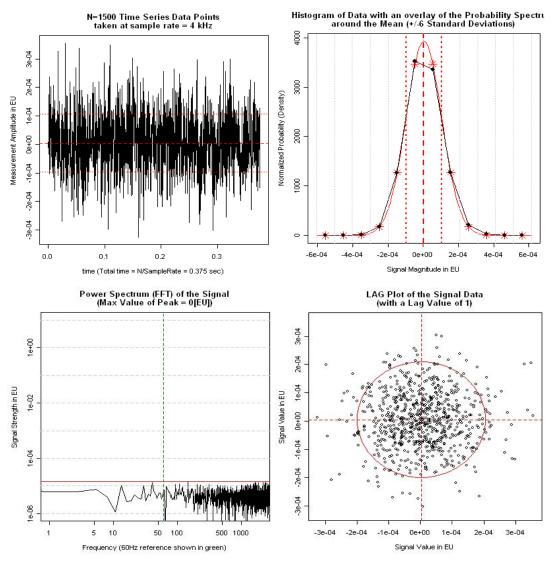


Figure 11. The MSA Reports on an Individual Channel's Data Quality

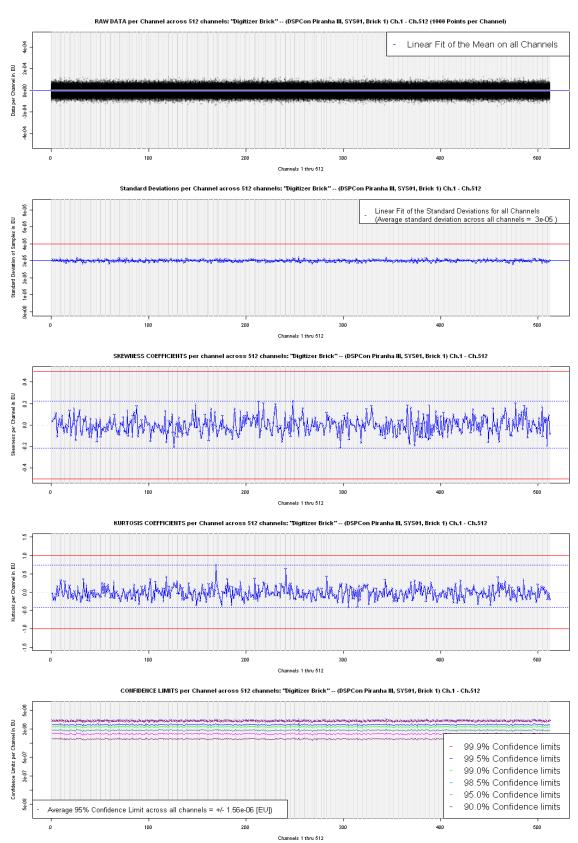


Figure 12. Whole System MSA Report for a 512-channel system

## **CONCLUSION**

A large-scale, distributed, high-speed data acquisition system is planned for the Vibro-Acoustic Test Facilities currently under construction at NASA Plum Brook Station. The HSDAS will be used additionally to support data acquisition in the thermal vacuum chamber at SPF. The system architecture and hardware capabilities were designed to be flexible, adaptable and expandable. By leveraging the highly integrated, modular architecture, a method to characterize the measurement variability was discussed. Combined with NIST traceable calibrations and measurement uncertainty analysis, these processes should guarantee valid test data for our customers.

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## **BIOGRAPHIES**

Mr. Hill works in the Plum Brook Management Office of NASA Glenn Research Center's Plum Brook Station in Sandusky Ohio. He is currently serving as Senior Data Systems and Controls Engineer. He has over twenty years experience as a test engineer in NASA Glenn's major Aeronautics Wind Tunnels and Space Test Facilities. Besides leading the HSDAS effort at Plum Brook's Space Power Facility (SPF), he is the DAC lead for the Space Propulsion Research Lab (B-2) Test Facility. He holds a BS in Electrical Engineering Technology from Cleveland State University, and MS in Electrical Engineering, also from Cleveland State University.

Mr. Evans works in the Plum Brook Management Office of NASA Glenn Research Center's Plum Brook Station in Sandusky, Ohio. He is currently the lead Data Systems Engineer at the Space Power Facility. He has over fourteen years experience as a mixed-signal instrumentation and digital systems engineer, which includes over a decade of experience from the nuclear physics community having worked at the Thomas Jefferson National Accelerator Facility as a digital instrumentation engineer on the 10kW Free Electron Laser Project. He holds a BS in Electrical Engineering from Geneva College (1995), and an MS in Applied Physics and Computer Science from Christopher Newport University (2006).

## APPENDIX A

Digitizer Signal Acquisition Specifications	
Sample Rate	1 K to 256 KS/S/Ch in .001 S/S Increments
Input Slew Rate	15 V/uSec
Input	Differential, ±10 v @ gain of 1
Input Impedance	100 kOhms
Frequency Response	$\pm$ 0.1 dB, DC to 90 kHz
Gain (Optional)	1, 10, 100
Time Skew	<50 ns
Inter-channel Phase Match	<0.1° @ 10 kHz, <1° @ 90 kHz
CMMR	100 dB Typical
<b>Analog Anti-aliasing Filter</b>	2-pole Butterworth @ 320 kHz
Digital Filter	Sigma/Delta @ 0.4535 x Sample Rate
Coupling	AC and DC
SNR	>90 dB
SFDR	>95 dB
SINAD	>90 dB