

Advanced Avionics and Processor Systems for Space and Lunar Exploration

Andrew S. Keys¹, James H. Adams,²
NASA Marshall Space Flight Center, Huntsville, AL 35812

Robert E. Ray³
Jacobs Engineering Group, Huntsville, AL 35801

Michael A. Johnson⁴
NASA Goddard Space Flight Center, Greenbelt, MD 20771

and

John D. Cressler⁵
Georgia Institute of Technology, Atlanta, GA 30332-0250

NASA's newly named Advanced Avionics and Processor Systems (AAPS) project, formerly known as the Radiation Hardened Electronics for Space Environments (RHESE) project, endeavors to mature and develop the avionics and processor technologies required to fulfill NASA's goals for future space and lunar exploration. Over the past year, multiple advancements have been made within each of the individual AAPS technology development tasks that will facilitate the success of the Constellation program elements. This paper provides a brief review of the project's recent technology advancements, discusses their application to Constellation projects, and addresses the project's plans for the coming year.

Nomenclature

°C = Temperature (degrees Celsius)

I. Introduction

The Advanced Avionics and Processor Systems (AAPS) project endeavors to expand the current state-of-the-art in radiation hardened electronics and avionics for high performance devices robust enough to withstand the extreme radiation and temperature levels of the space environment. The primary customers for AAPS-developed technologies are the multiple mission elements of NASA's Constellation Program, including the Altair Lunar Lander project, Lunar Surface Systems elements, and Extra Vehicular Activity (EVA) elements. Secondary customers for AAPS technologies include NASA science missions, collaborative efforts with other agencies of the US Government, and commercial applications. The newly-named AAPS project, previously known as the Radiation Hardened Electronics for Space Environments (RHESE) project, is a part of the Exploration Technology Development Program (ETDP), which manages an entire suite of technologies needed by the Constellation Program to accomplish many of the goals outlined in NASA's Vision for Space Exploration¹. For an external review of the ETDP and its multiple technology development projects, reference the 2008 review conducted by the National Research Council².

¹ Project Manager for RHESE, NASA MSFC VP33, AIAA Non-member.

² Cosmic Ray Astrophysics Team Lead and Modeling Task Lead, NASA MSFC VP62, AIAA Non-member.

³ Reconfigurable Computing Technical Lead, NASA MSFC EV43, AIAA Non-member.

⁴ Asst. Chief for Tech., Elect. Eng. Div. and High Perf. Processor Tsk Lead, NASA GSFC 560, AIAA Non-member.

⁵ Ken Byers Professor, School of Electrical and Computer Engineering, Georgia Tech, AIAA Non-member.

II. AAPS Technology Development Tasks

The individual technology development tasks that comprise the AAPS project are broad-based and diverse, but all carry the common goal of providing advanced avionic technologies that are capable of enduring the natural environments encountered by their host spacecraft. The AAPS technologies are targeted for development because they are generally not currently available from commercial sources. Specifically, the individual AAPS technology development tasks that comprise the project are:

- Model of Radiation Effects on Electronics (MREE),
- Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF),
- Radiation Hardened High Performance Processors (HPP),
- Reconfigurable Computing (RC),
- Volatile and Nonvolatile Memory Technologies, and
- Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments.

Because the AAPS project is an active technology development effort, advancements are continually being made to address the technology needs and avionic environmental hardness requirements of the multiple Constellation program projects. This paper builds on the project information provided in two previously publicized articles³⁻⁴ and summarizes some of the more recent accomplishments made within each AAPS technology development task during the U.S. Federal Government's 2009 fiscal year, ranging from 01 October 2008 through 30 September 2009. Each of the six AAPS technology development tasks (plus the project management function) is addressed in the following sections. Each task summary includes a brief description of the task followed by a short summary of the past year's achievements.

A. RHESE Project Management

The RHESE project management function handles the day-to-day administrative and programmatic concerns of the project including budget planning, schedule development, accomplishment monitoring, risk assessment, and project execution. The project management function serves to enable the technology development tasks and to represent the task accomplishments to the ETDP program office. NASA's Marshall Space Flight Center (MSFC) manages the RHESE project. Within the past fiscal year, the RHESE project was baselined in its plan for technology development by the ETDP office with the details captured in the RHESE Project Management Plan.

As a strategy to reduce duplicative efforts between NASA and other government-sponsored developers that may also be investing in environmentally hardened electronic and avionic technology, it is the responsibility of the RHESE project management function to be cognizant of external activities and investments being made by these other U.S. Government agencies, federal laboratories, academic institutes, and commercial developers and to develop collaborative efforts where appropriate. Collaborative efforts strive to leverage the technology investments of multiple sources to deliver products that may otherwise not be realized through independent and competing efforts. To maintain cognizance of current activities, the RHESE project manager and task leads regularly attend reviews, presentations, and conferences where multiple other non-NASA technologists are working to improve the state-of-the-art in radiation hardened electronics. Over the past year, the RHESE project was represented at many of these gatherings to discuss and coordinate technology development activities, including the AIAA SPACE 2008 conference, the Air Force Research Laboratory (AFRL)-sponsored Radiation Hardened Electronics Technology workshop, the Institute of Electrical and Electronics Engineers (IEEE) Aerospace 2009 conference, The Fault-Tolerant Spaceborne Computing Workshop 2009, the Government Microcircuit Applications and Critical Technology (GoMACTech) 2009 conference, and the IEEE Nuclear Science and Radiation Effects Conference (NSREC) 2009. Coordination activities with other government-sponsored developers continue into the coming fiscal year with particular emphasis on the six technology development tasks as summarized in the following sections.

B. Model of Radiation Effects on Electronics (MREE)

RHESE's MREE task is focused on developing an updated model of radiation effects on electronics. The previously used model, Cosmic Ray Effects on Micro Electronics 96 (CREME96)⁵⁻⁶, has been for years the industry standard modeling tool for estimating single event effects (SEEs) in electronics. However, over the past thirteen years since its release, the state-of-the-art in microelectronics has continued to advance toward architectures that incorporate smaller feature sizes and more complex electronic structures that often include heavy metals – all of which make today's modern electronic architectures more susceptible to SEEs and radiation induced failures. The paradigm for SEE prediction in the CREME96 model is deficient in accounting for the small features, complex geometries and heavy elements common to modern electronic architectures. It is therefore the goal of the MREE

task to develop a more physics-based approach to SEE prediction that will provide accurate results for modern electronics parts.

Efforts are ongoing to enable the new modeling tool the ability to assess the spacecraft's surrounding structure for purpose of calculating spacecraft self-shielding effects when assessing the susceptibility of a particular microelectronic circuit to the external radiation environment. By using a Computer Aided Drawing (CAD) file representation of the spacecraft's structure, the modeling tool will be designed to process the CAD file – complete with material fields within the file - to determine the level of shielding a sensitive electronic component may receive from the surrounding spacecraft structure. This approach also allows the detailed physical structure of the microelectronic circuit and the pattern of hole-electron creation within that circuit structure to be taken into account so that the collected charge and the resulting currents within the circuit may be estimated more accurately. This new model employs Monte Carlo simulations to predict SEE rates, allowing the updated software to be referred to as "CREME-MC." The CREME-MC codes account for a propagating particle's energy loss attributable to interactions with the spacecraft, the electronic packaging, the metallization used to build the circuit, and the metallization located within the semiconductor itself. During propagation, the effects of nuclear interactions and energy loss by ionization are taken into account as well. The calculated radiation environment at the chip will be used to not only estimate the device's accumulated total dose, but to also drive a second Monte Carlo simulation that predicts the SEE rate as described above.

Most of the accomplishments achieved by the MREE task within the past fiscal year stem from the establishment of the online CREME-MC website⁷ that will be employed to host the final Monte Carlo version of the CREME software. The online site currently offers the user the opportunity to execute a Monte Carlo based simulation of the energy deposition within multiple sensitive volumes that represent junctions within the electronic device under evaluation. The sizes, shapes and locations of these volumes are specified by the user. The site also offers a user the ability to define a multi-layered material stack that approximates the structure of the electronic device under evaluation. For continuity, the site will also host the older CREME96 and CREME86 versions of the software. User files from the CREME96 site⁶ at Naval Research Laboratory will be preserved and can be uploaded to the new CREME-MC site⁷ at Vanderbilt on request, allowing users the ability to access previously run data files. In order to ensure that the tool is appropriately addressing the needs of the electronics and avionics community, a period of "alpha" testing allowed select users the opportunity to run the code, evaluate the results, identify software problems, and submit comments that identify problems, deficiencies, or even desired capabilities that are not currently implemented. As of this past summer of 2008, the alpha testing concluded for the software and a period of "beta" testing has begun.

The capabilities of the CREME-MC site will be upgraded as the new model is improved and extended. The models that define the space environment, such as the lunar neutron environment, the galactic cosmic ray environment, and the solar particle environment are all being updated. Features planned for implementation in the coming years include the development of a nested sensitive volume assessment capability, further upgrades to the environmental models, and full hosting of the CREME96 and CREME86 software tools and associated users' files.

Additionally, there are tools enable the conversion of spacecraft CAD drawings into a format used for Monte Carlo transport code calculations. The current plan is to incorporate these in a downloadable software package that can be used to compute the radiation environment at the part of interest within the spacecraft. The resulting environment will then be uploaded to the CREME-MC site for SEE calculations. This approach avoids the need for users to upload a CAD model of the spacecraft to the CREME-MC site over the internet. Instead, the users can maintain the security of their CAD model by doing the radiation transport calculations at their facilities.

This task is led by NASA's Marshall Space Flight Center with contracted support from Vanderbilt University.

C. Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

The FPGA is an electronic component that has experienced widespread usage in multiple applications due to its ease of programmability. Because the FPGA can be customized, it is also an inexpensive, and therefore attractive, alternative to the design and development of a non-programmable, hardwired application-specific integrated circuit (ASIC). FPGAs are available in multiple architectures. The most common is the Static Random Access memory (SRAM)-based FPGA, which is reprogrammable within an active system to perform a large variety of functions. But these FPGAs are much like volatile memory in that they require reconfiguration after each power cycle. Also, due to their CMOS-based architecture, they are susceptible to radiation events. Antifuse FPGAs solve the volatility and radiation susceptibility problem by allowing a single configuration to be permanently programmed onto the device. Although radiation-hardened antifuse devices are less susceptible to single-event radiation effects, the main disadvantage of this architecture is that it can only be programmed once prior to use.

In an effort to address the radiation susceptibilities of a SRAM-based FPGA, the AAPS project has teamed with multiple government and industry partners to support the development of a radiation-hardened by design (RHBD) version of the Xilinx Virtex-5 FPGA. The resulting device will yield the benefits of reconfigurable hardware implemented in a radiation hardened by design architecture.

The SIRF task has progressed toward maturity over the past fiscal year through the fabrication and test of an FX1 version of the SIRF chip. This FX1 version has been tested and results are being assessed to assist with the next and final fabrication of the SIRF chip. Final delivery of the radiation hardened Virtex-5 FPGA is expected in December of 2010.

D. High Performance Processors (HPP)

Certain capabilities within the Constellation architecture, such as autonomous spacecraft operations, surface mobility, and hazard avoidance and landing, require intensive data processing capabilities. Whereas numerous systems with these capabilities have been developed and deployed, their requirements and implementations are typically constrained by data processing throughput, power resources, and susceptibilities to radiation effects. The AAPS HPP task seeks to expand the capabilities of data processing-intensive, spaceflight systems by advancing the sustained throughput and processing efficiency of high-performance radiation-hardened processors while seeking processor architectures that minimize power consumption.

The performance of processors developed from technologies appropriate for aerospace environments lags that of commercial processors by multiple performance generations. The highest performing radiation tolerant, commercially produced electronics offer increased performance at expense of reduced power efficiency. The HPP task seeks to concurrently advance the state-of-the-art of these two metrics; sustained throughput and processing efficiency.

The need for power-efficient high-performance radiation-tolerant processors and the peripheral electronics required to implement functional systems is not unique to NASA; this capability could also benefit commercial aerospace entities and other governmental agencies that require highly-capable spaceflight systems. This task will therefore leverage to the extent practical, relevant external technology- and processor-development projects sponsored by other organizations. Accordingly, important factors in defining and implementing the HPP strategy and implementation are the investment plans of these organizations and cognizance of relevant prior and ongoing NASA investments. The HPP team is addressing both of these factors through ongoing communication and collaboration with these other organizations.

Within the past fiscal year, the HPP task has fostered two promising processor development activities that are currently undergoing evaluation for their suitability for use in NASA's Constellation program. The first is a collaboration between the AAPS project and NASA's Innovative Partnership Program (IPP). A proposed effort between GSFC, JPL, and Coherent Logix Incorporated entitled "Extremely High-Performance, Ultra-Low Power, Radiation-Tolerant Processor: An Enabling Technology for Autonomous and Computationally Intensive Capabilities," was selected for funding by the IPP in FY2008. This effort seeks to assess the radiation susceptibility of the base HyperX processor, then formulate and implement radiation hardening strategies using software techniques. The effort began by performing a baseline radiation test of the HyperX processor, then used the results to develop software techniques that would mitigate susceptibility of the processor to radiation effects and damage. A second battery of tests was performed in this past fiscal year to assess the effectivity of the software techniques in radiation damage mitigation. Results for these tests are being assessed and documented.

To validate the radiation mitigation techniques in a flight environment, the processor will be flown as a part of the Materials International Space Station Experiment-7 (MISSE-7). The MISSE series of flight experiments provide an opportunity to assess the durability and functionality of various hardware components and materials during long duration exposure to the space environment in low Earth orbit. The flight hardware to be flown on MISSE-7 includes four Hyper-X processor boards and one Aeroflex LEON3FT controller board. This flight hardware has been successfully integrated, tested, and delivered to NASA's Kennedy Space Center for launch in late 2009.

The second processor development activity being worked through the HPP task is the assessment of the On-board Processing Expandable Reconfigurable Architecture (OPERA) Processor as developed by Tiler. This effort began as a DARPA initiative to develop a processor that performs with a high level of efficiency across all categories of application processing ranging from bit-level stream processing to symbolic processing, and encompassing processor capabilities ranging from special purpose digital signal processors to general purpose processors. Commercial versions of the OPERA processor have been procured and are currently being benchmarked to ensure the capabilities match the needs of the targeted Constellation applications.

One of the more mature capabilities that will require a highly capable radiation hardened flight processor is the Autonomous Landing and Hazard Avoidance Technology (ALHAT). This capability is being developed to operate

aboard Constellation's Altair Lunar Lander during descent of the lander to the lunar surface. The ALHAT system will be responsible for transmitting lidar signals, receiving the lidar returns, processing the returns for information regarding hazards within the landing site, comparing those hazards to known objects within onboard maps, identifying unknown objects, displaying descent information to the crew, and controlling the descent of the lander.. All of these functions combined result in requirements that cannot be efficiently met by today's commercially available radiation-hardened flight processors. To determine if the candidate processors described in this paper will be appropriate for Constellation applications such as the ALHAT system, NASA's JPL is working to benchmark the performance of the Hyper-X processor and the OPERA architecture as they run ALHAT processing algorithms.

This task is lead by NASA's Goddard Space Flight Center, with support from NASA's Marshall Space Flight Center, NASA's Langley Research Center, and the Jet Propulsion Laboratory.

E. Reconfigurable Computing (RC)

The concept of Reconfigurable Computing⁸ offers the promise of new capabilities within any particular plan of exploration that involves complex spacecraft. These new capabilities focus on the reduction of subsystem level flight spares inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces.

The RC task proposes a new paradigm for circuitry to respond to failures other than by redundancy voting schemes alone. The RC task strives to provide better failed circuitry detection, enablement of autonomous repair and/or replacement of defects, and support adapting circuitry to accommodate system failures. The goals of the RC task also include the concept of requiring a single configurable processor to autonomously conform to multiple configurations. Accomplishment of this goal yields a reduction in spares required to be carried on long-duration missions, since a single spare would then fit many processing functions. Such architecture adaptability will provide a great saving in spares volume and weight required by extended duration missions.

Three areas of focus have been identified for the RC task; internal modularity, external modularity, and fault detection and mitigation. The first involves ability of the core processor to emulate any form of computing resource as needed to serve all of the capacities required. The second enables the first by providing a capability to interface resources to any target system, by adapting communication standards, physical and electrical interconnections, and other parameters of the host system to hook up to the computing resource. The final allows the detection of an internal fault and autonomous isolation and recovery from the fault without required external involvement.

Cyclical and/or selective periodic testing will mitigate radiation damage and other commonly-feared failures. Reserve copies of circuitry will be generated and tested in order to bring them online in functional condition without interrupting system tasks. Then, the subsystem to be evaluated will be taken offline and tested with known inputs for known expected outputs in order to isolate possible undesirable responses. Provided the subsystem checks out as functionally correct, it can be returned to service, held in reserve for the next cycle of checks, or the reconfigurable processing units can be returned to a managed store for later redeployment. If the subsystem fails verification, the portions of circuitry causing the failure may be further isolated to mark those parts of the circuitry as defective and return the remainder to reserve, much as blocks of a computer hard disk are marked bad and ignored during future operations. Life limitations on electronics can be mitigated by these same means. Circuitry which becomes unstable and unreliable after extended active lifetime can be retired and new reserve circuitry powered up and configured into service, thus extending overall lifetime of the system.

Flexibility is also bolstered by the RC task. Interface reconfiguration can allow a single processor to make connections through different external interfaces as needed. By providing this external modularity, vehicle system integrity is enhanced by allowing processors to be transferred among busses and networks to replace lost functionality. Further, this directly supports the concept of reduced flight spares required by long duration missions.

Over the past fiscal year, the RC task has demonstrated the first of the three desired characteristics: internal modularity. A Xilinx FPGA was shown to reconfigure itself to perform three disparate tasks: motor control, DSP processing (via a Fast Fourier Transform, or FFT), and as a finite state machine (via a Turing Machine simulator). Work has begun on demonstrating the second characteristic: external modularity. Procurement of the necessary equipment for this demonstration is complete. This demonstration is tentatively scheduled for Fall 2009.

Also, to ensure continued leadership in the reconfigurable computing community, the RC team is providing a sponsorship of an academic membership in the Center for High Performance Reconfigurable Computing (CHReC), a consortium of academic representatives assembled to recommend Reconfigurable Computing research activities.

This task is managed by NASA's Marshall Space Flight Center with support from NASA's Langley Research Center.

F. Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments

The extreme temperature conditions on the lunar surface (at worst case, -230°C in shadowed polar craters, and ranging from -180°C to +120°C lunar night to day) precludes the use of conventional terrestrial electronics for applications such as sensing, actuation, and control that must be performed in the lunar ambient environment. This is problematic since the development of modular, expandable, and reconfigurable lunar spaceflight systems clearly requires electronic components that can provide robust operation without external thermal conditioning.

The AAPS SiGe task has as its goal the development and demonstration of extreme environment electronic components applicable to lunar robotic systems that possess distributed avionics architectures. Core to this effort is the use of low-cost, commercial SiGe Heterojunction Bipolar Transistors (HBTs) within Complementary Metal Oxide Semiconductor (CMOS) technology.⁹⁻¹³ Unlike other commercial off-the-shelf (COTS) integrated circuit technologies, SiGe offers unparalleled cryogenic temperature performance, radiation tolerance, wide temperature range capability, and optimal mixed-signal circuit design flexibility at the monolithic level. Other benefits include the ability to fabricate power efficient, multiple breakdown voltage, high-speed SiGe HBTs on the same piece of silicon wafer as high density Si CMOS circuits and passive components.

To ensure proper maturity of this technology, the SiGe task endeavors to deliver:

- Low-power, radiation tolerant (to 100krad), integrated SiGe BiCMOS mixed-signal (digital + analog + power) electronics for sensor/imager and actuator systems that can operate reliably across -180°C to +120°C, and under relevant radiation conditions.
- High-density packaging of these SiGe BiCMOS electronics components (with integrated passive components) which can operate reliably across -180°C to +120°C.
- Modeling and CAD tools for SiGe BiCMOS devices and packaging to accurately predict and simulate the electrical performance, reliability, and radiation tolerance of these SiGe BiCMOS mixed-signal circuits and packages across -180°C to +120°C.
- A development library of
- Definition and implementation of a general purpose Remote Electronics Unit (REU) prototype capable of operation across -180°C to +120°C and simultaneous relevant radiation conditions.

In pursuit of these goals, the SiGe task has been producing increasingly complex designs that successively build toward the fabrication of a final REU prototype system. The “CRYO” moniker is used to identify the progressive stages of the development effort. Completed in 2005, the first iteration of the CRYO series, CRYO 1, was a proof-of-concept fabrication run containing SiGe-based basic circuit building blocks such as operational amplifiers, digital-to-analog converters, and standard characterization and test structures. The final REU prototype system, the CRYO 5 design, will consist of a SiGe-based REU Sensor Interface (RSI) Application Specific Integrated Circuit (ASIC) and a Digital Control (RDC) ASIC chip. Both will be integrated into a single, environmentally tolerant package. This flight-ready REU system prototype will serve as a general purpose, extreme environment ready, sensors and control interface system-in-package for NASA missions. The planned verification and testing strategy will consist of characterization of the various SiGe mixed-signal components as a function of temperature, from -180°C to 120°C. Tests will also include radiation characterization to a total dose of at least 100 krad, life testing at the temperature extremes (-180°C and 120°C), and over-temperature part and package thermal cycle testing. Additional testing of components at cryogenic temperatures under radiation exposure will be used to evaluate the combined effects of temperature and radiation. When complete, the SiGe task will have matured a critical technology allowing many electronic components and data devices to be mounted such that they are exposed to the extremes of the space environment and no longer require the conditioning provided by the system’s warm box.

Initially scheduled to be delivered in 2009, the final REU prototype delivery was slipped until April 2010 to accommodate a refabrication and test of the RDC ASIC chip.

For purposes of testing the SiGe technology in the space environment, multiple flight experiments are underway which include SiGe-based electronic chips. Mounted on the MISSE-6 experiment are passive, unpackaged SiGe chips that function as a voltage reference. These circuits were protectively coated against atomic oxygen damage and tested prior to flight. Upon the retrieval of the MISSE-6 experiment, these circuits will be recovered and tested for operation. The NANOSAT program is another target for flying SiGe-based electronics. In cooperation with the Boeing Company, the SiGe team is planning to include an active, packaged version of the voltage reference circuit. And, in late 2009, an active, packaged SiGe-based control circuit, the CRYO 3a design, will fly as an integrated portion of a Boeing experiment on the MISSE-7 experiment platform.

The contract for this task is managed by NASA’s Langley Research Center with support from the Jet Propulsion Laboratory. The Georgia Institute of Technology is the prime contractor and leads a team made of multiple academic and industrial partners.

III. Conclusion

In response to the Constellation Program's need for environmentally hardened electronics and avionics, the AAPS technology development project is actively working to provide advancements in the areas of modeling of the radiation environment and its effect on advanced, modern electronics, FPGAs designed such that they are hardened against the radiation environment, High Performance Processors that will provide high efficiency, radiation hardened performance, Reconfigurable Computing capabilities that allow a single processor board to fulfill multiple functions, and SiGe-based electronics that allow operation in the low-temperature and radiation environments of the lunar surface. This overview paper provides a summary of each of these technology development tasks with an emphasis on the significant progress of the past fiscal year and identification of the additional development milestones planned for the coming fiscal year.

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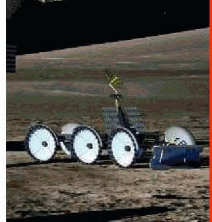


Exploration Technology Development Program

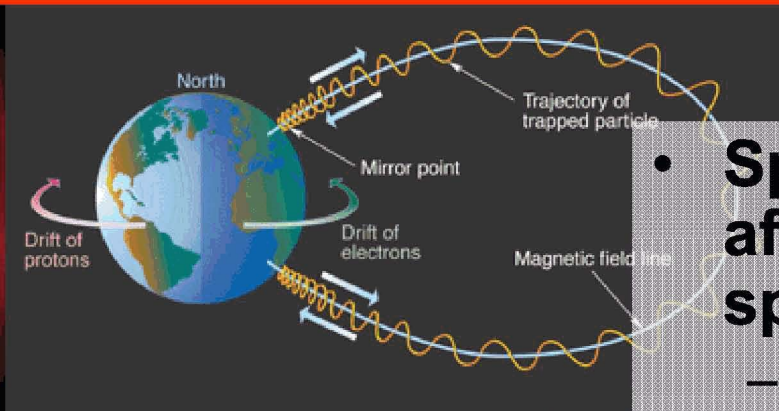
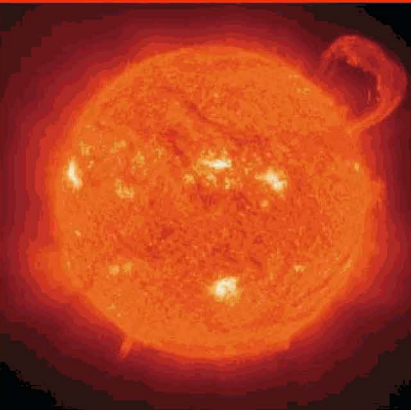
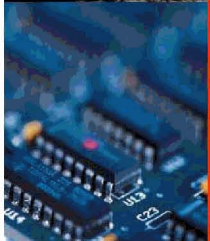
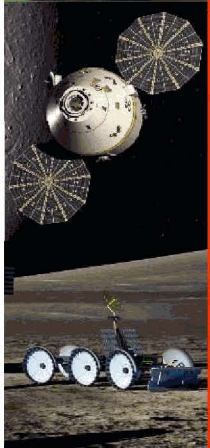
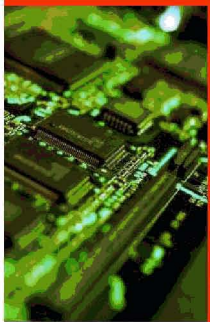
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NASA Goddard Space Flight Center, Greenbelt, MD 20771
John D. Cressler
Georgia Institute of Technology, Atlanta, GA 30332-0250

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The Radiation Environment



- **Space Radiation affects all spacecraft.**

- Spacecraft electronics have a long history of power resets, safing, and system failures due to:

- Long duration exposures,
- Unpredictable solar proton activity,
- Ambient galactic cosmic ray environment.

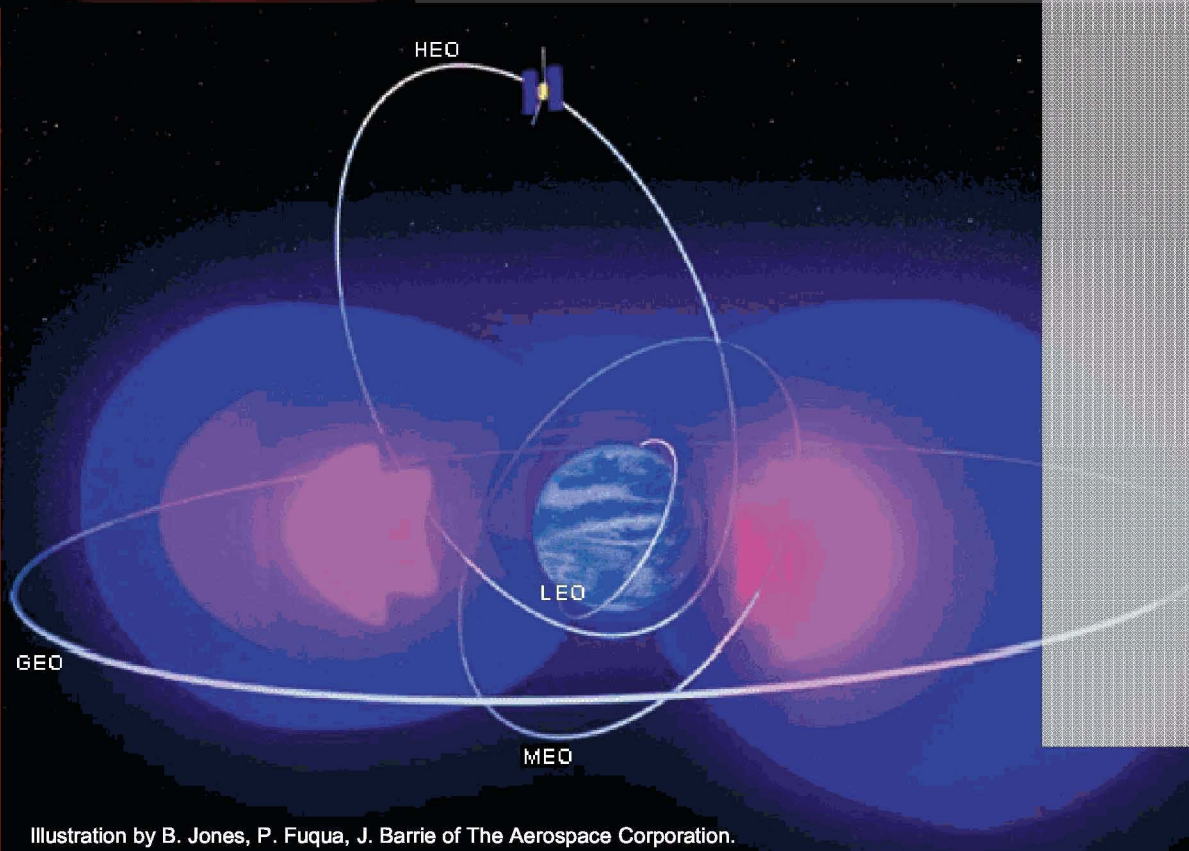
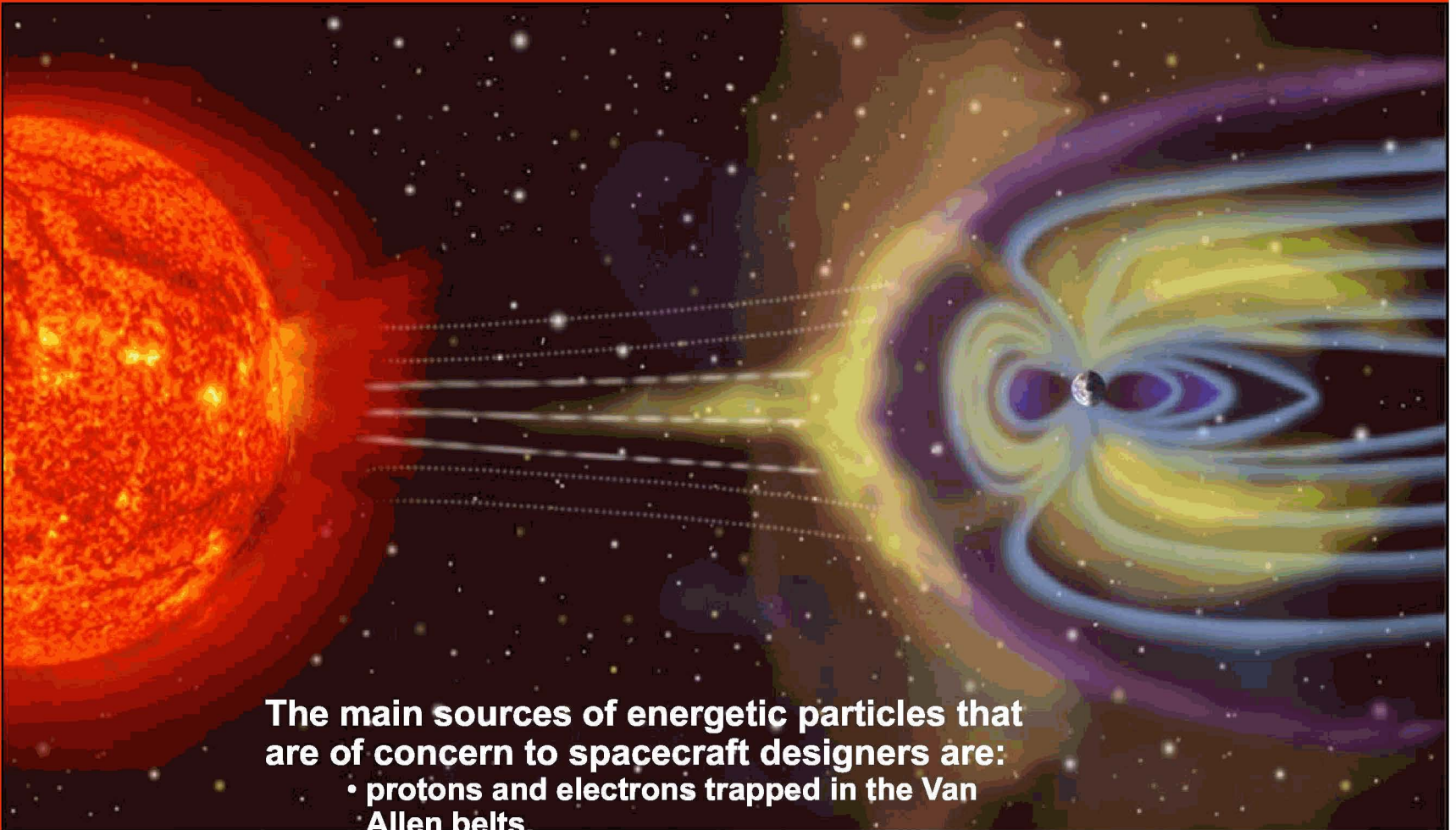
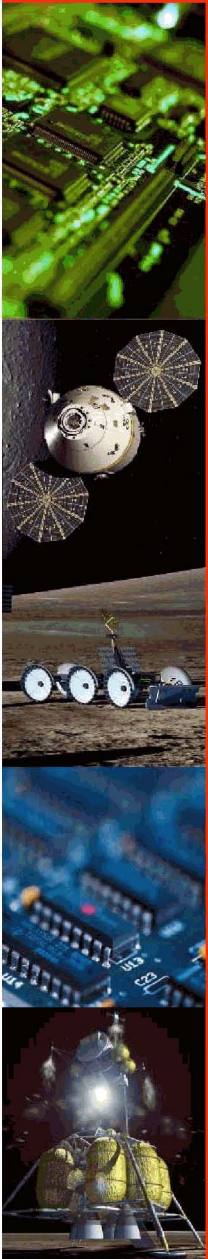


Illustration by B. Jones, P. Fuqua, J. Barrie of The Aerospace Corporation.

Space Environment Radiation Sources

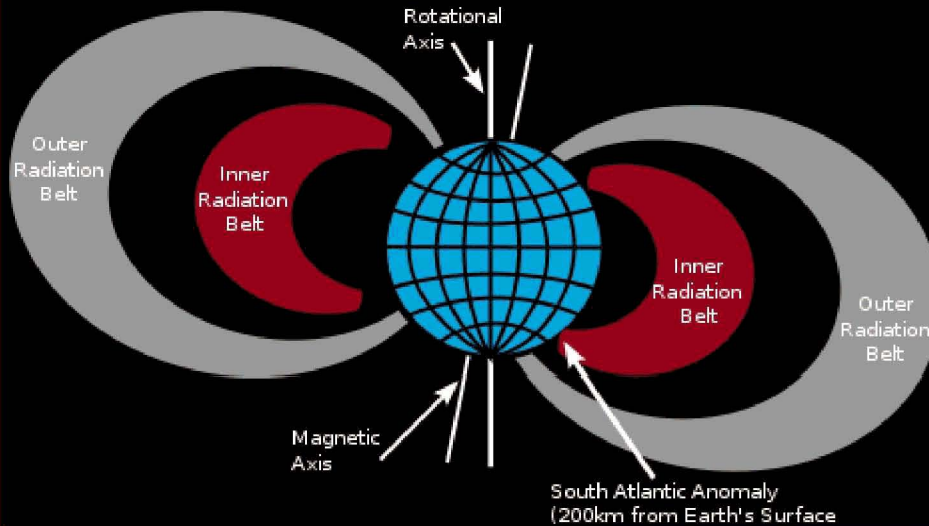


The main sources of energetic particles that are of concern to spacecraft designers are:

- protons and electrons trapped in the Van Allen belts,
- heavy ions trapped in the Earth's magnetosphere,
- cosmic ray protons and heavy ions of multiple elements, and
- protons and heavy ions from solar flares.

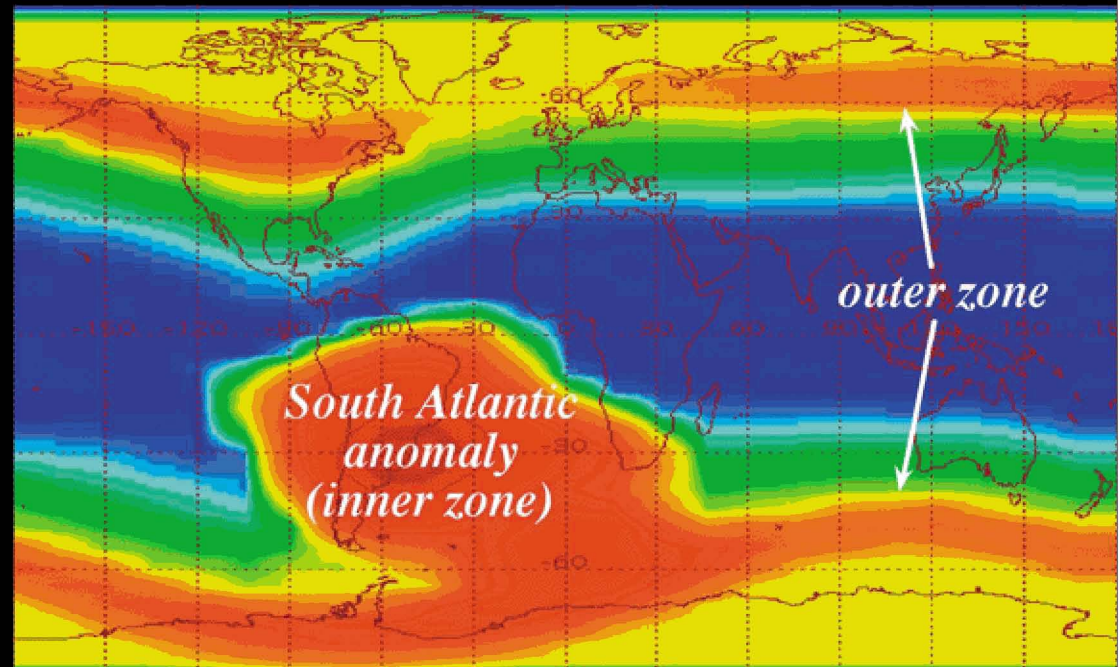


South Atlantic Anomaly

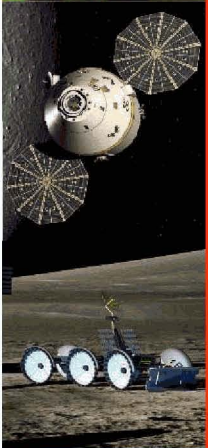
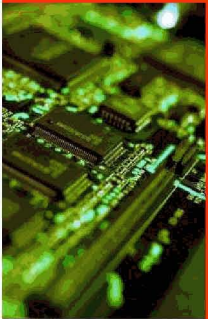


Earth's magnetic field is tilted with respect to its rotational axis, currently about 11 degrees.

Count rate of protons and electrons greater than 0.5 MeV in low Earth orbit measured by the NASA/SAMPEX satellite.



Maximum Energies of Particles



Particle Type

Maximum Energy*

Trapped Electrons

10s of MeV

Trapped Protons &
Heavier Ions

100s of MeV

Solar Protons

100s of MeV

Solar Heavy Ions

GeV

Galactic Cosmic Rays

TeV and beyond!

* For engineering applications

Six ground-based experiments have reported a total of 22 events $>10^{20}$ eV (super-Greisen-Zatsepin-Kuzmin (GZK) events) during the last 40 years:

- 1 event from Volcano Ranch,
- 4 from Haverah Park,
- 1 from Yakutsk,
- 1 from Fly's Eye,
- 8 from the Akeno Giant Air Shower Array (AGASA), and
- 7 from the preliminary High-Resolution Fly's Eye Experiment (HiRes-1).

This corresponds to a flux of about one event per km² per century.

Radiation Effects on Electronics



Long-Term Electronic Damage Mechanisms:

Total Ionizing Dose (TID) Damage:

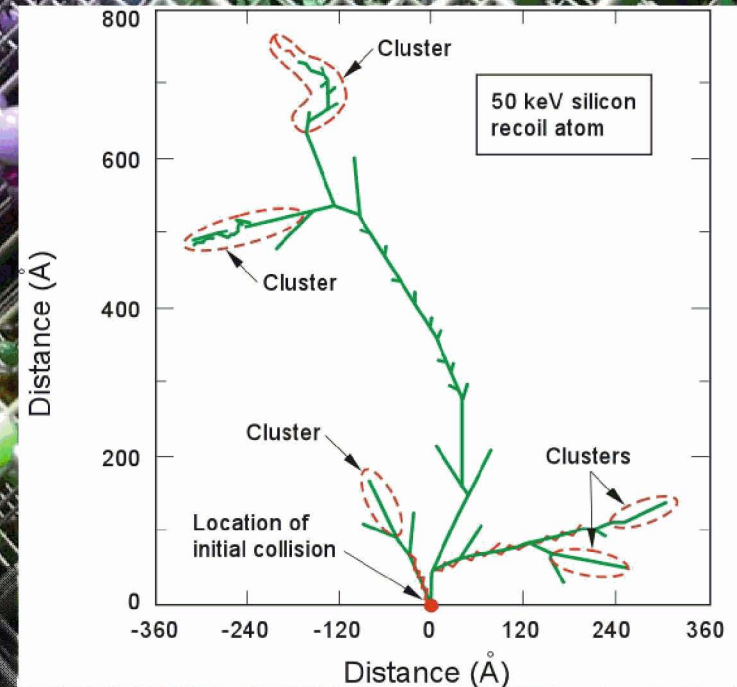
- Radiation causes lattice ionization, generating migratory carrier traps.
- Traps can permanently collect near interfaces, causing leakage currents and increased threshold voltage shifts.
- Multiplied by millions, leakage currents can cripple a device.

Cumulative Lattice Displacement Damage:

- Clustered atom displacement within the crystal lattice causes minority carrier lifetime degradation.
- Bipolar transistors operate using minority carriers, so carrier recombination can cause performance degradation.
- High-energy radiation particles can actually anneal some lattice problems but dose is uncontrollable in the space environment.

Enhanced Low Dose Rate Sensitivity (ELDRS):

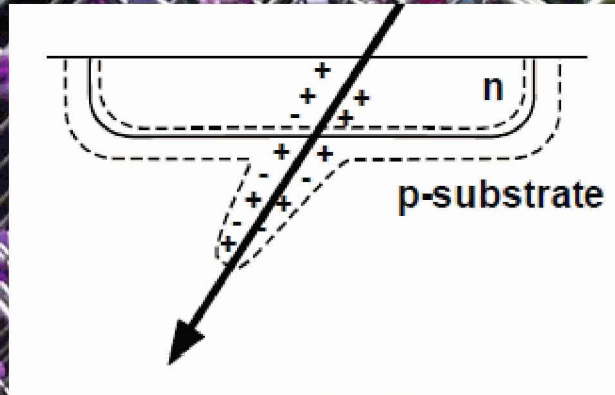
- Affects linear bipolar devices.
- Damage often done in unpowered mode.



Radiation Effects on Electronics

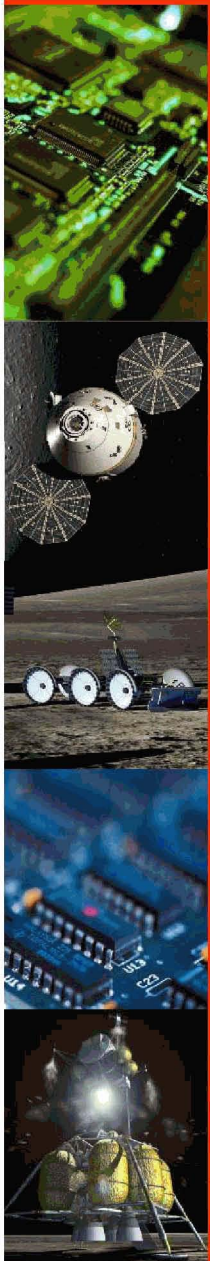


Short-Term Electronic Damage Mechanisms:

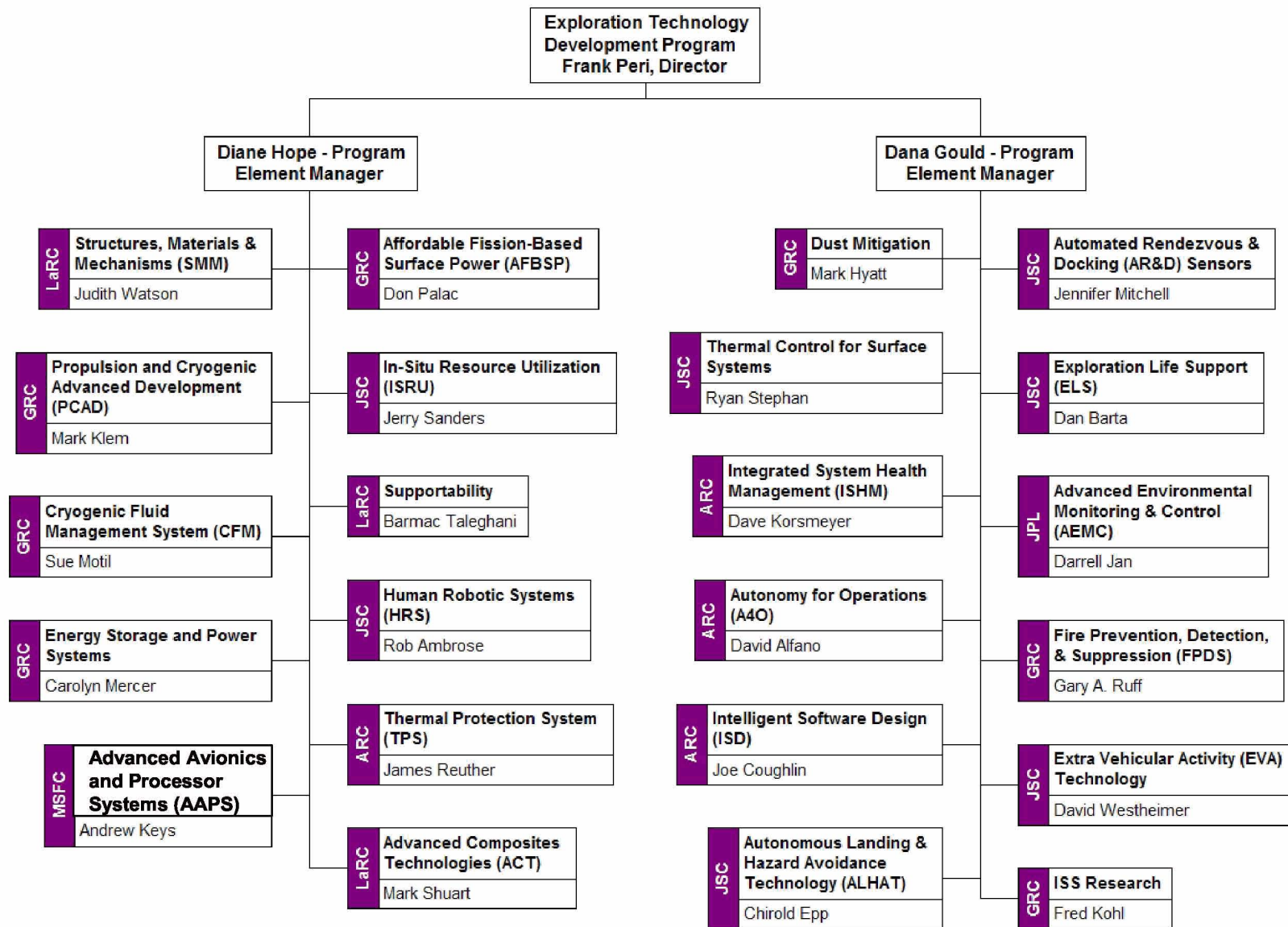
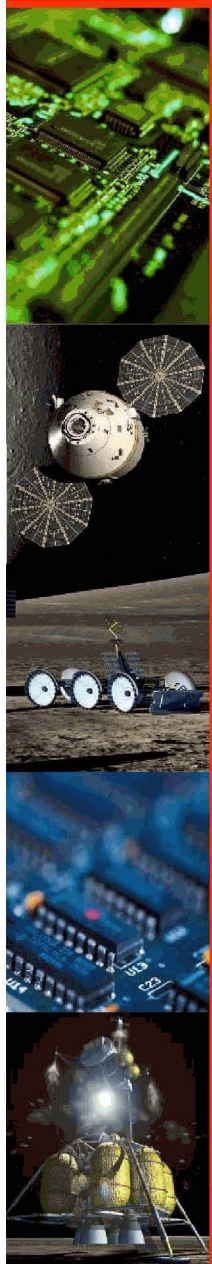


- **Transient Ionization Effects:**

- High energy particles ionize the surrounding atoms, generating charges that propagate and collect. In digital circuitry, this can result in a Single Event Effect (SEE). Many types of SEEs have been characterized:
 - **Single-Event Upsets (SEU):** transient state changes of memory or register bits caused by a single ion interaction.
 - **Single-Event Latch up (SEL):** high energy ion or proton forces a latched state that is held until power cycled. If the state causes high current flow, permanent damage can occur.
 - **Single-Event Transient (SET):** charge collected from an ionization event results in a spurious signal propagating through the circuit.
 - **Single-Event Induced Burnout (SEB):** occurs in power MOSFETs when ionization causes the breakdown voltage to be exceeded and high current risks destroying the device.
 - **Single-Event Gate Rupture (SEGR):** occurs in power MOSFETs when a heavy ion hits the gate region while a high voltage is applied to the gate, causing a short through the gate oxide and permanent device destruction.



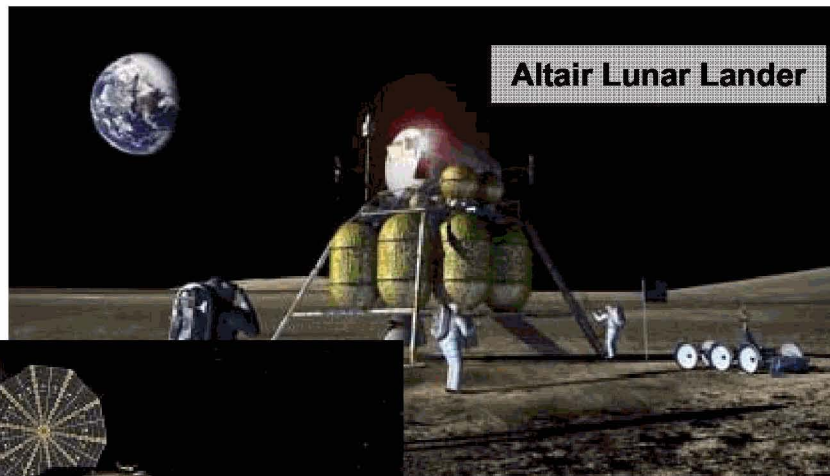
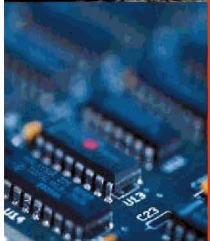
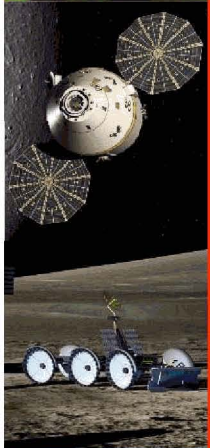
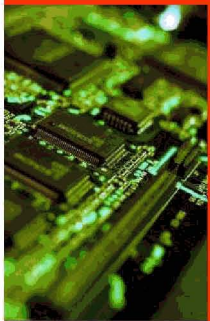
Exploration Technology Development Program Organizational Chart



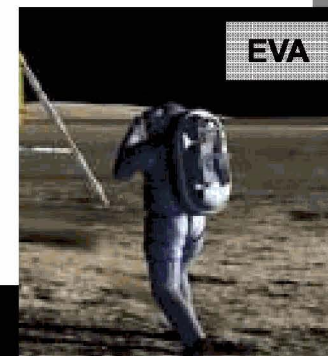
AAPS Supports Multiple Constellation Projects



- **AAPS's products are developed in response to the needs and requirements of multiple Constellation program elements, including:**
 - Ares V Crew Launch Vehicle (Earth Departure Stage),
 - Orion Crew Exploration Vehicle (Lunar Capability),
 - Altair Lunar Lander,
 - Lunar Surface Systems,
 - Extra Vehicular Activity (EVA) elements,
 - Future applications to Mars exploration architecture elements.



Altair Lunar Lander



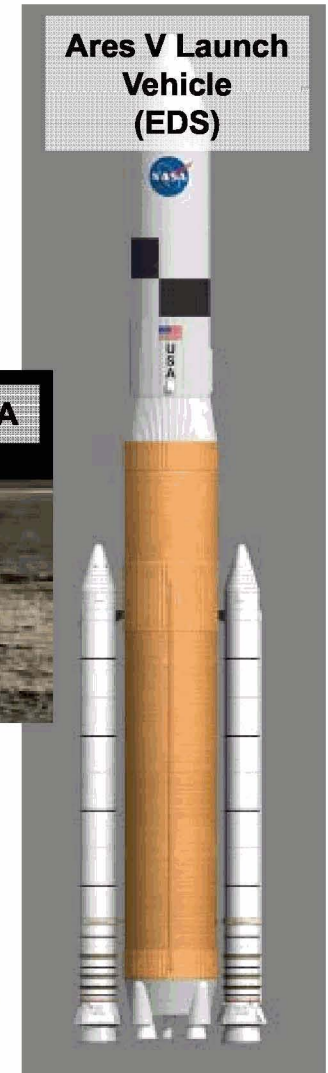
EVA



Orion Crew Exploration Vehicle



Lunar Surface Systems



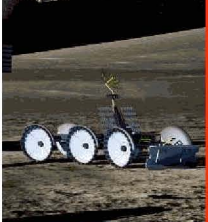
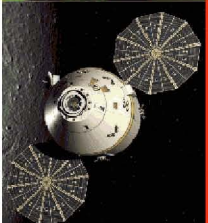
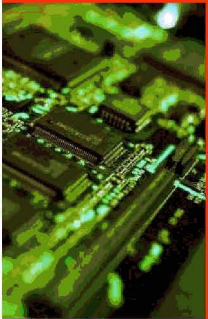
Ares V Launch Vehicle (EDS)

AAPS Objective and Project Goals

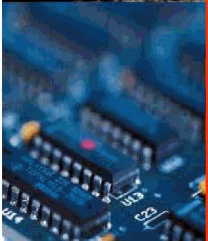
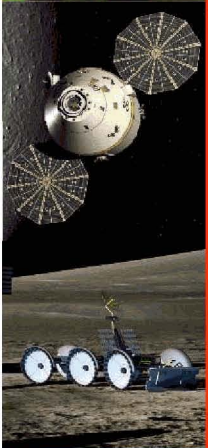
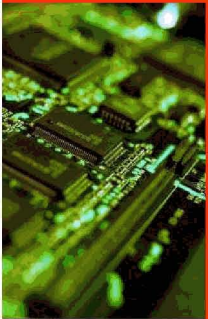


The **Advanced Avionics and Processor Systems (AAPS)** project expands the current state-of-the-art in spacecraft avionics components and processor systems to develop high performance devices for long duration exposure to the space and lunar environments.

- The specific **project goals** of the AAPS project are to foster technology development efforts in radiation-hardened electronics possessing these associated capabilities:
 - improved Total Ionization Dose (TID) tolerance,
 - reduced Single Event Upset (SEU) rates,
 - increased threshold for Single Event Latch-up (SEL),
 - increased sustained processor performance,
 - increased processor efficiency,
 - increased speed of dynamic reconfigurability,
 - reduced operating temperature range's lower bound,
 - increased the available levels of redundancy and reconfigurability, and
 - increased the reliability and accuracy of radiation effects modeling.



Customer Requirements and Needs

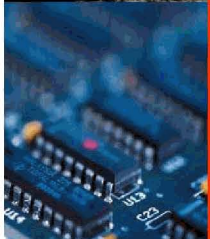
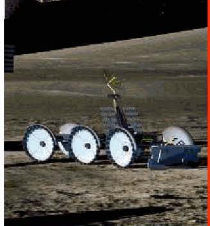
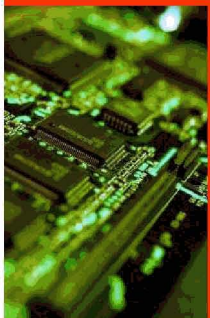


- AAPS is a “**requirements-pull**” technology development effort.
- AAPS is a “**cross-cutting**” technology, serving a broad base of multiple project customers within Constellation.
- Constellation Program requirements for avionics and electronics continue to evolve and become more defined.
- AAPS develops products per **derived requirements** based on the Constellation Architecture’s Level I and Level II requirements defined to date.

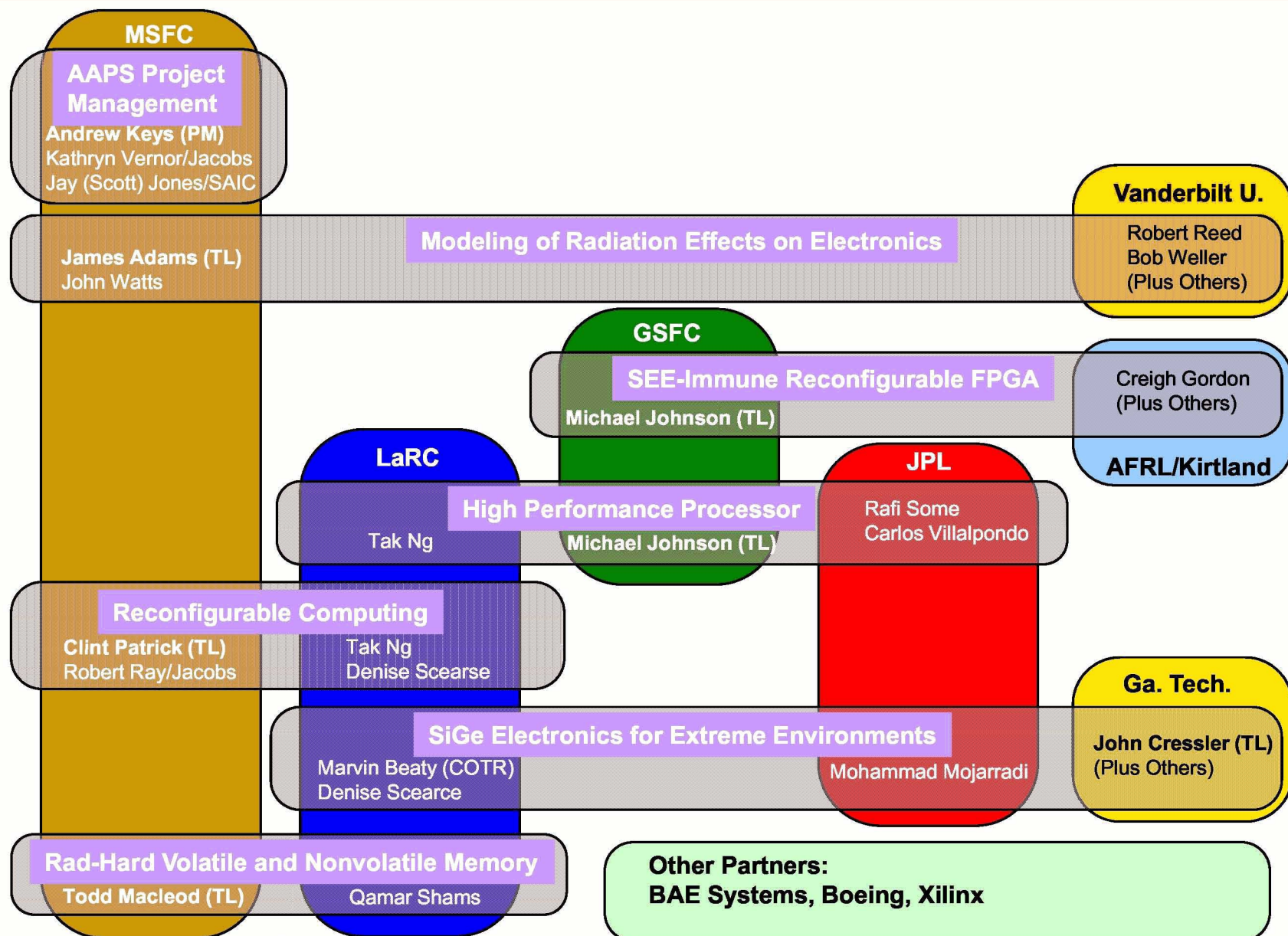
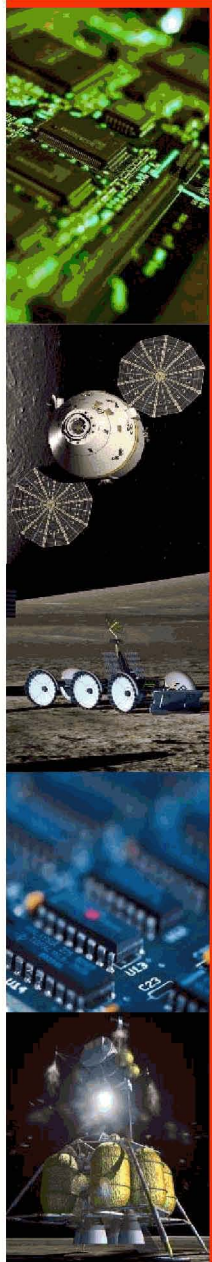
AAPS Tasks



- **Specifically, the AAPS tasks for FY09 are:**
 - Model of Radiation Effects on Electronics (MREE),
 - Lead Center: MSFC
 - Participants: Vanderbilt University
 - Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF),
 - Lead Center: GSFC
 - Participants: AFRL, Xilinx
 - Radiation Hardened High Performance Processors (HPP),
 - Lead Center: GSFC
 - Participants: LaRC, JPL, Multiple US Government Agencies
 - Reconfigurable Computing (RC),
 - Lead Center: MSFC
 - Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments.
 - Lead Center: LaRC
 - Participants: Georgia Tech. leads multiple commercial and academic participants.
 - Radiation-Hardened Volatile and Non-Volatile Memory
 - Lead Center: MSFC
 - Participants: LaRC, Multiple Vendors



AAPS Project Management Structure

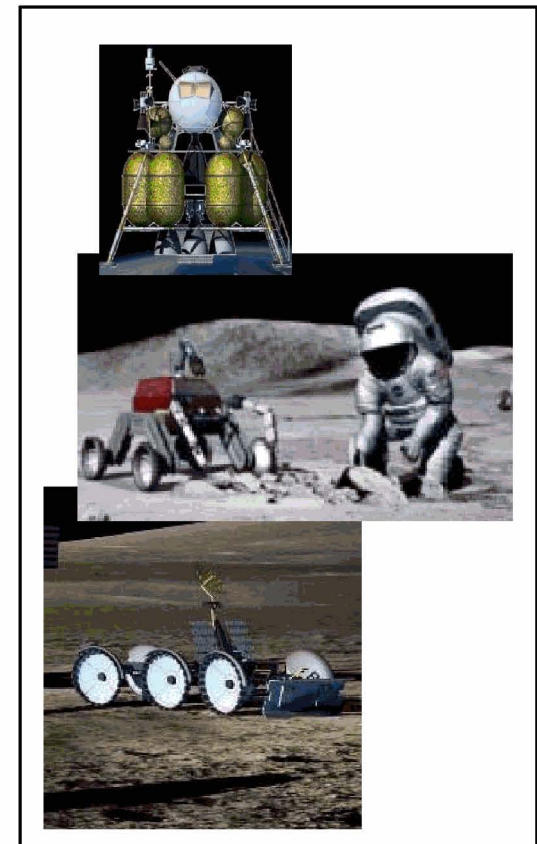
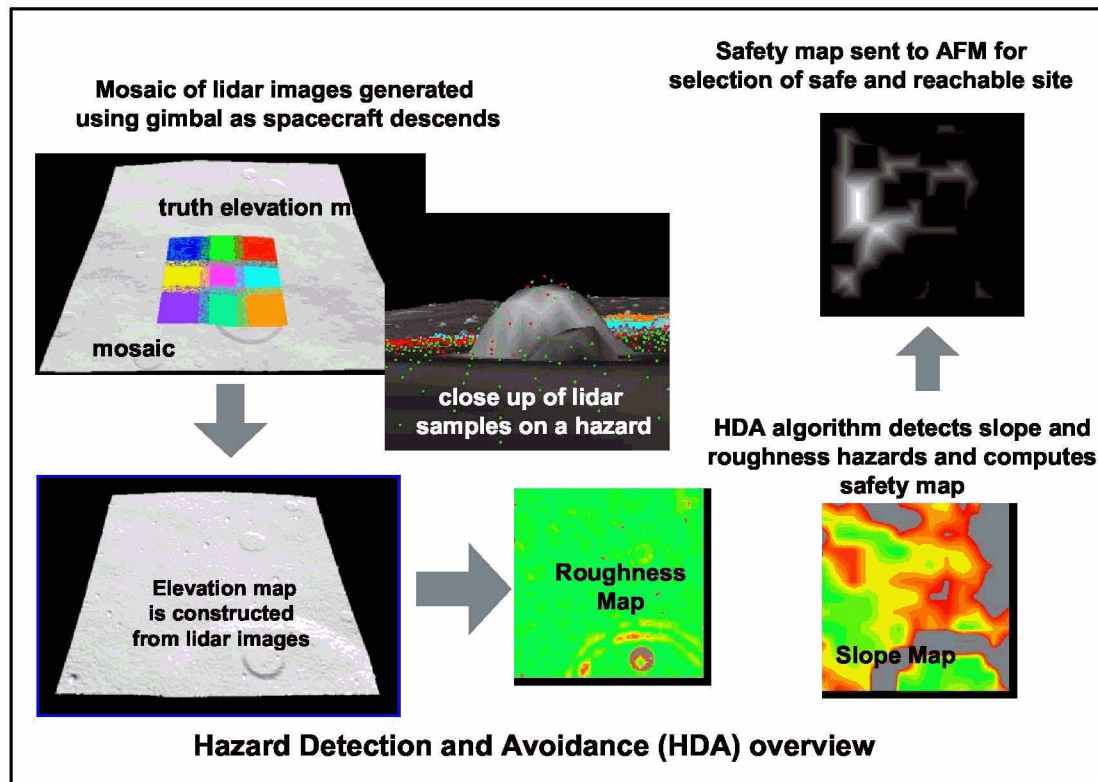


HPP FY09 Accomplishments



Objective:

- Assess performance and susceptibilities of high-performance processor options
 - Focus on HyperX (Hx) and Tiler options
- Recommend high performance processor for ALHAT (and other) capabilities
- Assess options for (ultra) low-power embedded processors for LSS, EVA capabilities

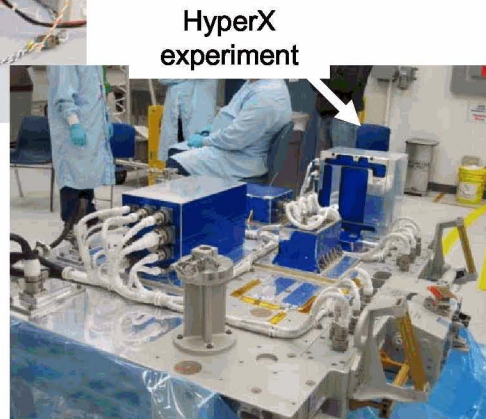
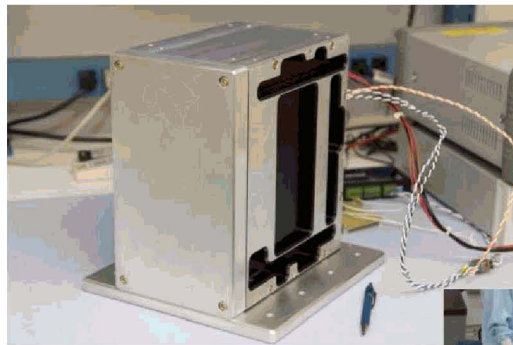
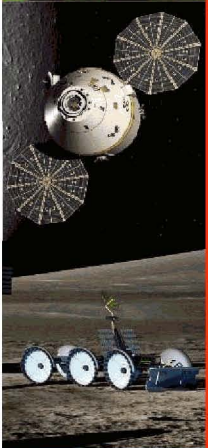
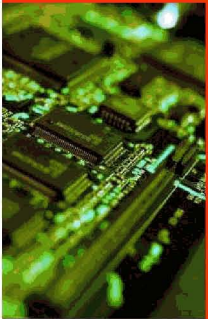


HPP FY09 Accomplishments



Key Status /Accomplishment/Deliverable/Milestone

- Capability-specific (ALHAT) and general processor performance assessments are ongoing
- Hx radiation susceptibilities and effectiveness of mitigation strategies were assessed via beam tests
- Hx processor technology was integrated onto MISSE7 payload for STS-129 ISS deployment (Nov. 2009)
- Recently developed radiation-hardened general purpose processor (LEON-3FT) was also integrated onto MISSE7 payload. First space-flight processor deployment.
- Tracking / influencing development of ultra-low power embedded processor development activities (SBIR, Air Force Research Laboratory)



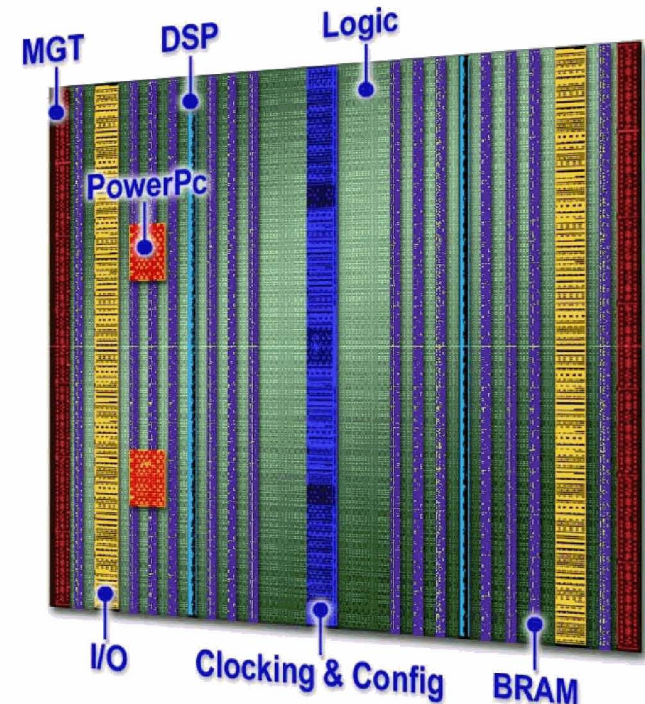
SIRF FY09 Accomplishments



Key Status

/Accomplishment/Deliverable/Milestone

- FX1 engineering prototype component was fabricated and is under test
- The FX1 chip has been successful in achieving its goals
 - No functional anomalies have been found at all
 - The design-hardened chip should run at full commercial speed
- Customers are strongly urging Xilinx and AFRL to come out with a product quickly
- Program will likely proceed to productization with only minor changes to FX1



**The SIRF program is lead and majority funded by the
Air Force Research Laboratory**

Memory FY09 Accomplishments



Objective:

Develop a Memory Testing Laboratory at LaRC to conduct testing of memory devices for use in Exploration Projects

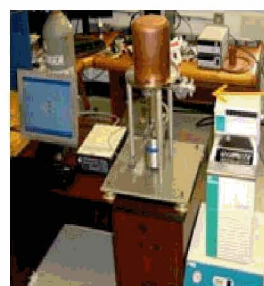
Key Accomplishment:

- May/2009

Significance:

The Memory Test Laboratory was completed and started testing memory devices. It has the capability of characterizing several different memory technologies. It can also perform thermal testing at high temperatures and extremely low temperatures with the use of a helium cryostat. This facility is now on-line and has started testing Silicon-On-Insulator technology memory devices.

Pictures from LaRC Memory Test Lab

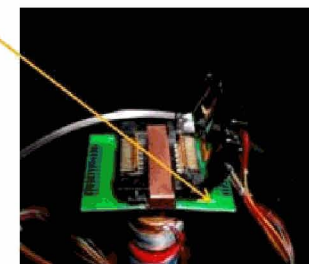


Cryostat System

Cold Head



Electronics Board Sockets for Memory Devices

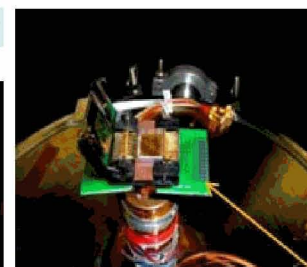
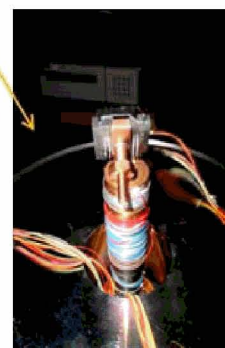


Thermally Conducting Adapter for Memory Devices

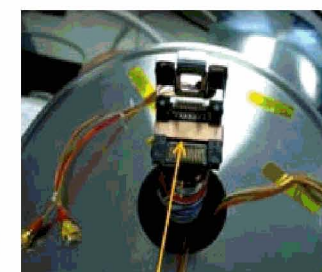
Cold Head Top



Backside of Memory Adapter



Thermally Conducting Memory Characterization Set-up Arrangement on Top of Cold Head



Memory FY09 Accomplishments



Objective:

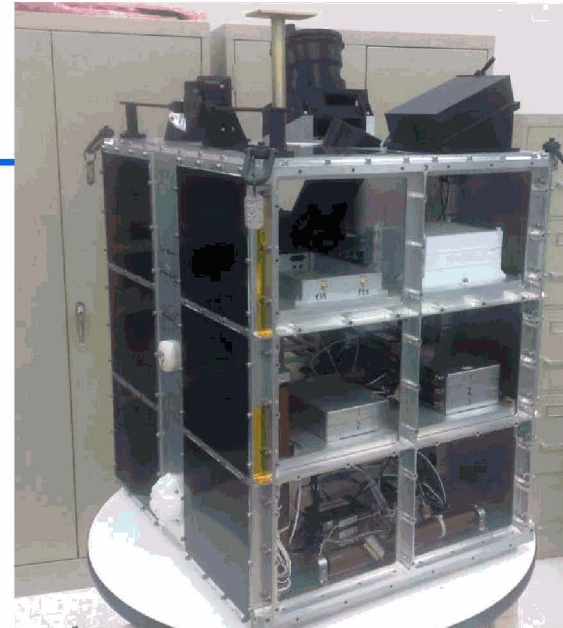
Develop the Memory Test Experiment for the Fast and Affordable Science and Technology Satellite.

Key Accomplishment:

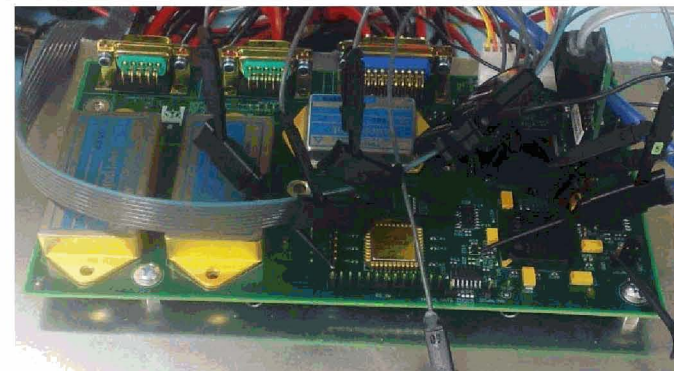
- June 2009

Significance:

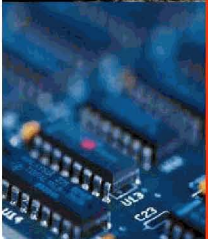
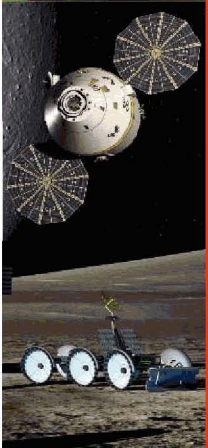
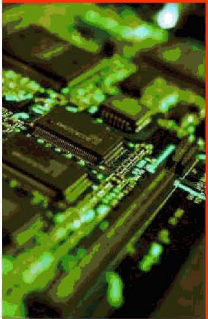
- The Memory Test Experiment (MTE) design and development was completed. The experiment was designed and developed by MSFC civil servants developing the FASTSAT avionics. This experiment contains a Ferroelectric based memory circuit that will be tested during the year long flight of the Fast and Affordable Science and Technology Satellite (FASTSAT). Launch is scheduled for February 2010. The test consists of writing and reading test patterns into the memory device and reporting and errors detected. The MTE is incorporated into the telemetry board for the satellite.



**FASTSAT
Satellite**



**Telemetry Board containing the Memory
test Experiment**



Memory FY09 Accomplishments



Objective:

Radiation Testing the Memory Test Experiment for the Fast and Affordable Science and Technology Satellite at Indiana University.

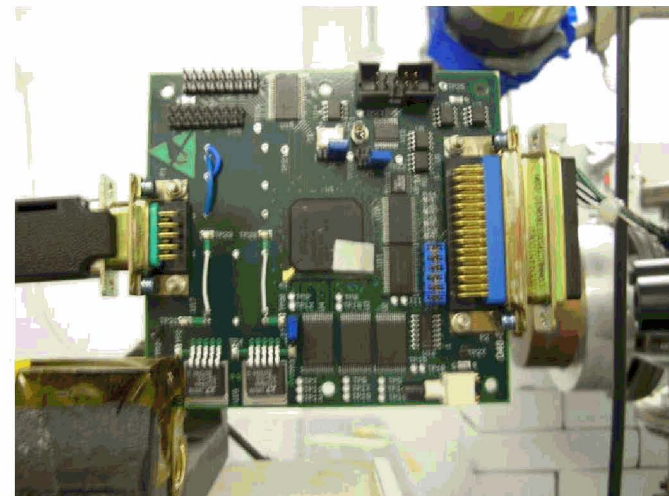
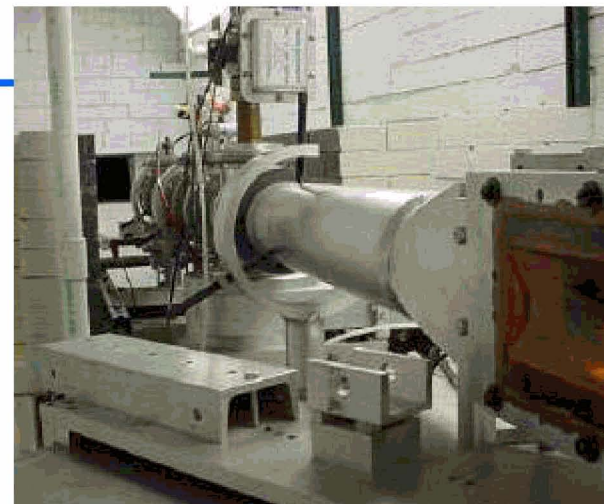
Key Accomplishment/:

- July 2009

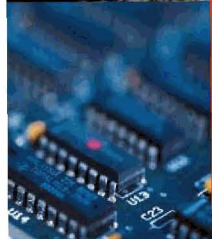
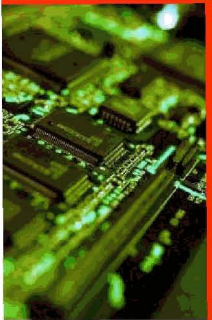
Significance:

- The Memory Test Experiment (MTE) was tested under proton radiation at Indiana University. The test was conducted to verify the FASTSAT avionics. The MET is incorporated into the telemetry board of the FASTSAT avionics. The test consisted of putting the avionics boards into the proton beam and testing them with power on and off. Energy levels were up to 200 KeV with the dose of 115 rads. The telemetry board passed the radiation testing and no errors were recorded in the ferroelectric memory devices.

Telemetry Board



RC Development Approach



RC Development Concentrates on Three Interrelated Areas:

**Internal Modularity
External Modularity
Fault Management**

RC FY09 Accomplishments



Objective:

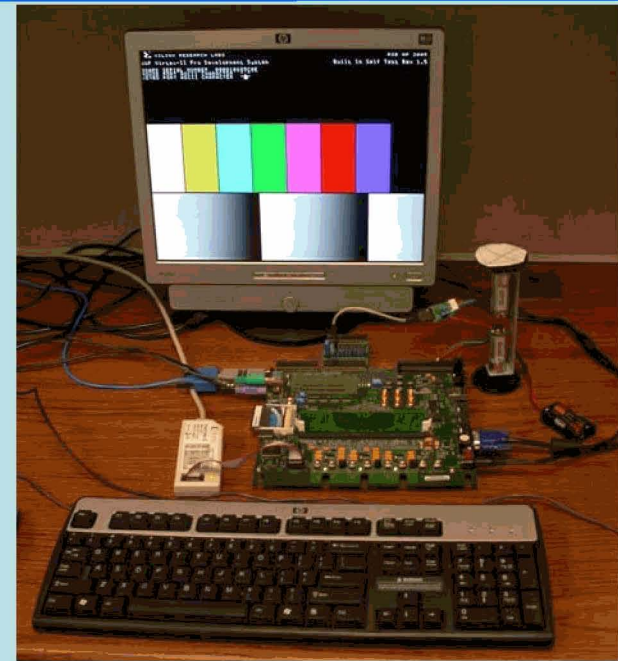
Radiation-Hardened Electronics for Space Environments (AAPS) Reconfigurable Computing (RC) task Demonstration #1 was to show basic manual reconfiguration of the test hardware into three substantially different computing resources.

Key Accomplishment/Deliverable/Milestone:

- 13 January 2009
- Basic concepts of RC were showcased at MSFC. Coupled with the demo was an informative slideshow with background information, a description of goals and activities of the demonstration itself, and plans for future research and demonstrations of progressively more complex RC concepts and capabilities. This demo concentrated on very basic manual reconfiguration of the test hardware into three substantially different computing resources. These were: microprocessor, digital signal processor and motor control/feedback setups.

Significance:

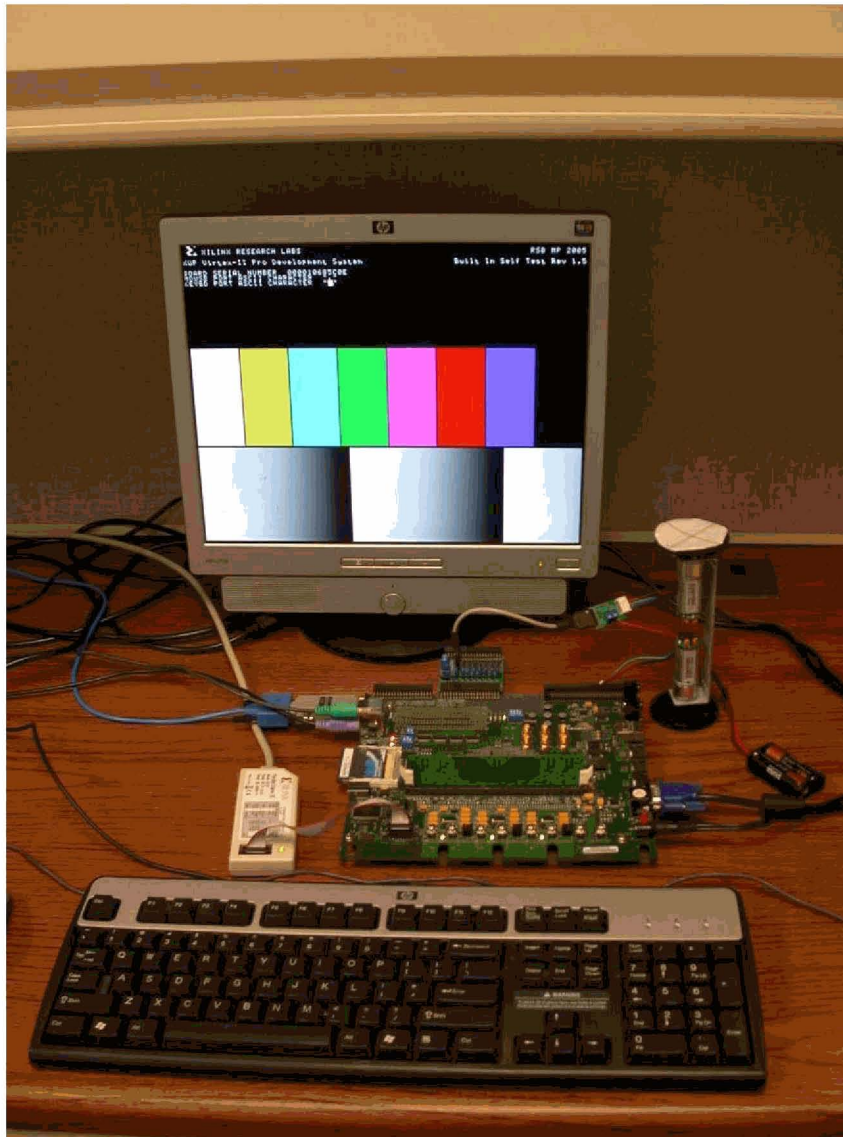
- Establishes a foundation for RC upon which further demonstrations of internal reconfiguration, external reconfiguration, and fault recognition functions will build.
- Provides crucial publicity of RC efforts within NASA and the technical community at large; weighs heavily in efforts to garner significant technical and fiscal support for RC.



Shown: Hardware for RC Demo #1

RC Demonstration #1

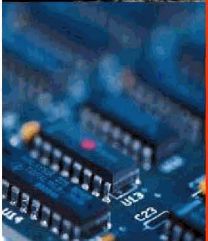
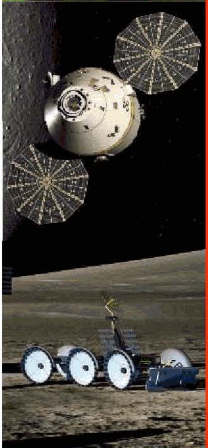
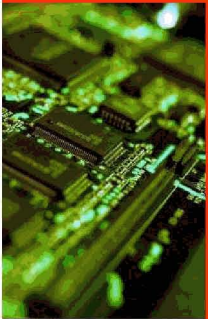
Internal Modularity



- **Objectives**
 - **Proof of Concept: Basic Reconfigurability (“Increased Internal Reusability”)**
 - **Demonstrate multiple discreet configurations separately**
- **Configurations**
 - **μ P: Turing Machine**
 - **DSP: Video FFT**
 - **μ C: Motor Control and Feedback**
- **MSFC, January 13, 2009**

RC Demonstration #2

External Modularity



- **Objectives**

- **Proof of Concept: External Reconfigurability (“Increased External Reusability”)**
- **Demonstrate multiple discrete configurations using the same FPGA board**
- **Will physically move a PC/104 board through three configurations**

- **Configurations**

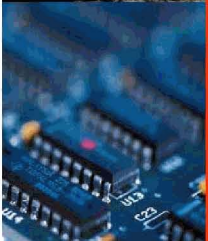
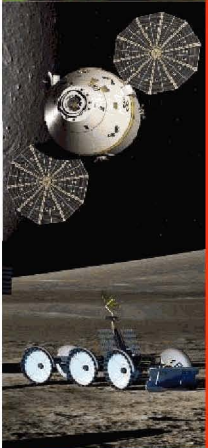
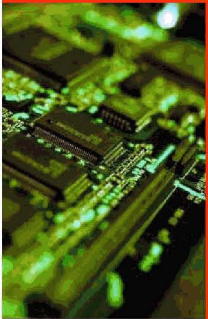
- **iRobot Create + Camera**
- **Closed-Loop Fluid Transfer**
- **Sensor Interface**

- **Largely developed by Robotics Academy students**

- **MSFC, Fall 2009**

RC Demonstration #2

iRobot with Camera



Ingredients

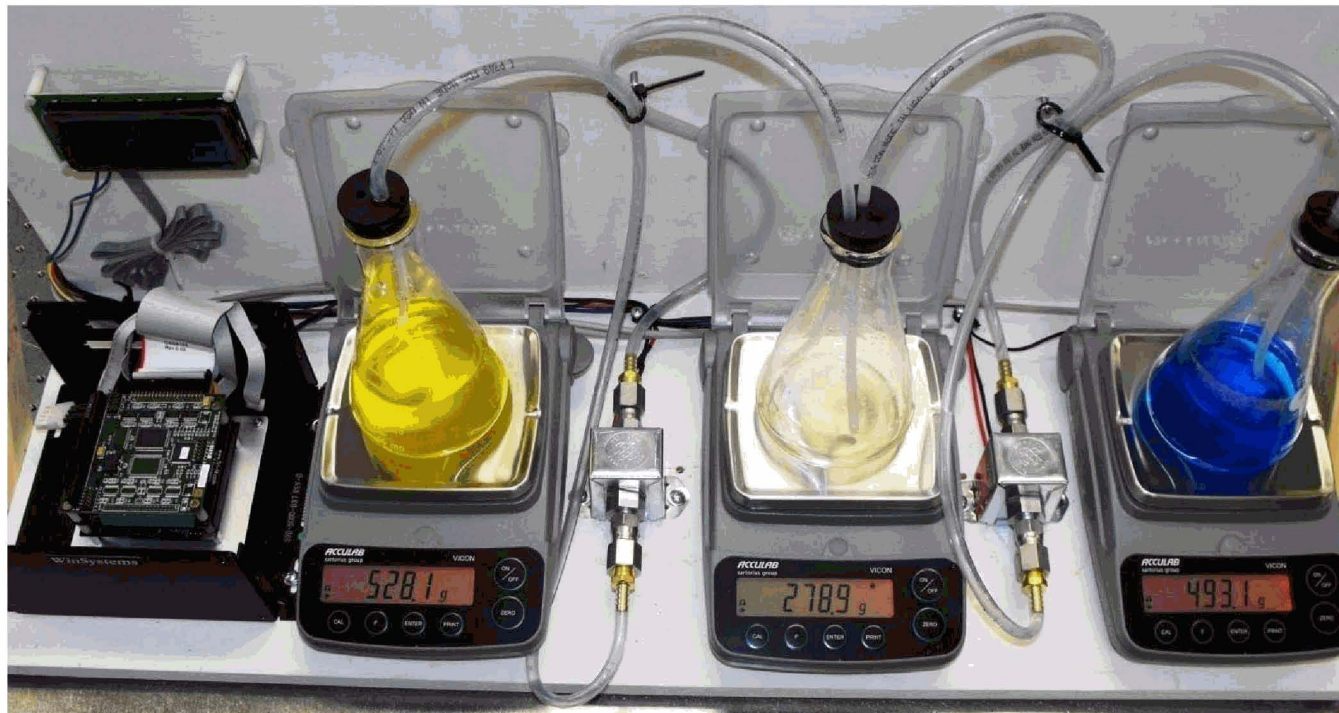
- iRobot Create educational robot
- PC/104 Xilinx Virtex II board
- PC/104 PixelSmart Frame Grabber
- PC/104 Quad-UART (RS232) board
- PC/104 12V Power Supply board

Demonstration

- A volunteer will place a square on the wall of a particle board pen.
- The robot will position itself in the center of a pen, then search the walls of the pen for the square.
- If found, the robot will approach the square and play a “happy” song.
- If not found, the robot will play a “sad” song.

RC Demonstration #2

Closed-loop Fluid Transfer

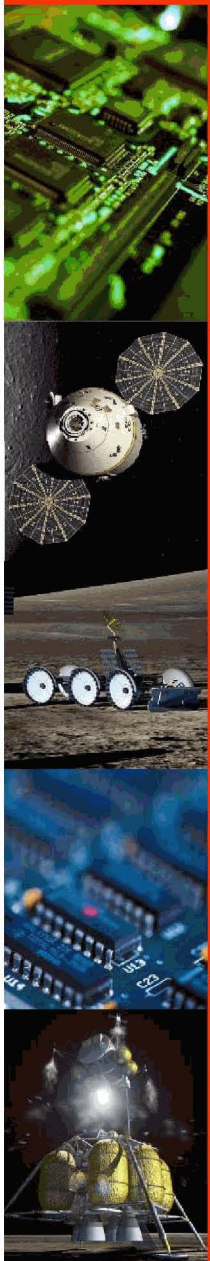


Ingredients

- PC/104 Xilinx Virtex II board
- PC/104 Quad-UART (RS232) board
- PC/104 12V Power Supply board
- PC/104 12V Relay board
- Two automotive fuel pumps
- RS-232 Laboratory scales

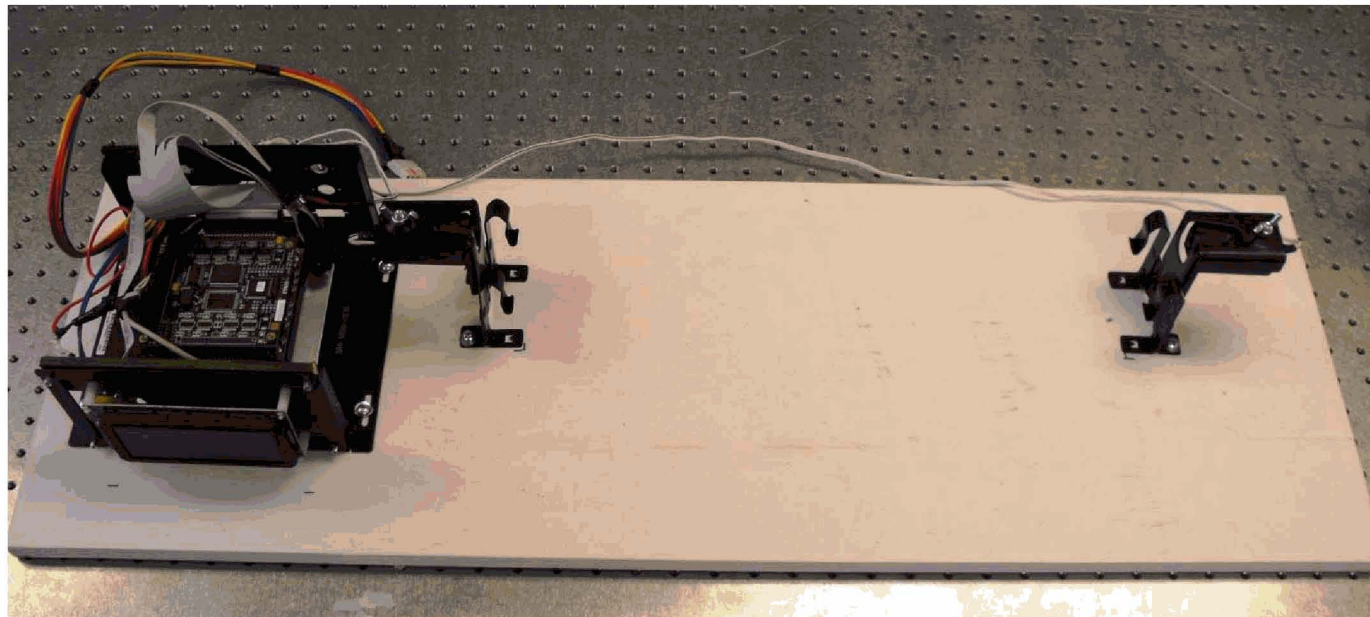
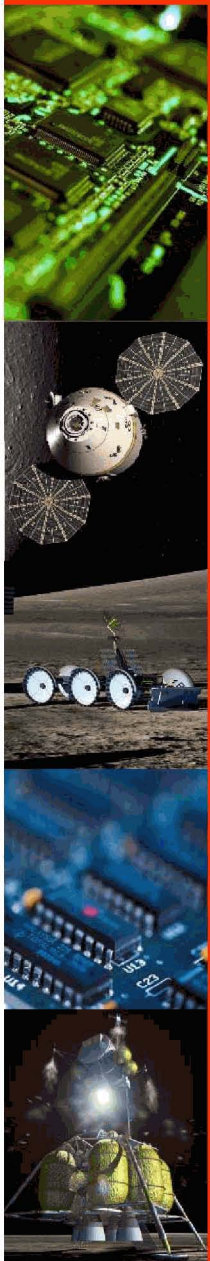
Demonstration

- Have a volunteer place unequal amounts of blue and yellow fluid into two beakers.
- Transfer equal amounts of blue and yellow fluid to produce green fluid (water and food coloring).



RC Demonstration #2

Sensor Interface



Ingredients

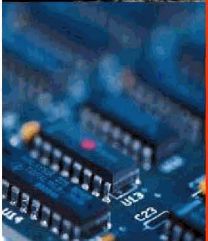
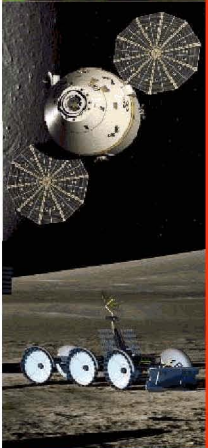
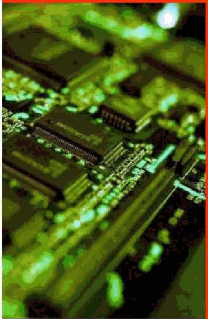
- PC/104 Xilinx Virtex II board
- PC/104 Quad-UART (RS232) board
- PC/104 12V Power Supply board
- PC/104 12V A/D converter board
- Photoelectric Infrared sensor (garden variety garage door safety sensor)

Demonstration

- Have a volunteer interrupt the beam between the emitter and sensor.
- Alert the Fault Detection, Diagnosis, and Response (FDDR) computer system of the interruption via RS-232.

RC Demonstration #3

Fault Management



- **Objectives**

- **Proof of Concept: Fault Management (“Failure Recovery”)**
- **Demonstrate the ability to recover from radiation-induced hardware failures**

- **Configuration**

- **Small form factor “SiRF-board”**
- **Four soft-processors in TMR+1 configuration, ala AP-101S)**
- **Execute one or more applications from Demonstration #1 or #2**
- **Induce failure via fault injection (synthetic)**
- **Induce failure via various ion beams at the TAM cyclotron**

- **MSFC, Fall 2010+**

- **Schedule dependent upon Xilinx part availability**
- **Schedule dependent upon board development activities**
- **Scope dependent upon coordination with NEPP/TAM**

MREE FY09 Accomplishments



Objective:

Develop a revised model for estimating radiation effects on spacecraft electronics.

Motivation for this Task:

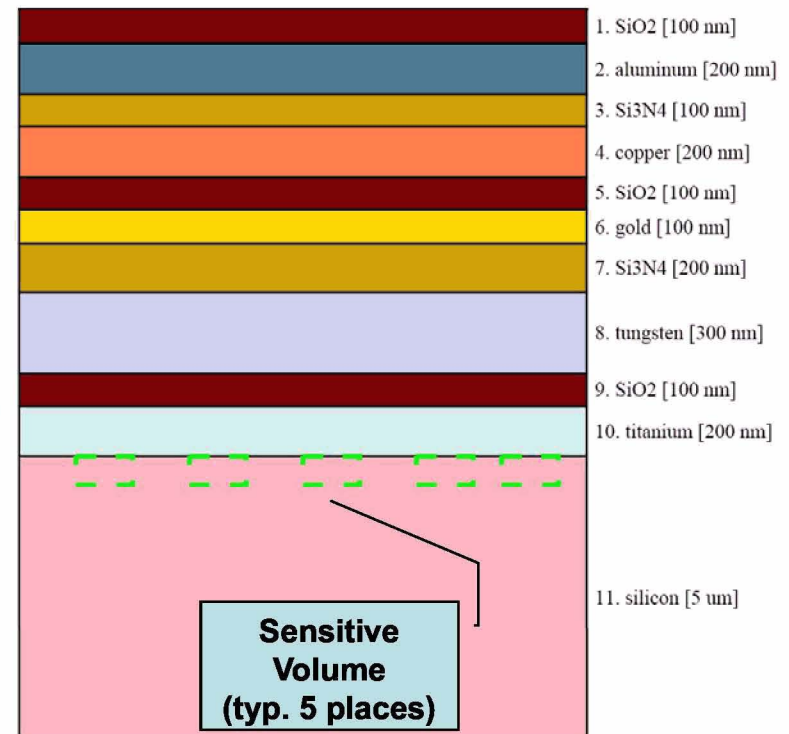
- The paradigm used in CREME96 and other models of that generation do not account for the feature sizes and complexities of modern electronic components.

Key Accomplishment/Deliverable/Milestone:

- 27 February 2009
 - Completed Maturation Plan
- 31 March 2009
 - Selected Revised Cosmic Ray Model
- 2 April 2009
 - Charge transport and collection models defined
- 1 June 2009
 - Legacy CREME96 Model On-line at Vanderbilt

Significance:

- Well defined plan for maturing the revised model
- Selected the most accurate galactic cosmic ray model by comparison with an extensive database.
- Developed a model for charge transport and collection by a microelectronic circuit following an ionizing particle strike that approximates a full TCAD calculation
- Put CREME96 on line at Vanderbilt University in order to preserve access to it after the NRL host goes down.



**CRÈME-MC Device Model from the
Vanderbilt WWW Site**

<https://creme-mc.isde.vanderbilt.edu/>

SiGe Objectives / Approach



“SiGe Integrated Electronics for Extreme Environments”

Objective:

Develop and Demonstrate Extreme Environment Electronic Components Required for Distributed Architecture Lunar / Martian Robotic / Vehicular Systems Using SiGe Technology

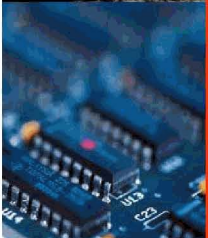
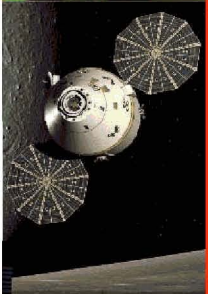
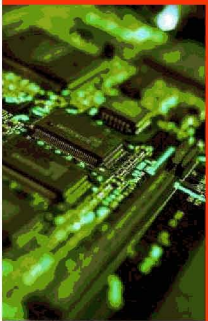
Extreme Environment Requirements: (e.g., Lunar)

- +120C (day) to -180C (night) + cycling
- radiation (TID + SEE tolerant, SEL immune)

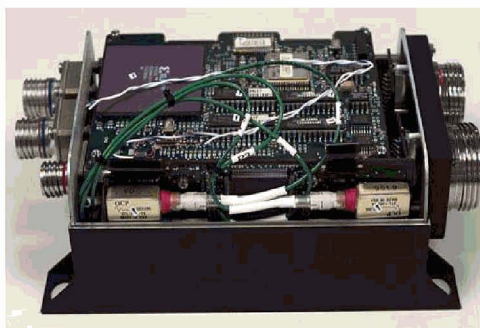
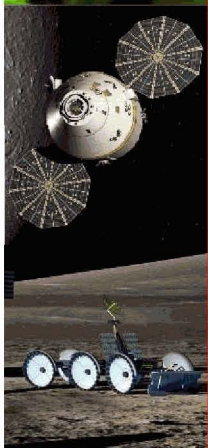
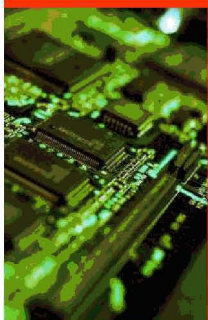
• **Major Project Milestones / Approach:**

- develop mixed-signal electronics with proven wide T + radiation capability
- **deliver** compact modeling tools for circuit design (**design suite**)
- **deliver** SiGe mixed-signal circuit components (**component library**)
- **deliver** robust packaging for ICs (**integrated multi-chip module**)
- **deliver** a SiGe Remote Electronics Unit (REU) sensor interface prototype
- demonstrate device + circuit + package reliability per NASA specs
- develop a robust infusion path for NASA mission insertion (**TRL-6**)

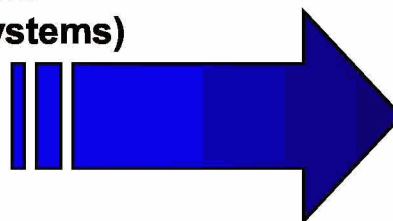
- Goals:**
- 1) **Establish Requisite Infrastructure for NASA Use of SiGe**
 - 2) **Build an Interesting Electronic Prototype for NASA Use**



SiGe Remote Electronics Unit (REU)

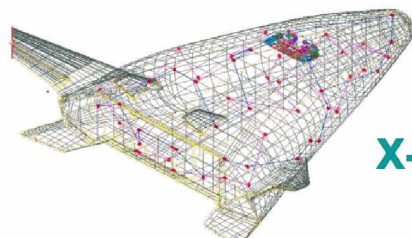


The X-33 Remote Health Monitoring Node,
circa 1998
(BAE Systems)



Original Specifications

- 5" x 3" x 6.75" = 101 in³ size
- 2.3 kg weight
- 17 W power dissipation
- -55°C to +125°C



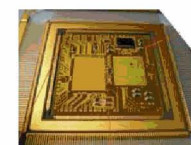
X-33

Supports MANY Different Sensor Types:

Temperature, Strain, Pressure, Acceleration, Vibration, Heat Flux, Position, etc.

Can Use This REU as a Remote Vehicle Health Monitoring Node

Project Demo: SiGe Remote Electronics Unit

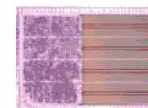


REU in
multichip
package

Analog front
end die



Digital
control die



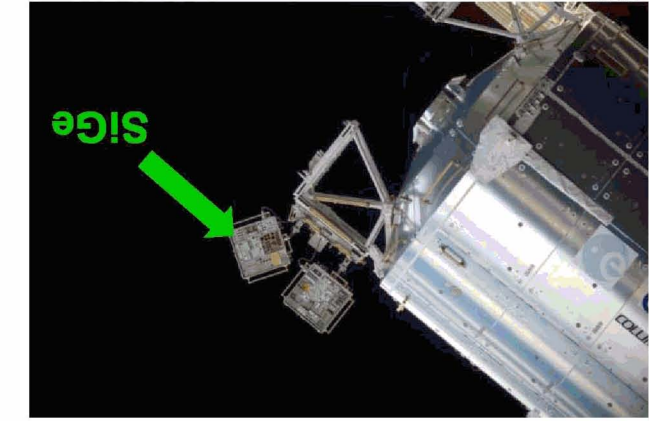
Conceptual integrated REU
system-on-chip SiGe BiCMOS die

Our SWAP Goals

- < 1.5" x 1.5" x 0.5" = 1.1 in³ (100x)
- < 0.2 kg (10x)
- < 1-2 W (10x)
- -180°C to +125°C and rad tolerant!

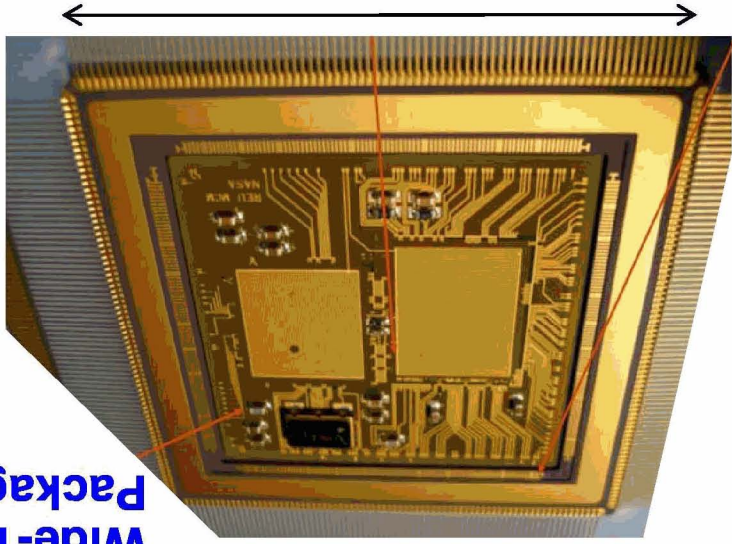


SIGe FY09 Accomplishments

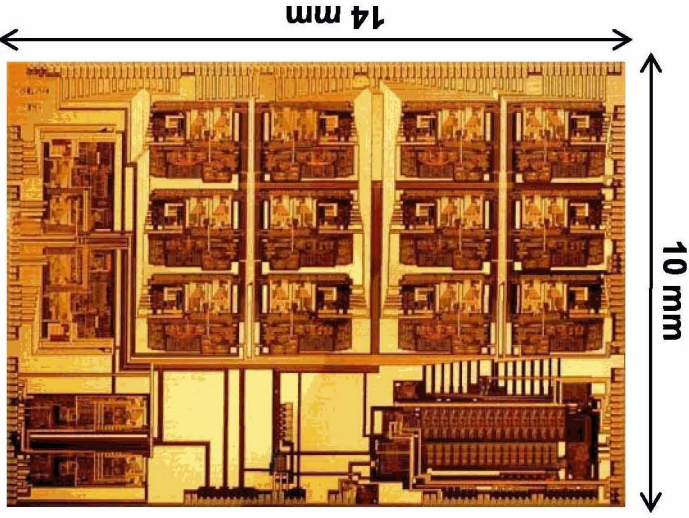


ISS Experiments (MISSE-6,7)

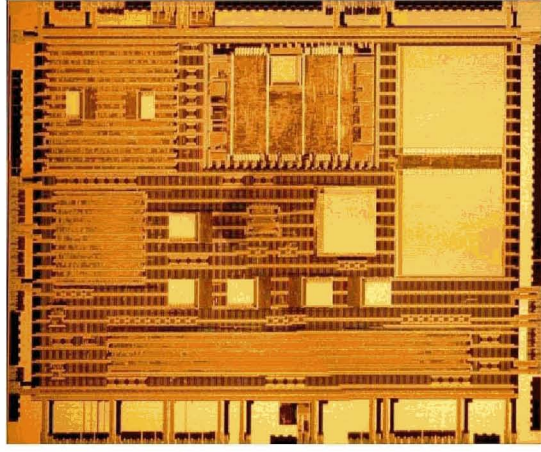
Wide-T
Packaging



2 inches



CRYO-5 SIGe Analog ASIC

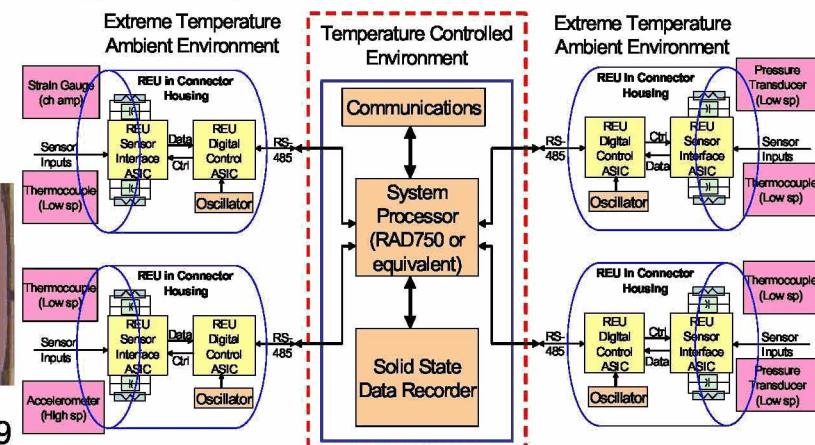
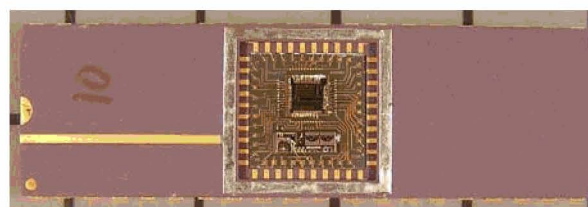
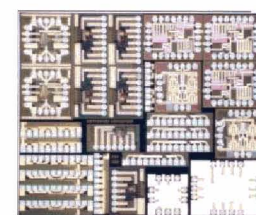
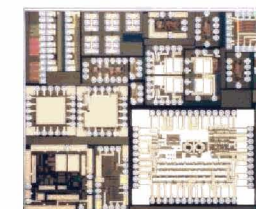
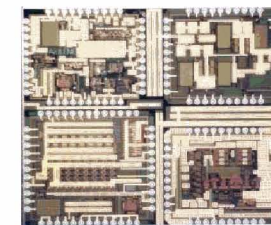
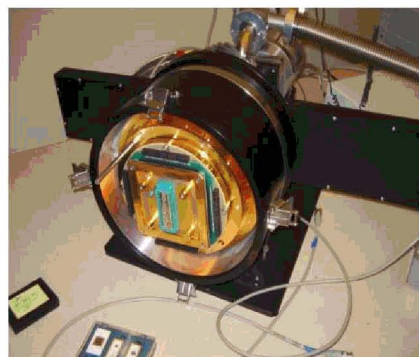
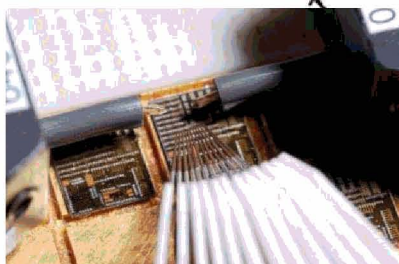
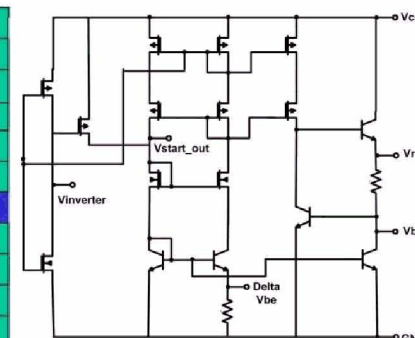
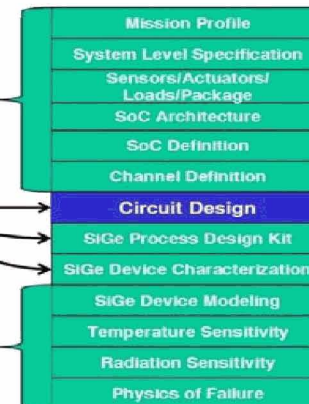
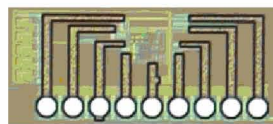
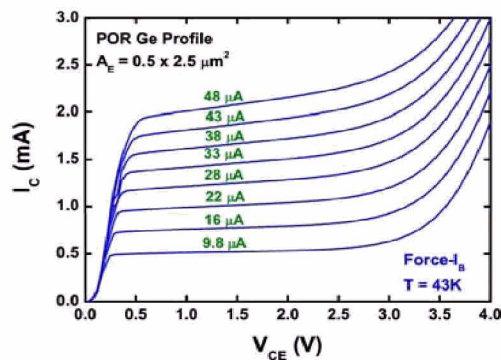
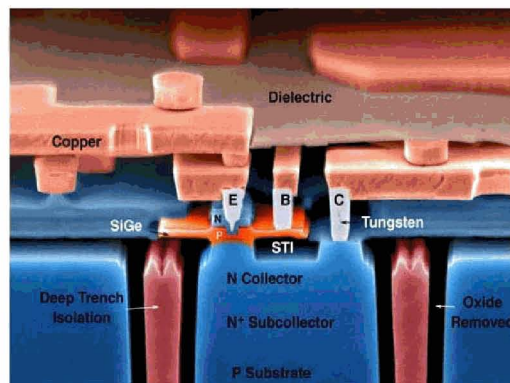


CRYO-5 SIGe Digital ASIC

ETDP AAPs to Lunar Surface Systems TCR, 05 Aug. 2009



SiGe Infrastructure Development



Summary



In response to the Constellation Program's need for environmentally hardened electronics and avionics, the AAPS technology development project is actively working to provide:

- High Performance Processors that will provide high efficiency, radiation hardened performance,
- FPGAs designed such that they are hardened against the radiation environment,
- Volatile and nonvolatile memories using new technologies that can withstand the radiation environment,
- Reconfigurable Computing capabilities that allow a single processor board to fulfill multiple functions,
- SiGe-based electronics that allow operation in the low-temperature and radiation environments of the lunar surface, and
- The capability to accurately model the response of an electronic design to the radiation environment.

