



Balloon for Long-Duration, High-Altitude Flight at Venus

A document describes a 5.5-m-diameter, helium-filled balloon designed for carrying a scientific payload having a mass of 44 kg for at least six days at an altitude of about 55 km in the atmosphere of Venus. The requirement for floating at nearly constant altitude dictates the choice of a mass-efficient spherical super-pressure balloon that tracks a constant atmospheric density. Therefore, the balloon is of a conventional spherical super-pressure type, except that it is made of materials chosen to minimize solar radiant heating and withstand the corrosive sulfuric acid aerosol of the Venusian atmosphere.

The shell consists of 16 gores of a multilayer composite material. The outer layer, made of polytetrafluoroethylene, protects against sulfuric acid aerosol. Next is an aluminum layer that reflects sunlight to minimize heating, followed by an aluminized polyethylene terephthalate layer that resists permeation by helium, followed by an aromatic polyester fabric that imparts strength to withstand deployment forces and steady super-pressure. A polyurethane coat on the inner surface of the fabric facilitates sealing at gore-to-gore seams. End fittings and seals, and a tether connecting the end fittings to a gondola, are all made of sulfuric-acid-resistant materials.

*This work was done by Jeffrey Hall, Viktor Kerzhanovich, and Andre Yavrouian of Caltech; Debra Fairbrother and Magdi Said of NASA-Wallops Flight Facility; and Chuck Sandy and Thad Fredrickson of ILC Dover, Inc. for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
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Wide-Temperature-Range Integrated Operational Amplifier

A document discusses a silicon-on-insulator (SOI) complementary metal oxide/semiconductor (CMOS) integrated-circuit operational amplifier to be replicated and incorporated into sensor and actuator systems of Mars-explorer robots. This amplifier is designed to function at a supply potential ≤ 5.5 V, at any temperature from -180 to $+120$ °C. The design is implemented on a commercial radiation-hard SOI CMOS process rated for a supply potential of ≤ 3.6 V and temperatures from -55 to $+110$ °C. The design incorporates several innovations to achieve this, the main ones being the following:

- NMOS transistor channel lengths below 1 μm are generally not used because research showed that this change could reduce the adverse effect of hot-carrier injection on the lifetimes of transistors at low temperatures.

- To enable the amplifier to withstand the 5.5-V supply potential, a circuit topology including cascade devices, clamping devices, and dynamic voltage biasing was adopted so that no individual transistor would be exposed to more than 3.6 V.
- To minimize undesired variations in performance over the temperature range, the transistors in the amplifier are biased by circuitry that maintains a constant inversion coefficient over the temperature range.

This work was done by Mohammad Mojaradi, Greg Levanas, Yuan Chen, Elizabeth Kolawa, and Raymond Cozy of Caltech, and Benjamin Blalock, Robert Greenwell, and Stephen Terry of the University of Tennessee for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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