cost, largely by utilizing digital processing in advanced field-programmable gate arrays (FPGAs) to perform all of the many functions (for example, color-balance and contrast adjustments) of a professional color video camera. The processing is programmed in VHDL so that application-specific integrated circuits (ASICs) can be fabricated directly from the program. ["VHDL" signifies VHSIC Hardware Description Language C, a computing language used by the United States Department of Defense for describing, designing, and simulating very-high-speed integrated circuits (VHSICs).]

The image-sensor and FPGA clock frequencies in these cameras have generally been much higher than those used in video cameras designed and manufactured elsewhere. Frequently, the outputs of these cameras are converted to other video-camera formats by use of pre- and post-filters.

This work was done by William Glenn of Florida Atlantic University for Marshall Space Flight Center. For further information, contact Jerry Engelbrecht at 561-297-2335. MFS-32091-1

Circuit for Full Charging of Series Lithium-Ion Cells

Differences among cells would no longer prevent full charging.

Lyndon B. Johnson Space Center, Houston, Texas

An advanced charger has been proposed for a battery that comprises several lithium-ion cells in series. The proposal is directed toward charging the cells in as nearly an optimum manner as possible despite unit-to-unit differences among the nominally identical cells.

The particular aspect of the charging problem that motivated the proposal can be summarized as follows: During bulk charging (charging all the cells in series at the same current), the voltages of individual cells increase at different rates. Once one of the cells reaches full charge, bulk charging must be stopped, leaving other cells less than fully charged.

To make it possible to bring all cells up to full charge once bulk charging has been completed, the proposed charger would include a number of "top-off" chargers — one for each cell. The top-off chargers would all be powered from the same DC source, but their outputs would be DC-isolated from each other and AC-coupled to their respective cells by means of transformers, as described below.

Each top-off charger would include a flyback transformer, an electronic switch, and an output diode. For suppression of undesired electromagnetic emissions, each top-off charger would also include (1) a resistor and capacitor configured to act as a snubber and (2) an inductor and capacitor configured as a filter. The magnetic characteristics of the flyback transformer and the duration of its output pulses determine the energy delivered to the lithium-ion cell.

It would be necessary to equip the cell with a precise voltage monitor to determine when the cell reaches full charge. In response to a full-charge reading by this voltage monitor, the electronic switch would be held in the "off" state. Other cells would continue to be charged similarly by their top-off chargers until their voltage monitors read full charge.

This work was done by William E. Ott and David L. Saunders of Honeywell, Inc. for Johnson Space Center.

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457(f)}, to Honeywell, Inc. Inquiries concerning licenses for its commercial development should be addressed to:

Honeywell, Inc.
P.O. Box 52199
Phoenix, AZ 85072-2199

Refer to MSC-23503, volume and number of this NASA Tech Briefs *issue, and the page number.*

Analog Nonvolatile Computer Memory Circuits

Digital data would be stored in analog form in FFETs.

Marshall Space Flight Center, Alabama

In nonvolatile random-access memory (RAM) circuits of a proposed type, digital data would be stored in analog form in ferroelectric field-effect transistors (FFETs). This type of memory circuit would offer advantages over prior volatile and nonvolatile types:

- In a conventional complementary metal oxide/semiconductor static RAM, six transistors must be used to store one bit, and storage is volatile in that data are lost when power is turned off. In a conventional dynamic RAM, three transistors must be used to store one bit, and the stored bit must be refreshed every few milliseconds. In contrast, in a RAM according to the proposal, data would be retained when power was turned off, each memory cell would contain only two FFETs, and the cell could store multiple bits (the exact number of bits depending on the specific design).
- Conventional flash memory circuits afford nonvolatile storage, but they operate at reading and writing times of the order of thousands of conventional computer memory reading and writing times and, hence, are suitable for use only as off-line storage devices. In addition, flash memories cease to function after limited numbers of writing cycles. The proposed memory circuits would not be subject to either of these limitations.
- Prior developmental nonvolatile ferroelectric memories are limited to one bit per cell, whereas, as stated above, the proposed memories would not be so limited.

The design of a memory circuit according to the proposal must reflect the fact that FFET storage is only partly nonvolatile, in that the signal stored in an FFET decays gradually over time. (Retention times of some advanced FFETs exceed