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## Maintaining Stability During a Conducted-Ripple EMC Test

**Ripple is now injected via amplifier-controlled FETs instead of a transformer.**

*NASA's Jet Propulsion Laboratory, Pasadena, California*

An improved technique, and electronic circuitry to implement the technique, have been developed for a military-standard electromagnetic-compatibility (EMC) test in which one analyzes susceptibility to low-frequency ripple conducted into the equipment under test via a DC power line. In the traditional technique for performing the particular test, the ripple is coupled onto the DC power line via a transformer. Depending upon some design details of the equipment under test, the inductance of the transformer can contribute a degree of instability that results in an oscillation of amplitude large enough to destroy the equipment.

It is usually possible to suppress the oscillation by connecting a damping resistor to the primary terminals of the

ripple-injection transformer. However, it is important to emphasize the “usually” in the preceding sentence: sometimes, the resistive damping becomes insufficient to suppress destructive oscillation. In addition, undesirably, the resistor contributes to power dissipation and power demand, and thereby also necessitates the use of a larger ripple-voltage amplifier. Yet another disadvantage of the transformer-coupling technique is that the transformer introduces low-frequency distortion of the injected ripple voltage.

The improved technique makes it possible to inject ripple with very low distortion at low frequency, without inducing oscillation. In this technique, a transformer is not used: Instead, power

is fed to the equipment under test via series power field-effect transistors (FETs) controlled by a summing operational amplifier. One of the inputs to the amplifier controls the DC component of the power-line voltage; the other input, generated by an external oscillator, controls the ripple component. The circuitry for implementing this technique includes panel displays, an internal power supply for the operational amplifier and panel displays, and amplitude controls for the DC and ripple power-line voltage components.

*This work was done by Vatche Vorperian of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-30652*

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## Photodiode Preamplifier for Laser Ranging With Weak Signals

**This circuit suppresses noise without sacrificing timing accuracy.**

*NASA's Jet Propulsion Laboratory, Pasadena, California*

An improved preamplifier circuit has been designed for processing the output of an avalanche photodiode (APD) that is used in a high-resolution laser ranging system to detect laser pulses returning from a target. The improved circuit stands in contrast to prior such circuits in which the APD output current pulses are made to pass, variously, through wide-band or narrow-band load networks before preamplification. A major disadvantage of the prior wide-band load networks is that they are highly susceptible to noise, which degrades timing resolution. A major disadvantage of the prior narrow-band load networks is that they make it difficult to sample the amplitudes of the narrow laser pulses ordi-

narily used in ranging.

In the improved circuit, a load resistor is connected to the APD output and its value is chosen so that the time constant defined by this resistance and the APD capacitance is large, relative to the duration of a laser pulse. The APD capacitance becomes initially charged by the pulse of current generated by a return laser pulse, so that the rise time of the load-network output is comparable to the duration of the return pulse. Thus, the load-network output is characterized by a fast-rising leading edge, which is necessary for accurate pulse timing.

On the other hand, the resistance-capacitance combination constitutes a low-pass filter, which helps to suppress noise. The long time constant causes the load-

network output pulse to have a long shallow-sloping trailing edge, which makes it easy to sample the amplitude of the return pulse. The output of the load network is fed to a low-noise, wide-band amplifier. The amplifier must be a wide-band one in order to preserve the sharp pulse rise for timing. The suppression of noise and the use of a low-noise amplifier enable the ranging system to detect relatively weak return pulses.

*This work was done by Alexander Abramovici and Jacob Chapsky of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-30598*

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## Advanced High-Definition Video Cameras

*Marshall Space Flight Center, Alabama*

A product line of high-definition color video cameras, now under development, offers a superior combination of desirable characteristics, including high frame rates, high resolutions, low power con-

sumption, and compactness. Several of the cameras feature a 3,840 × 2,160-pixel format with progressive scanning at 30 frames per second. The power consumption of one of these cameras is about 25

W. The size of the camera, excluding the lens assembly, is 2 by 5 by 7 in. (about 5.1 by 12.7 by 17.8 cm).

The aforementioned desirable characteristics are attained at relatively low

cost, largely by utilizing digital processing in advanced field-programmable gate arrays (FPGAs) to perform all of the many functions (for example, color-balance and contrast adjustments) of a professional color video camera. The processing is programmed in VHDL so that application-specific integrated circuits (ASICs) can be fabricated directly from the program. ["VHDL" signifies

VHSIC Hardware Description Language C, a computing language used by the United States Department of Defense for describing, designing, and simulating very-high-speed integrated circuits (VHSICs).]

The image-sensor and FPGA clock frequencies in these cameras have generally been much higher than those used in video cameras designed and manufac-

ured elsewhere. Frequently, the outputs of these cameras are converted to other video-camera formats by use of pre- and post-filters.

*This work was done by William Glenn of Florida Atlantic University for Marshall Space Flight Center. For further information, contact Jerry Engelbrecht at 561-297-2335. MFS-32091-1*

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## Circuit for Full Charging of Series Lithium-Ion Cells

**Differences among cells would no longer prevent full charging.**

*Lyndon B. Johnson Space Center, Houston, Texas*

An advanced charger has been proposed for a battery that comprises several lithium-ion cells in series. The proposal is directed toward charging the cells in as nearly an optimum manner as possible despite unit-to-unit differences among the nominally identical cells.

The particular aspect of the charging problem that motivated the proposal can be summarized as follows: During bulk charging (charging all the cells in series at the same current), the voltages of individual cells increase at different rates. Once one of the cells reaches full charge, bulk charging must be stopped, leaving other cells less than fully charged.

To make it possible to bring all cells up to full charge once bulk charging has been completed, the proposed charger would include a number of "top-off" chargers — one for each cell. The top-off

chargers would all be powered from the same DC source, but their outputs would be DC-isolated from each other and AC-coupled to their respective cells by means of transformers, as described below.

Each top-off charger would include a flyback transformer, an electronic switch, and an output diode. For suppression of undesired electromagnetic emissions, each top-off charger would also include (1) a resistor and capacitor configured to act as a snubber and (2) an inductor and capacitor configured as a filter. The magnetic characteristics of the flyback transformer and the duration of its output pulses determine the energy delivered to the lithium-ion cell.

It would be necessary to equip the cell with a precise voltage monitor to determine when the cell reaches full charge. In response to a full-charge reading by

this voltage monitor, the electronic switch would be held in the "off" state. Other cells would continue to be charged similarly by their top-off chargers until their voltage monitors read full charge.

*This work was done by William E. Ott and David L. Saunders of Honeywell, Inc. for Johnson Space Center.*

*Title to this invention has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457(f)}, to Honeywell, Inc. Inquiries concerning licenses for its commercial development should be addressed to:*

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*Refer to MSC-23503, volume and number of this NASA Tech Briefs issue, and the page number.*

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## Analog Nonvolatile Computer Memory Circuits

**Digital data would be stored in analog form in FFETs.**

*Marshall Space Flight Center, Alabama*

In nonvolatile random-access memory (RAM) circuits of a proposed type, digital data would be stored in analog form in ferroelectric field-effect transistors (FFETs). This type of memory circuit would offer advantages over prior volatile and nonvolatile types:

- In a conventional complementary metal oxide/semiconductor static RAM, six transistors must be used to store one bit, and storage is volatile in that data are lost when power is turned off. In a conventional dynamic RAM, three transistors must be used to store one bit, and the stored bit must be re-

freshed every few milliseconds. In contrast, in a RAM according to the proposal, data would be retained when power was turned off, each memory cell would contain only two FFETs, and the cell could store multiple bits (the exact number of bits depending on the specific design).

- Conventional flash memory circuits afford nonvolatile storage, but they operate at reading and writing times of the order of thousands of conventional computer memory reading and writing times and, hence, are suitable for use only as off-line storage devices. In addition, flash

memories cease to function after limited numbers of writing cycles. The proposed memory circuits would not be subject to either of these limitations.

- Prior developmental nonvolatile ferroelectric memories are limited to one bit per cell, whereas, as stated above, the proposed memories would not be so limited.

The design of a memory circuit according to the proposal must reflect the fact that FFET storage is only partly nonvolatile, in that the signal stored in an FFET decays gradually over time. (Retention times of some advanced FFETs exceed