# Reconfigurable, Bi-Directional Flexfet Level Shifter for Low-Power, Rad-Hard Integration

**These level shifters enable the development of multi-level voltage systems.**

*Goddard Space Flight Center, Greenbelt, Maryland*

Two prototype Reconfigurable, Bi-directional Flexfet Level Shifters (ReBiLS) have been developed, where one version is a stand-alone component designed to interface between external low voltage and high voltage, and the other version is an embedded integrated circuit (IC) for interface between internal low-voltage logic and external high-voltage components. Targeting stand-alone and embedded circuits separately allows optimization for these distinct applications. Both ReBiLS designs use the commercially available 180-nm Flexfet Independently Double-Gated (IDG) SOI CMOS (silicon on insulator, complementary metal oxide semiconductor) technology.

Embedded ReBiLS circuits were integrated with a Reed-Solomon (RS) encoder using CMOS Ultra-Low-Power Radiation Tolerant (CULPRiT) double-gated digital logic circuits. The scope of the project includes: creation of a new high-voltage process, development of ReBiLS circuit designs, and adjustment of the designs to maximize performance through simulation, layout, and manufacture of prototypes.

The primary technical objectives were to develop a high-voltage, thick oxide option for the 180-nm Flexfet process, and to develop a stand-alone ReBiLS IC with two 8-channel I/O busses, 1.8–2.5 I/O on the low-voltage pins, 5.0-V-tolerant input and 3.3-V output I/O on the high-voltage pins, and 100-MHz minimum operation with 10-pF external loads.

Another objective was to develop an embedded, rad-hard ReBiLS I/O cell with 0.5-V low-voltage operation for interface with core logic, 5.0-V-tolerant input and 3.3-V output I/O pins, and 100-MHz minimum operation with 10-pF external loads.

A third objective was to develop a 0.5-V Reed-Solomon Encoder with embedded ReBilS I/O:

- Transfer the existing CULPRiT RS encoder from a 0.35-μm bulk-CMOS process to the ASI 180-nm Flexfet, rad-hard SOI Process.
- 0.5-V low-voltage core logic.
- 5.0-V-tolerant input and 3.3-V output I/O pins.
- 100-MHz minimum operation with 10-pF external loads.

The stand-alone ReBiLS chip will allow system designers to provide efficient bi-directional communication between components operating at different voltages. Embedding the ReBiLS cells into the proven Reed-Solomon encoder will demonstrate the ability to support new product development in a commercially viable, rad-hard, scalable 180-nm SOI CMOS process.

*This work was done by Kelly DeGregorio and Dale G. Wilson of American Semiconductor, Inc. for Goddard Space Flight Center. Further information is contained in a TSP* *(see page 1).* *GSC-15565-1*

# Hardware-Efficient Monitoring of I/O Signals

*Lyndon B. Johnson Space Center, Houston, Texas*

In this invention, command and monitor functionality is moved between the two independent pieces of hardware, in which one had been dedicated to command and the other had been dedicated to monitor, such that some command and some monitor functionality appears in each. The only constraint is that the monitor for signal cannot be in the same hardware as the command I/O it is monitoring. The splitting of the command outputs between independent pieces of hardware may require some communication between them, i.e. an intra-switch trunk line. This innovation reduces the amount of wasted hardware and allows the two independent pieces of hardware to be designed identically in order to save development costs.

*This work was done by Kevin R. Driscoll, Brendan Hall, and Michael Paulitsch of Honeywell, Inc. for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809.*

*Title to this invention has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457(f)} to Honeywell, Inc. Inquiries concerning licenses for its commercial development should be addressed to:*

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*Refer to MSC-24458-1, volume and number of this* NASA Tech Briefs *issue, and the page number.*

# Video System for Viewing From a Remote or Windowless Cockpit

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A system of electronic hardware and software synthesizes, in nearly real time, an image of a portion of a scene surveyed by as many as eight video cameras aimed, in different directions, at portions of the scene. This is a prototype of systems that would enable a pilot to view the scene outside a remote or windowless cockpit. The outputs of the cameras are digitized.

Direct memory addressing is used to store the data of a few captured images in sequence, and the sequence is repeated in cycles. Cylindrical warping is used in merging adjacent images at their borders to construct a mosaic image of the scene. The mosaic-image data are written to a memory block from which they can be rendered on a head-mounted display (HMD) device. A subsystem in the