Pilotless Frame Synchronization Using LDPC Code Constraints

Performance equals or exceeds that attainable by use of pilot symbols.

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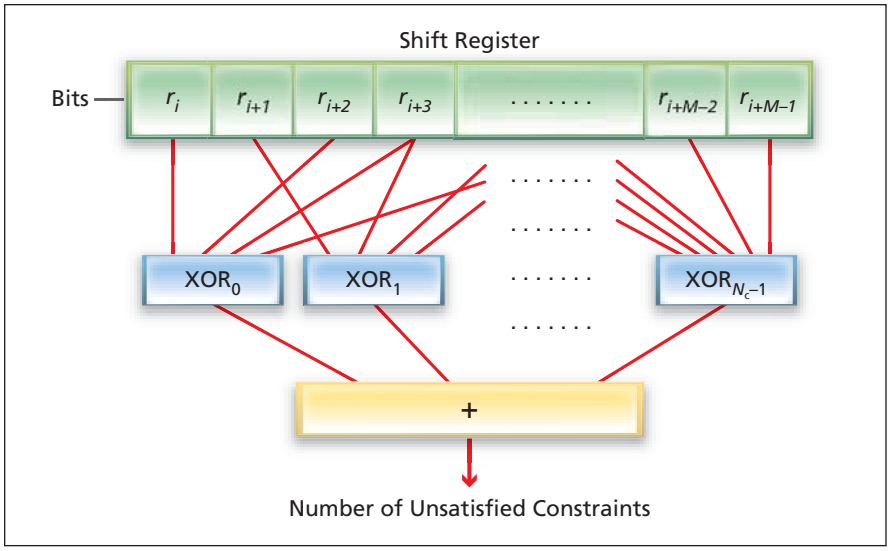
A method of pilotless frame synchronization has been devised for low-density parity-check (LDPC) codes. Heretofore, it has been conventional practice to add pilot symbols, which serve as frame-synchronization markers, to LDPC codes as well as to some other codes. The reception of a signal modulated by a code accompanied by pilot symbols includes a process, separate from the decoding process, in which a correlation rule is used to estimate an offset between (1) the actual received code frame time and (2) a previous estimate of the code frame time. The estimate of the offset then serves as feedback for correcting the previous estimate of the frame time. On the other hand, in pilotless frame synchronization, there are no pilot symbols; instead, the offset is estimated by exploiting selected aspects of the structure of the code. The advantage of pilotless frame synchronization is that the bandwidth of the signal is reduced by an amount associated with elimination of the pilot symbols. The disadvantage is an increase in the amount of receiver data processing needed for frame synchronization.

The present method of pilotless frame synchronization is an instance of code-aided frame synchronization. Most of the prior research on code-aided frame synchronization has focused on Viterbi and turbo codes. One prior method applicable to an LDPC code involves performance of an LDPC iteration and monitoring of the mean of the absolute values of log-likelihood ratios (LLRs) of the variable nodes of the code. The rationale for this method is that the said mean values should be higher for correctly temporally aligned than for incorrectly temporally aligned code words. While this prior method is effective as a means of synchronization, it requires performance of a full LDPC iteration for every possible candidate offset.

The present method of pilotless frame synchronization does not require full LDPC iterations. Instead, it involves exploitation of information available from the constraint nodes of the LDPC code. In an LDPC code, a constraint node represents a parity-check equation in which a set of variable nodes is used as a set of inputs. A valid decoded code word is deemed to be obtained if all parity-check equations are satisfied. Heretofore normally, the information from constraint nodes has been utilized only within the iterative LDPC decoding process to assess the convergence behavior of the process. However, the constraint-node information also has value for frame synchronization in that the number and nature of satisfied constraint-node equations serve as a measure, not only of code convergence, but also of the accuracy of estimates of frame-time offsets.



The **Number of Unsatisfied Constraints** can be computed by using the hardware functional blocks shown here. The labels (r_i,r_{i+1},...) represent bits embodying a decision concerning a decoded symbol. N_c represents the total number of constraints. M represents the number of variable nodes (or block length).

In the present method, hard decisions concerning received symbols are used in the parity-check computations for each constraint node. Because these computations consist mostly of exclusive-OR (XOR) operations, they are considerably less complex than are those of full LDPC iterations. The method could be implemented in hardware that would include a shift register, a multi-operand XOR block for each constraint node, and a multi-operand adder (see figure). The output of the adder — the number of unsatisfied constraints — would be subtracted from the total number of constraints to obtain the number of satisfied constraints.

The present method of pilotless frame synchronization, and alternative methods of synchronization by use of pilot symbols, have been tested by means of computational simulations on a representative LDPC code. Comparative analysis of the results of the simulations has led to the conclusion that the present method of pilotless frame synchronization yields equal or superior performance in the sense that the signal-to-noise ratio needed to keep the bit-error rate from exceeding a given value in this method can be equal to or lower than that needed in any of the alternative methods.

This work was done by Christopher Jones of Caltech and Dong-U Lee, Hyungjin Kim, and John Villasenor of the UCLA Electrical Engineering Department for NASA's Jet Propulsion Laboratory.

The software used in this innovation is available for commercial licensing. Please contact Karina Edmonds of the California Institute of Technology at (626) 395-2322. Refer to NPO-45032.