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Assessment of SOI AND Gate, Type CHT-7408, for Operation in Extreme Temperature Environments

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Background

Electronic parts based on silicon-on-insulator (SOI) technology are finding widespread applications due to their ability to operate in harsh environments and the benefits they offer as compared to their silicon counterparts. Due to their construction, they are tailored for high temperature operation and show good tolerance to radiation events. In addition, their inherent design lessens the formation of parasitic junctions, thereby reducing leakage currents, decreasing power consumption, and enhancing speed. These devices are typically rated in temperature capability from -55°C to about +225°C, and their characteristics over this temperature range are documented in data sheets. Since electronics in some of NASA space exploration missions are required to operate under extreme temperature conditions, both cold and hot, their characteristic behavior within the full temperature spectrum must be determined to establish suitability for use in space applications.

The effects of extreme temperature exposure on the performance of a new commercial-off-the-shelf (COTS) SOI AND gate device were evaluated in this work. The high temperature, quad 2-inputs AND gate device, which was recently introduced by CISSOID, is fabricated using a CMOS SOI process [1]. Some of the specifications of the CHT-7408 chip are listed in Table I. By supplying a constant DC voltage to one gate input and a 10 kHz square wave into the other associated gate input, the chip was evaluated in terms of output response, output rise (t_r) and fall times (t_f), and propagation delays (using a 50% level between input and output during low to high (t_{PLH}) and high to low (t_{PHL}) transitions). The supply current of the gate circuit was also obtained. These parameters were recorded at various test temperatures between -195°C and +250°C using a Sun Systems environmental chamber programmed at a temperature rate of change of 10°C/min. In addition, the effects of thermal cycling on this chip were determined by exposing it to a total of 12 cycles between -195°C and +250°C. Following the cycling activity, measurements were performed again at the test temperatures of -195°C, +21°C, and +250°C.

Table I. Manufacturer specifications of CISSOID CHT-7408 AND gate.

Parameter	Symbol	CHT-7408
Voltage Supply (V)	V_{DD}	3.3 to 5
Quiescent Current (μA)	I_{DD}	10.5
Operating Temperature (°C)	T_{oper}	-55 to +225
Rise Time (ns)	t_r	12.5
Fall Time (ns)	t_f	14.5
Propagation Delay Time (ns)	τ_{PLH}	16.5
Propagation Delay Time (ns)	τ_{PHL}	18.0
Package		DIL-14
Lot Number		2080182.1

Results and Discussion

Temperature Effects

Waveforms of the input and the output signal for the CHT-7408 AND gate at room temperature are shown in Figure 1. These waveforms were also obtained for all other test temperatures in the range from -195°C to +250°C. The gate circuit was found to maintain its logic function throughout the entire test temperature range. Therefore, only those waveforms pertaining to data collected at the extreme temperatures of -195°C and +250°C are presented and shown in Figures 2 and 3, respectively.

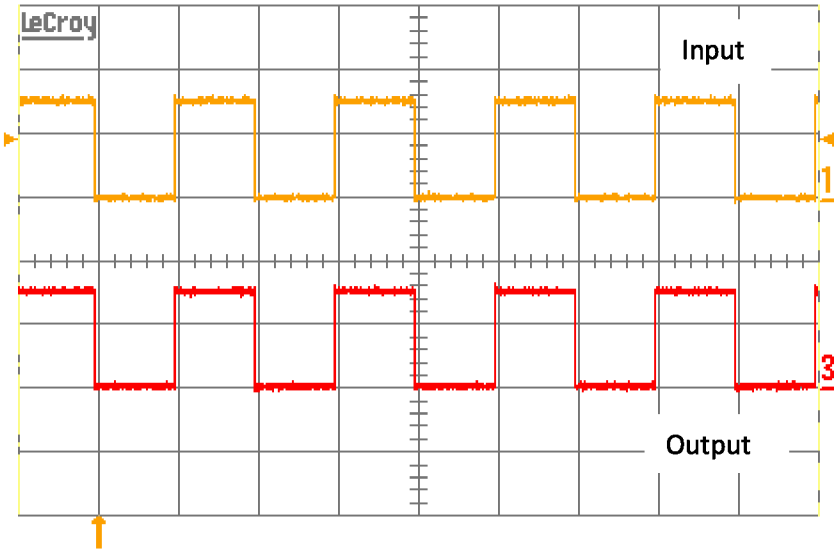

Figure 1. Waveforms of CHT-7408 output signals at +21°C.

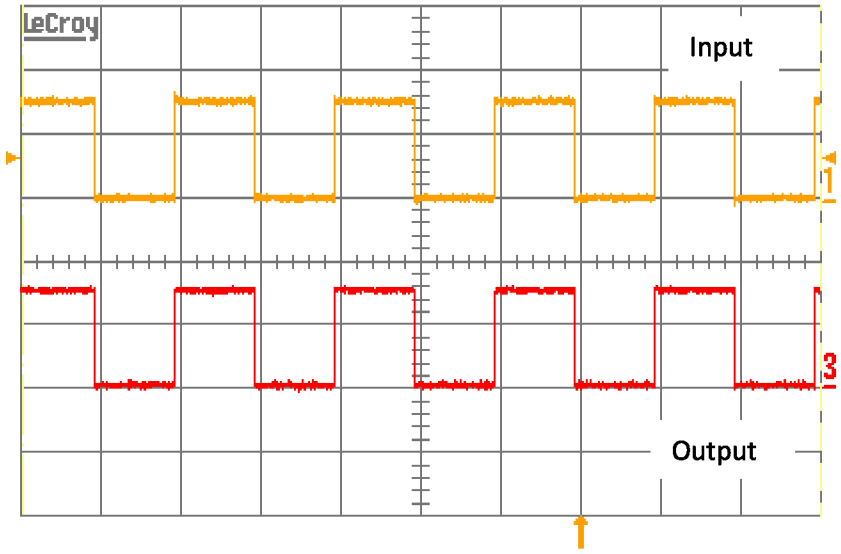

Figure 2. Waveforms of CHT-7408 output signals at -195°C.

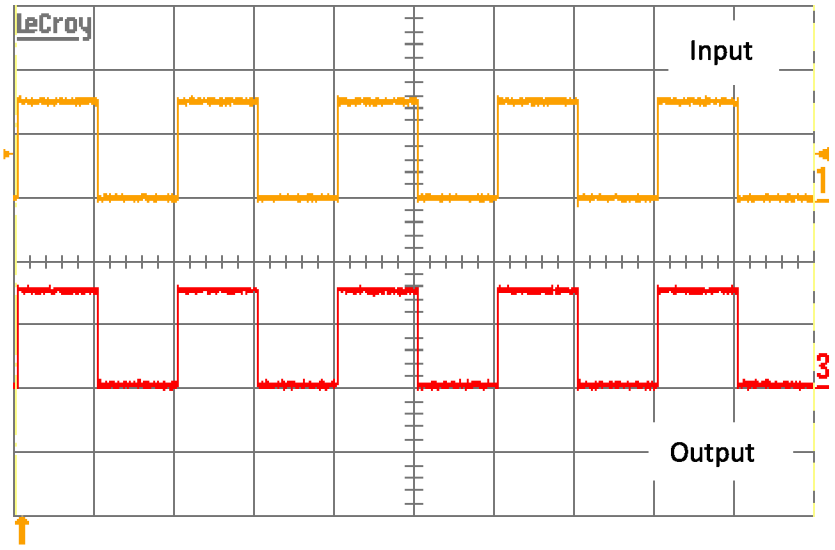

Figure 3. Waveforms of CHT-7408 output signals at +250°C.

Among the parameters that were investigated throughout the chip's evaluation were the rise and fall times of its output signal. Figure 4 shows the variation in these properties as a function of temperature. The rise times obtained throughout the entire test temperature range showed a slight but continuous increase in value as temperature was increased. The trend in fall times was similar to that of the rise times.

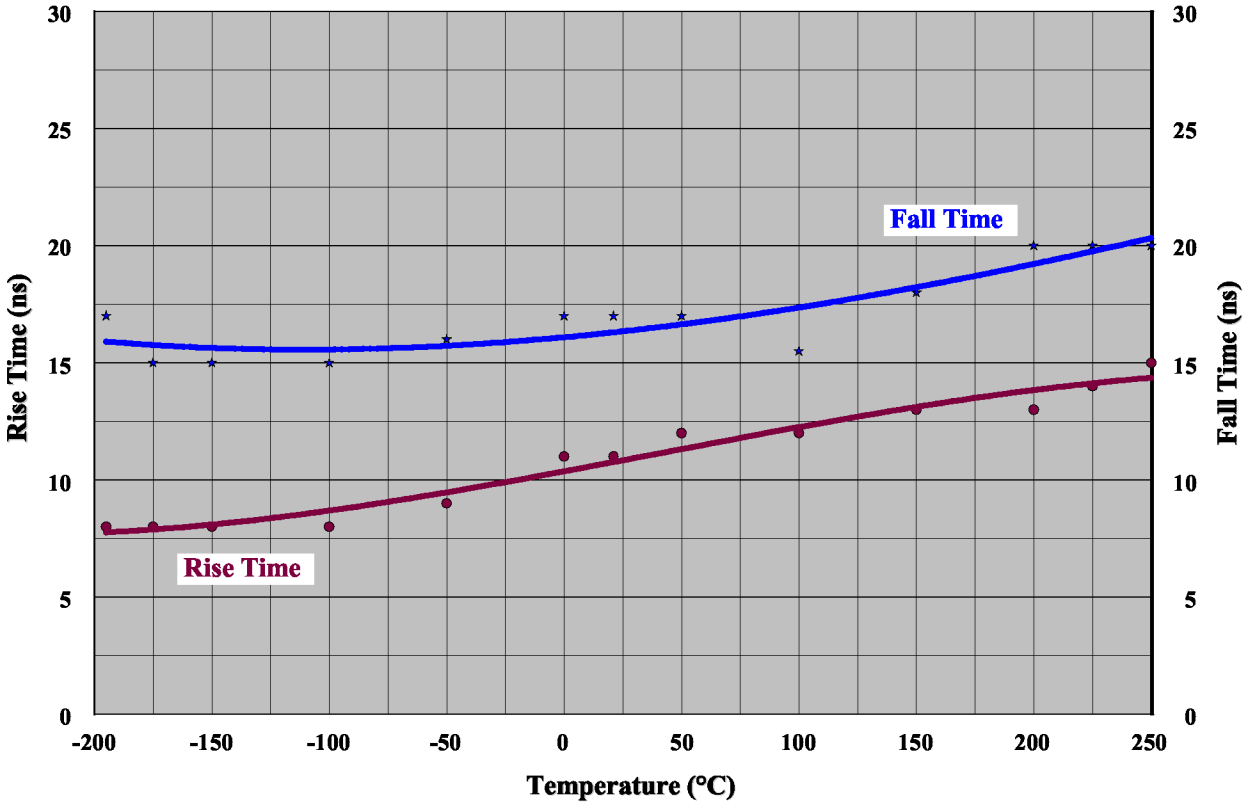

Figure 4. Rise and fall times with respect to temperature for the CHT-7408 AND gate.

The other timing parameters evaluated for the CHT-7408 AND gate were the propagation delay times at 50% level between input and output. These delays were measured for both the low to high (t_{PLH}) and high to low (t_{PHL}) transitions and are depicted in Figure 5. It can be determined from this figure that the delay times from low to high experienced a gradual increase throughout the entire test temperature range of -195°C to +250°C. This increase, however, was more noticeable between the temperatures of -100°C and +150°C. On the other hand, the delay times from high to low experienced a slight decrease in the range from -195°C up to about -100°C. This decrease was then followed by a relatively steep increase in value as the temperature was further increased up to +250°C.

Variation in the supply current of the gate circuit is shown in Figure 6. It can be seen that the supply current maintained a relatively stable value in the temperature range between -200°C and 21°C. Above 21°C, however, the supply current exhibited a sharp increase with increasing temperature. For example, the supply current reached a level of 62 μA at 250°C compared to about 2 μA at room temperature.

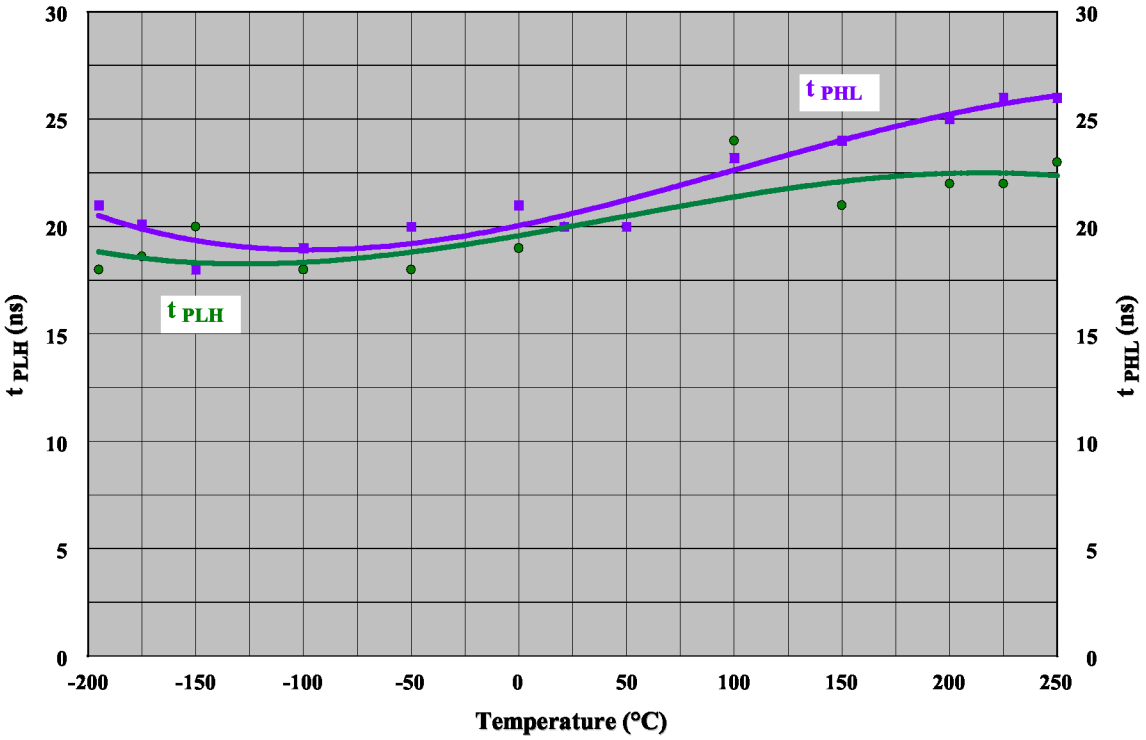

Figure 5. Propagation delay times versus temperature for the CHT-7408 AND gate.

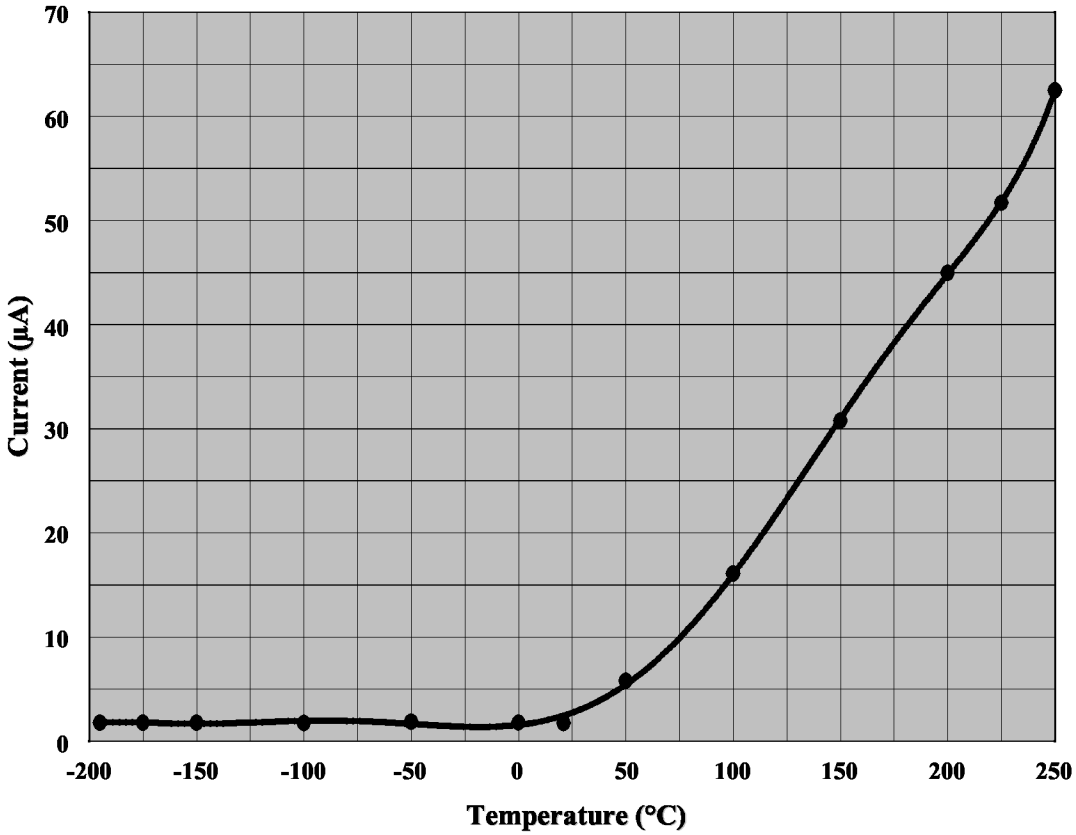

Figure 6. Supply current as a function of temperature for the CHT-7408 AND gate.

Effects of Thermal Cycling

The effects of thermal cycling on the operation of the CISSOID CHT-7408 SOI AND gate were determined by exposing the chip to a total of 12 cycles between -195°C and +250°C at a temperature rate of 10°C/min. The circuit was powered while the cycling activity was taking place. In addition to the pre-cycling data, readings of the investigated properties were taken during as well as after the cycling. No major change was observed in the characteristic behavior of the circuit due to cycling. Table II shows the pre- and post-cycling values of the investigated properties at the selected temperatures of -195°C, 21°C, and 250°C. The limited cycling seemed to also have no effect on the packaging of the chip as no physical damage was observed.

Table II. Post-cycling data for gate properties at extreme temperatures

T (°C)	I_s (µA)		t_r (ns)		t_f (ns)		τ_{PLH} (ns)		τ_{PHL} (ns)	
	Prior	Post	Prior	Post	Prior	Post	Prior	Post	Prior	Post
-195	1.78	1.73	8	9	17	16	18	19	21	21
21	1.74	3.41	11	11	17	16	20	20	20	21
250	62.49	58.90	15	14	20	21	23	23	26	26

Conclusion

A recently introduced commercial-off-the-shelf SOI AND gate chip was characterized under extreme temperature exposure and thermal cycling within the range of -195°C and +250°C. The quad 2-input gate was evaluated in terms of logic response, output rise (t_r) and fall times (t_f), and propagation delays at 50% level between input and output during low to high (t_{PLH}) and high to low (t_{PHL}) transitions. The gate performed very well throughout the entire test temperature range as no significant changes occurred either in its function or in its output signal timing characteristics. The limited cycling, which consisted of 12 cycles between -195°C and +250°C, also had no influence on the gate's performance. In addition, the ceramic packaged part underwent no structural damage due to the extreme temperature exposure. These preliminary results indicate that this device has the potential for use in extreme temperature environments and under wide thermal swings. Additional testing, however, is required to establish its reliability for long-term use in space exploration missions.

References

[1]. CISSOID Corp. "CHT-7408 Quad 2-Inputs AND Gate", Data Sheet, Rev: 01.00, 7/08.

Acknowledgements

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