# NASA Workmanship Hot Topics:

## Water Soluble Flux & ESD Charge Device Model

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http://nepp.nasa.gov/workmanship

http://secureworkgroups.grc.nasa.gov/workmanship

# Overview

- Water Soluble Flux
  - Voiding
  - Cleanliness
- ESD
  - NASA-HDBK-8739.21 for Human Body Model (HBM) and Machine Model (MM) Safety Methods
  - Challenges associated with the Charged Device Model (CDM)

# Water Soluble Flux is not new; just new to NASA (sort of)

Water soluble flux (WSF) has been in commercial use ~20 years. Literature is rich with relevant research.

A NASA spacecraft supplier has used WSF for 10+ years

Assemblies made with (WSF) have entered NASA GSFC systems via:

- Use of a commercial spacecraft bus production line *(several NASA S/C on orbit were built with WSF; one on orbit for 9 years so far)*
- Use of a commercial single board computer
- Difficult-to-solder joints:
  - Custom attach of a connector pigtail/leads to ceramic substrate
  - Device replacement on SMT assembly
- Lead tinning

# NASA Standard Requirement for Non-standard Processes and Materials

4.1.3 Nonstandard Processes, Materials, or Parts. When the supplier intends to use processes, materials, or parts not covered by this publication, the **supplier shall document the details of fabrication and inspection, including acceptance and rejection criteria, and shall provide appropriate test data** (Requirement). Such documentation shall be approved by the procuring NASA Center prior to use (Requirement).

6.13 Flux

6.13.1 Types and Usage . Process documentation shall describe the types of fluxes, where each is used, and the necessary precautions (Requirement).

6.13.2 **Rosin Flux. Rosin flux shall conform to ANSI/J-STD-004, Type L0, L1, or equivalent** (Requirement). Rosin flux types R or RMA in accordance with the requirements of the former military specification, MIL-F-14256 (cancelled June 15, 1995), are considered equivalent to ANSI/J-STD-004, Types L0 or L1, respectively.

6.13.2 continued.

For all fluxing applications **where adequate subsequent cleaning is not practical, only rosin flux Type L0 (Type R of MIL-F-14256) shall be used** (Requirement). Liquid flux used with flux-cored solder shall be chemically compatible with the solder core flux and with the materials with which it will come in contact (Requirement).

6.13.3 Variations. The use of any other flux compositions and forms (other than those listed in paragraph 6.13.2) shall require the approval of the procuring supplier (Requirement). The request for approval shall include the following information as a minimum (Requirement):

a. A complete **chemical characterization** of each flux.

b. A detailed **control system for procurement, receiving inspection, storage, usage**, and application.

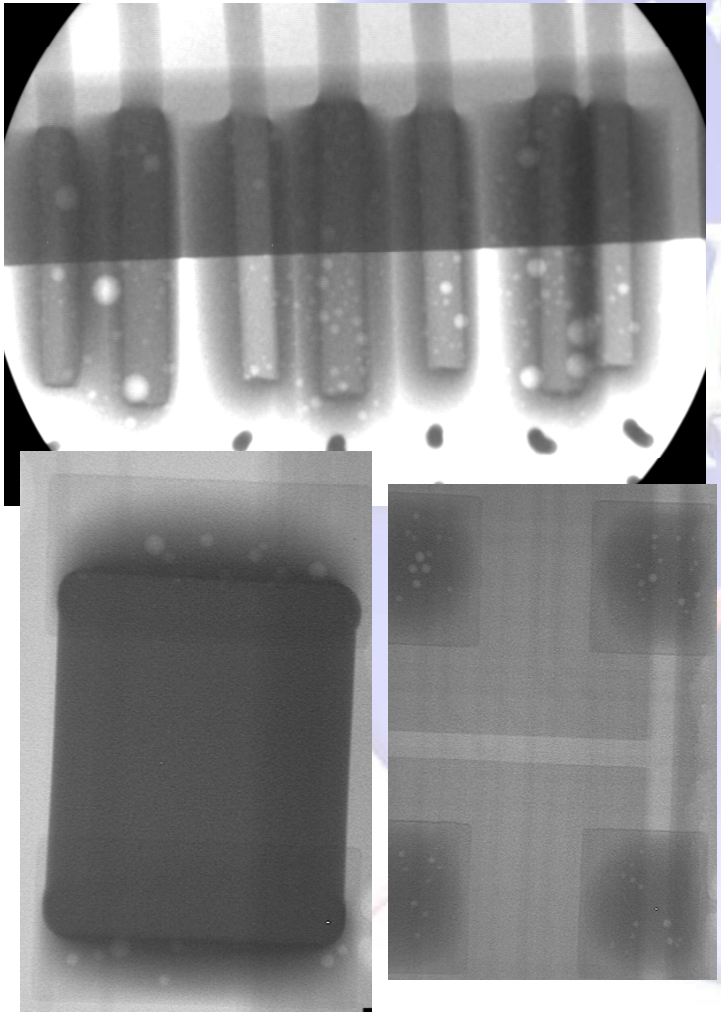
c. Detailed **flux removal cleaning processes, monitoring requirements, cleanliness test methods**, and their results.

***"….is our standard process which has been used on prior flight hardware, for xxx years, with no reliability problems…"***

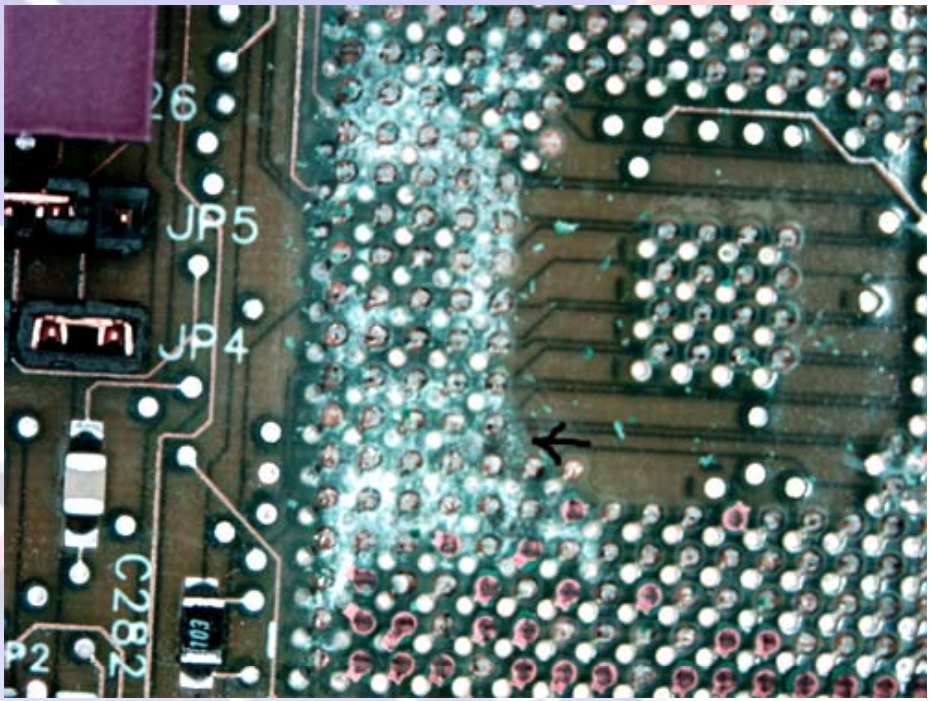
NASA Workmanship cannot use this statement to retire WSF risk.

# Primary Concerns:

## Voiding



## Cleanliness




*Courtesy: Foresite*

*Images and "most" text by courtesy of Intel**

# Voiding – types & causes

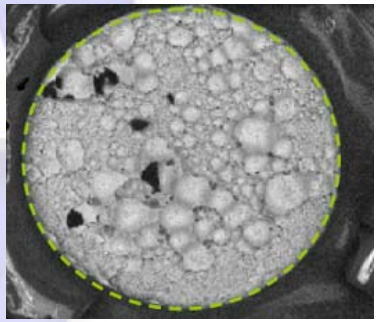
## Macro

**100 to 300 µm** (4 to 12 mils) in diameter [GSFC observed them as small as 10 µm]

**Found anywhere** in the solder joint, not just Land to solder interfaces

Cause: **vaporized ingredients of fluxes** and solder pastes that can't escape molten solder.

IPC Specs 25% max area requirement is targeted toward Macro Voids

## Planar Microvoids – "Champagne Voids"

Smaller than **1-2 mils** in diameter

Located in **one plane** at the Land-to-solder interface **above the IMC**

Yield loss is low, Reliability risk is high

Cause: ??? ENIG voids, excess Phosphorous???

*Larger voids are formed when small voids "bump into" each other.*

*Are planar voids precursors to macro voids?*

*Are they unrelated?*

*Voids in Solder Joints, Raiyo Aspandiar, Senior Materials Scientist, Intel Corporation, Board Technology Segment Integration Group, September 21, 2005, SMTA Northwest Chapter Meeting

# Macro Void Studies

Research focuses on BGAs and Pb-free solder.

Voids noticed during X-ray inspection of hidden solder joints

Concerns are:

- Large voids cause **reductions in effective cross-sectional area** of the soldered joint.
- This results in **higher joint stresses** across that reduced area
- Voiding may also **reduce the distance fatigue cracks have to propagate to cause failure**, although alternatively, voids may act as crack arrestors stopping the propagation of a crack and requiring additional energy to initiate a continuing crack through the remainder of the joint

Published test data don't support established solder fatigue models:

- Many papers how no relationship between voiding and reduced thermal cycle life. Some show the opposite.
- Several researchers reported not being able to simulate greater than 25% voiding (by area in Xray image)

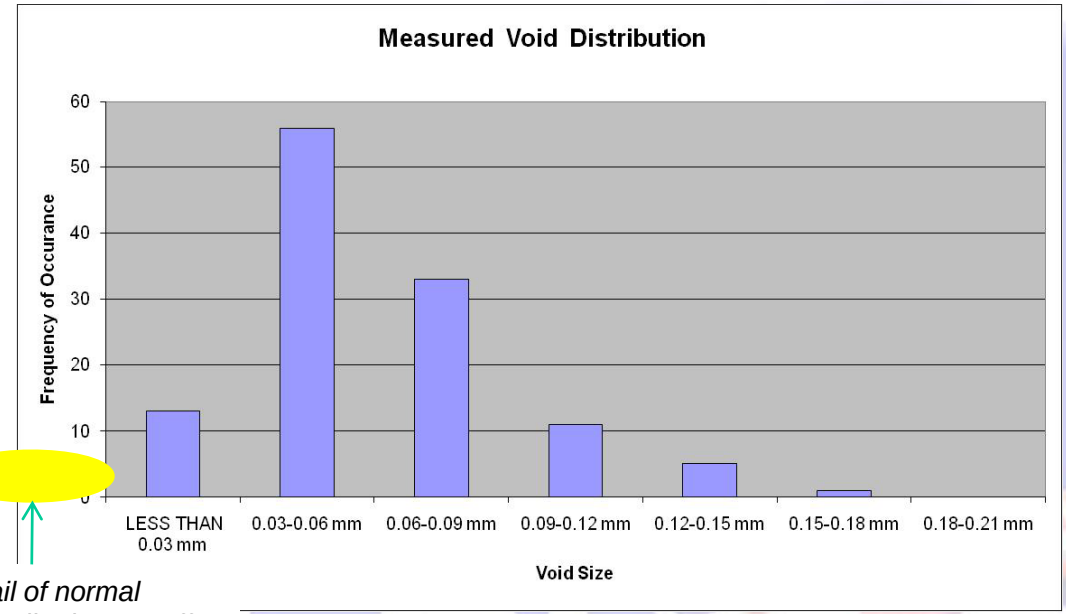
# Lack of Knowledge Drives Need for Project-specific Qualification Data

Step 1: characterize "typical" **void distribution** using Xray

Step 2: use vibration/shock to **establish high cycle/high load life** (pass/fail); also a precondition simulating launch

Step 3: use thermal cycling test, with realistic $\Delta T$ to establish low cycle, **CTE-induced load life**. Test to failure so that Weibull distribution parameters can be determined ($\beta>1$; first failure>life requirement)

Step 4: coordinate with Reliability group to determine acceptability for both **life expectancy** and correlation to **pass/fail criteria for void %**



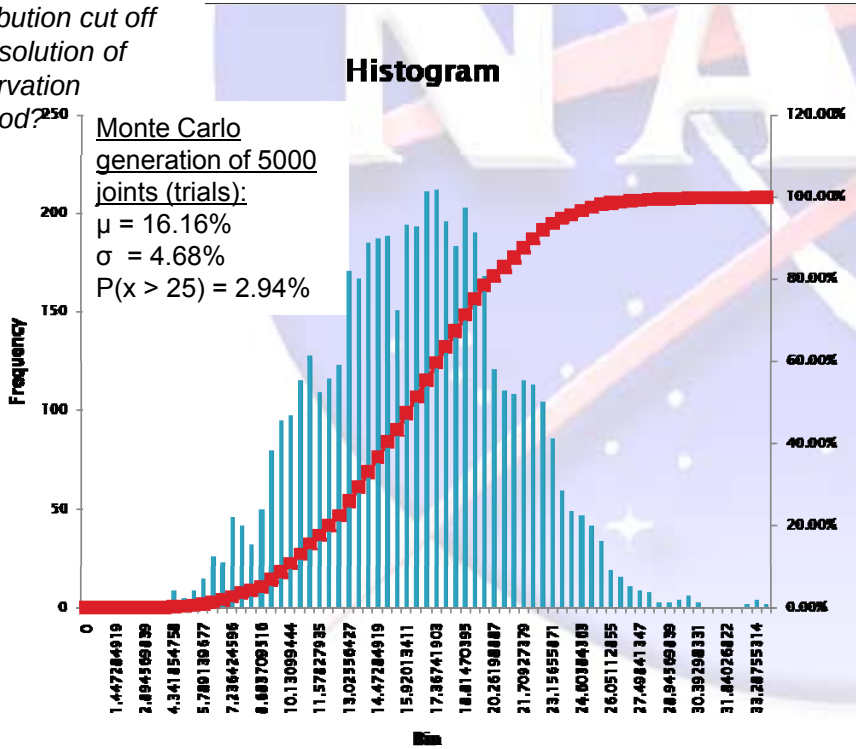

*Tail of normal distribution cut off by resolution of observation method?*

1. Looked at real distribution of voids in a sample board

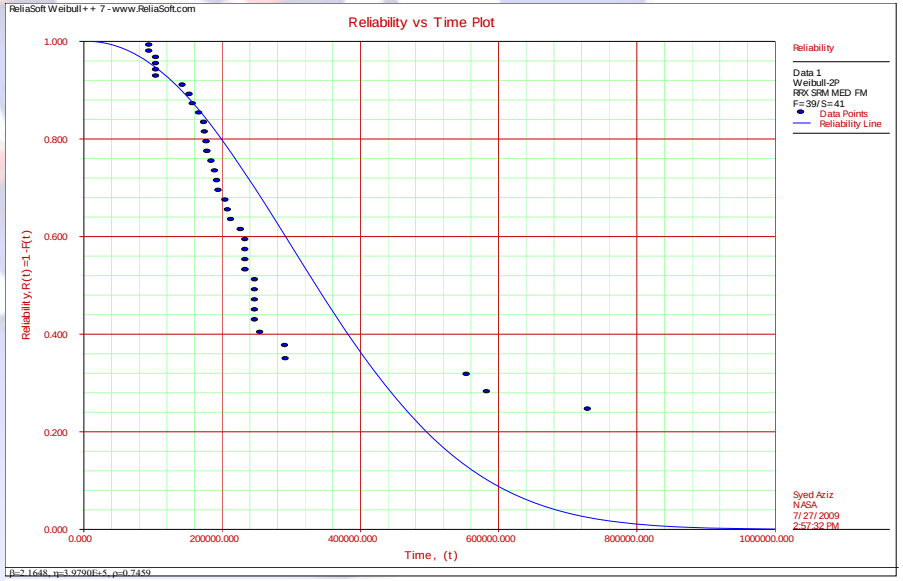
2. Wanted to keep voids under 25% (shear strength reduction starts)

3. Used Monte Carlo simulation on distribution of voids in a sample board to find **screening limit** for void %

4. Used supplier Weibull distribution for Tcycle test data to **establish reliability was acceptable** (supplier's void% was under 5%)




Monte Carlo generation of 5000 joints (trials):
μ = 16.16%
σ = 4.68%
P(x > 25) = 2.94%



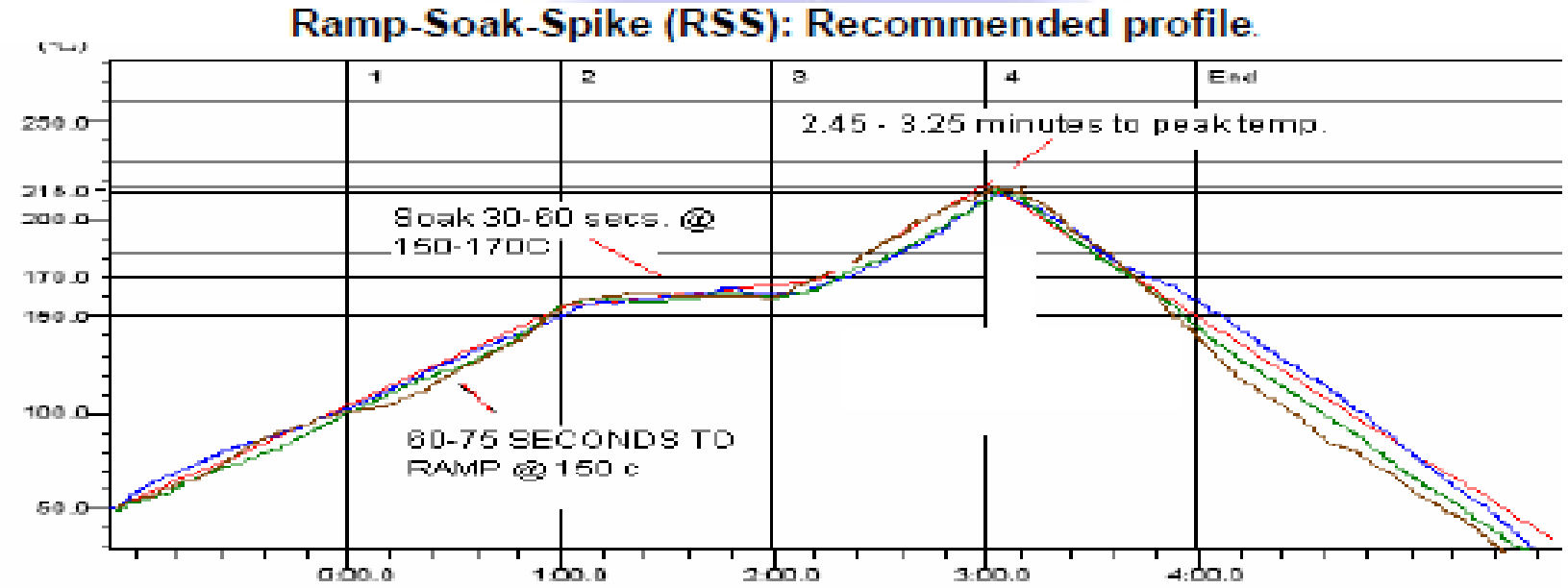

β=2.1648, η=3.979e5, 1st failure at 400,000 cycles

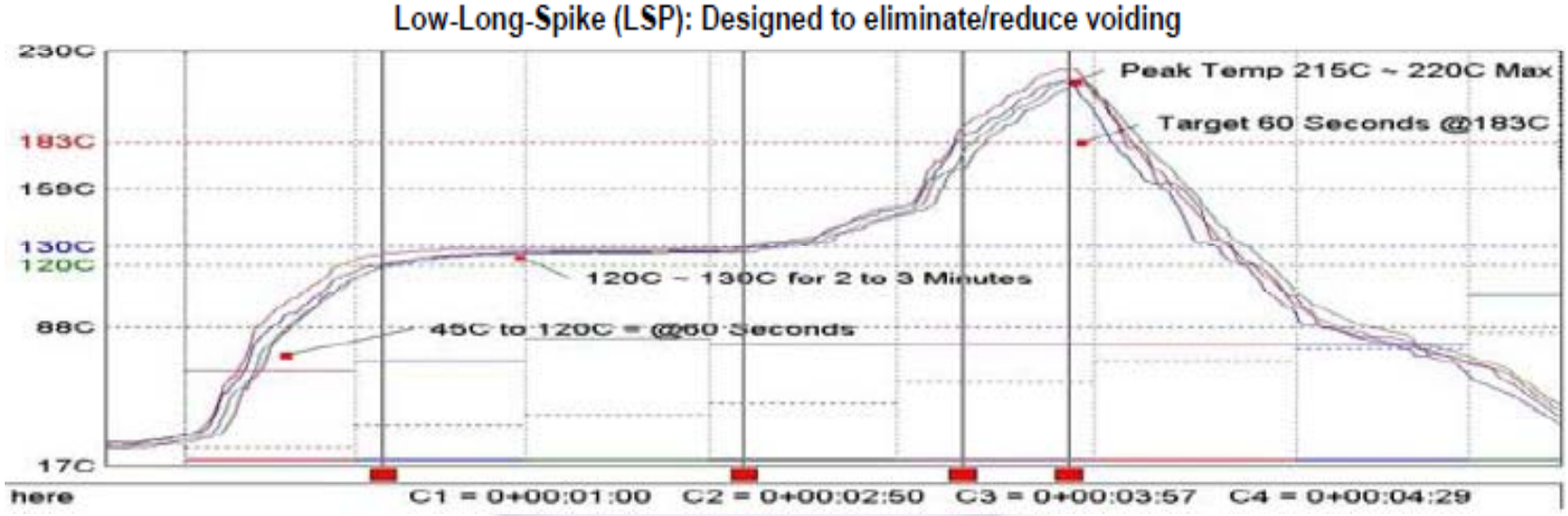
# Not Every Process Creates Voids

- Can't know without looking: most SMT lines do not include Xray unless doing area array attach
  - One supplier (who uses in-line Xray) has no voiding
  - One supplier had problems with a particular part whose solderability was suspect.
- Flux suppliers recommend longer soak time at flux activation temperature for void reduction.
- Relationship of processing parameters to voiding, for all joint types, is not well understood.

Solder Paste Solvent  Solder Powder characteristics  Flux Activity  Flux Amount
Reflow Process Profile  Reflow Atmosphere  PCB and Component Surface
Finish Material and Quality  Land Size and design  Contamination
Ambient temperature and humidity conditions

Ref: datasheet for AIM WS 483



# Will Voids Burst in Vacuum and Release Un-reacted Flux and Solder Shards? Probably Not.

Residues trapped in voids of solder and vias have shown good performance for more than ten years of operating life, even with a voltage differential.[1/]
*(this statement is not referenced to data)*

Risk associated with trapped flux in bubbles? Theoretically

- the amount of flux is insignificant
- the "shell" of solder between the cavity and the outside of the joint must be very thin
- for large bubbles, the thin wall would cave in in room temp/pressure conditions
- for small bubbles, in vacuum there would not be enough pressure to push through the solder.[2/]

1/ Residue Effects of Weak Organic Acid (WOA) Flux Activators, Foresite, August 2005

2/ From: Henning W Leidecker, To: Jeannette F. Plante, Sent: Wednesday, March 04, 2009 9:47 PM, Subject: the reduced atmospheric pressure...

# Research Needed

1. What attributes and boundary conditions differentiate problematic macro voids and planar voids from no-impact macro voids?
   a) Resolve test data with theoretical model
   b) Generate data for standard SMT joints and SnPb solder
2. Assurance through item screening: How can solder joints be screened for macro-voids?
   a) Inspection method including void% determination
   b) Sampling method (unit, lot, line)
3. Assurance through process qualification: What are the process parameters which cause macro-voids and planar voids?
   a) Specific process quality requirements (new area for NASA contracts?)

# Why is Cleanliness Important?

- Un-reacted flux constituents can corrode metals: solder, plating, copper PCB traces

- Ions + Water + Potential difference (V)
  - → Electromigration of metal causing shorts
  - → Conduction through electrolyte
  - → Conduction through formed metallic salts

- Un-reacted WSF is source of Water: Weak Organic Acids (WOA) in WSF readily bind with water.

- Source of ions is: halide additive, "dirty" boards. "dirty" parts, halide built into boards (by design or via poor quality; can be released with heat during reflow or rework).

- Contamination failures will evolve quickly; cost and schedule risk from scrapped boards/parts.

- Metallic salts may be impossible to remove

# How does WSF change our Standard Approach?

Rosin Flux: **Forms protective "shell" over circuitry with high insulation resistance** which stays hard below 65˚C

Water Soluble Flux (WSF):

- Weak Organic Acids are hydrophilic: **collects and retains water.**
- **WOAs are not detected using an ionic measurement of cleaning fluid:** water and alcohol bind to free ion in WOA

**Nondestructive cleanliness screening test not available. Must use process-based quality control and periodic quality monitor.**

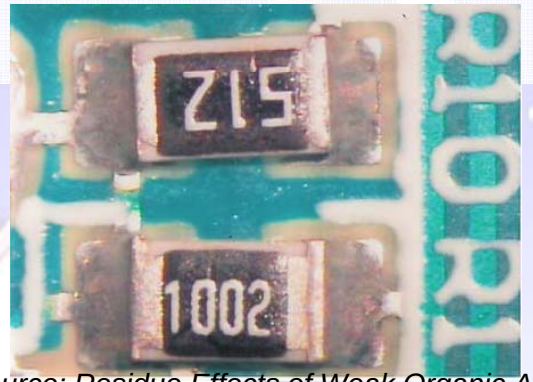



**Photo – High level of WOA flux residue (179 µg/in$^2$) is creating a leakage pathway, but is invisible to the eye.**

*Source: Residue Effects of Weak Organic Acid (WOA) Flux Activators, Foresite, August 2005*

# Measures of Cleanliness

| Test Name | Acronym | Method | Description |
|---|---|---|---|
| Resistance of Solvent Extract | ROSE | IPC-TM-650, 2.3.25 and NASA-STD-8739.2, para. 11.6 | Pass 75/25 IPA/$H_20$ solution over both sides of finished PWA, measure resistivity of solution, >2E6 Ω-cm |
| Sodium Chloride Salt Equivalent Ionic Contamination (Omega Meter) | IC | NASA-STD-8739.2, para 11.7 | Tests cleaning bath using automated equipment and a salt-equivalency standard, <1.55 µg/cm$^2$ (<10 µg/in$^2$) |
| Ion Chromatography | IC | IPC-TM-650, 2.3.28 | Heat sample in 80˚C, 75/25 IPA/$H_20$ solution, 1 hr, [column specified by TM? AS11 column for anion analysis and a CS12A column for cation analysis used on GSFC project]. No established accept/reject standard. |
| Surface Insulation Resistance | SIR | IPC-TM-650, 2.6.3.3 *[8 more test methods identified by DfR]* | Performed on test article, >1E8 Ω after min 168 hrs, standard comb pattern |
| Electrochemical Migration | EM | IPC-TM-650, 2.6.14.1 | Performed on a test article, 10V, 65˚C/88.5% RH, 596 hrs, $IR_{final}$ must not degrade by more than a decade from $IR_{initial}$, no filament growth reducing electrode spacing by >20%, no corrosion |

| Technique | Equivalency Factor |
|---|---|
| ROSE | 1 |
| Omega-Meter | ~1.5 |
| Ion-Chromatography | ~4.0 |

Source: *PCBA Cleanliness Guidelines, C. Hillman, http://www.dfrsolutions.com/uploads/webcasts/PCBA_Cleanliness/index.htm*
*Equivalency factor in last row confirmed by Trace Laboratories in white paper Solvent Extraction Matrix Selection and its Potential Affects on Cleanliness Test Results, K. Sellers, J. Radman, via testing.*

# NASA-STD-8739.2 Cleanliness Test Not Valid for WSF

It is well established that the ROSE and Omega-Meter tests DO NOT detect WOAs. Successfully passing these "cleanliness" tests do not describe remnant WOAs on assembly.
*(water/IPA rinse masks presence of WOAs)*

ROSE and Omega-Meter are suitable for PCB cleanliness testing and for finding halide remnants after soldering. Remnant WOAs do not cause failure directly but significantly increase risk.

Ion Chromatography (IC) is only test that finds WOAs

- No standard accept/reject limits for NASA
- Questions about DI/IPA ratio due to IPA effect on WOA solubility

WOAs change approach to cleanliness assurance:

- item-level testing (screening) is not available
- emphasis falls to production line monitoring
- method of monitoring is time consuming and involves additional expense
  - Lot jeopardy may be larger due to longer time between quality monitor data sets

1/ Solvent Extraction Matrix Selection and its Potential Affects on Cleanliness Test Results, K. Sellers, J. Radman, Trace Laboratories

| Anions | STI Washed [1/] | DfR[2/] | Foresite | GE[2/] | DoD[2/] | IPC[2/] | ACI[2/] | "Medical"[3/] (90/10 DI/IPA) |
|---|---|---|---|---|---|---|---|---|
| Chloride | < 6 | <2 | <2 | <3.5 | <6.1 | <6.1 | <10 | <3 |
| Nitrite | < 3 | <2-4 | | | | | | |
| Sulfate | <3 | | | | | | | <4 |
| Bromide | <10 | <10 | <10 | <10 | <7.8 | <7.8 | <15 | <6 |
| Nitrate | <3 | <2-4 | | | | | | <4 |
| Phosphate | <3 | | | | | | | <4 |
| **Weak Organic Acids** | | <175 | <150 | | | | | <30 |
| Acetate | <3 | | | | | | | <4 |
| Formate | <3 | | | | | | | <4 |
| MSA, Adipic, Succinic (total) | <25 | | | | | | | <2 |
| **Cations** | | | | | | | | |
| Lithium | <3 | | | | | | | |
| Sodium | <3 | | | | | | | <4 |
| Ammonium | <3 | | | | | | | <4 |
| Potassium | <3 | | | | | | | <4 |

All units in µg of ion per $in^2$

Users are establishing their own pass/fail limits while no standard exists

Two regions are used for WOA limits (Max & SPC limits)

1/ Analytical Techniques to Identify Unexpected Contaminants On Electronic Assemblies, K. Freeman, STI Electronics
2/ PCBA Cleanliness Guidelines, C. Hillman, http://www.dfrsolutions.com/uploads/webcasts/PCBA_Cleanliness/index.htm
3/ Solvent Extraction Matrix Selection and its Potential Affects on Cleanliness Test Results, K. Sellers, J. Radman, Trace Laboratories

# How to Resolve Cleanliness Concern?

1. PCB Quality
   a) PCBs must be cleaned prior to soldering for ORxx flux.
   b) Cleanliness testing performed using ROSE or Omega-Meter method
2. Clarify cleanliness requirements in terms of Ion Chromatography test for PWAs using ORxx flux.
   a) Disallow the use of ROSE or Omega-meter test as single option; ok for halide remnants
   b) Specify accept/reject limit, water/IPA ratio
   c) Sampling criteria (suggested test coupon is IPC B-52)
3. Extend control of cleanliness to handling and packaging (cleanrooms, bags, boxes) during period before conformal coating.
4. NASA Standard requires broader understanding of the material and process used (see slide above).

# Summary WSF

- Solder joint voiding has been associated with WSF.
- Sufficient reliability must be established for maximum voiding produced.
- Process quality monitor must be used to keep voiding within acceptance limit.

- WSF does not provide encapsulation buffer between un-reacted flux, remnant halides, and solder pads
- Assurance must be heightened for elimination of halide remnants
- WSF remnants cannot be detected using NASA Std cleanliness test.
- Screening test for WSF remnants is not available. Process monitoring using Ion Chromatography is needed.


Electrostatic
Discharge Safety

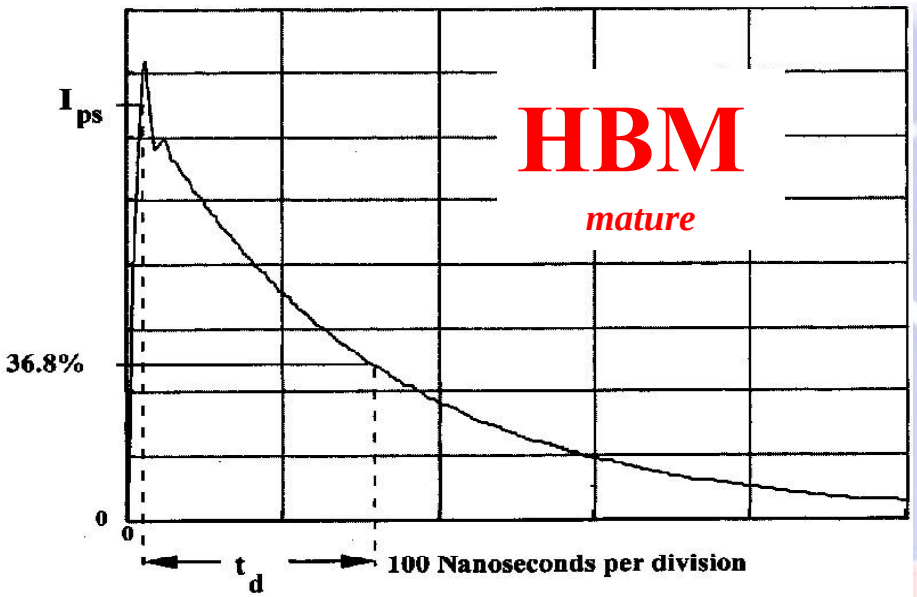
# Overview

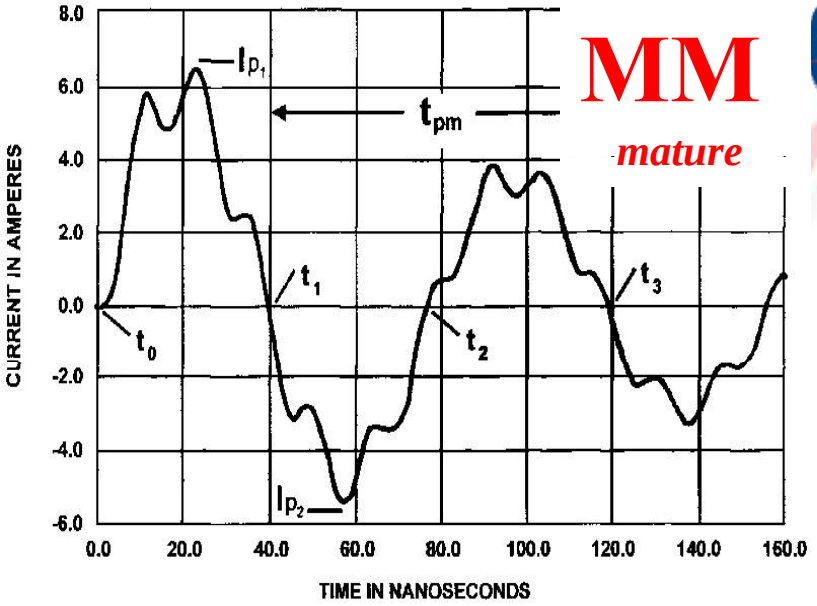
(1) ESD Models Provide a way to characterize the sensitivity of components to ESD

(2) The different ESD models simulate the different environments experienced by electronic components during the manufacturing process.

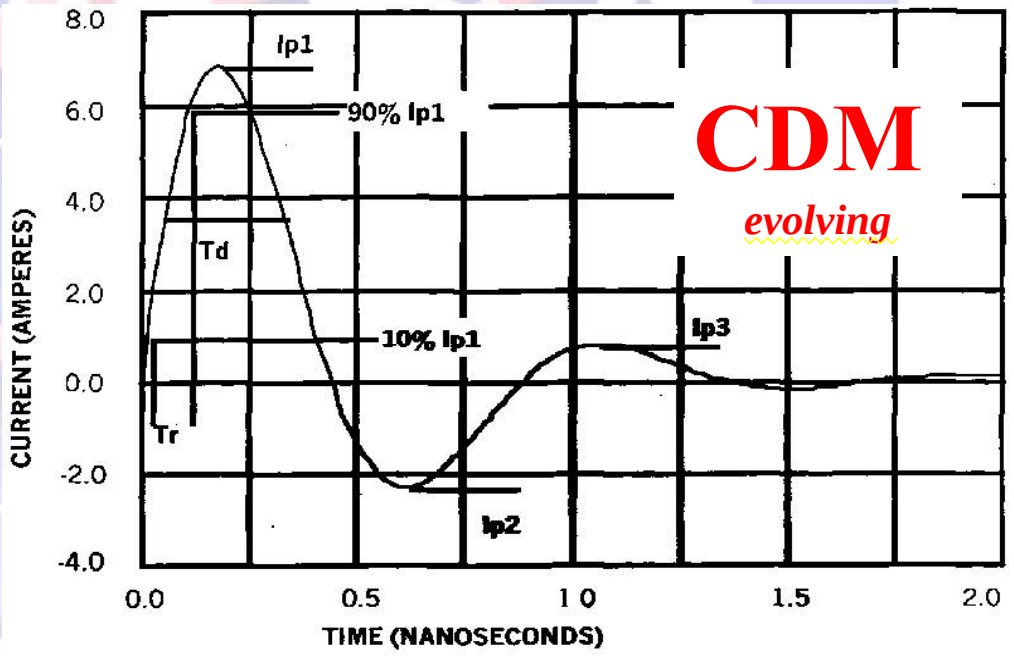
(3) Parts and assemblies may be exposed to more than one type of ESD event over the manufacturing and test life cycle.

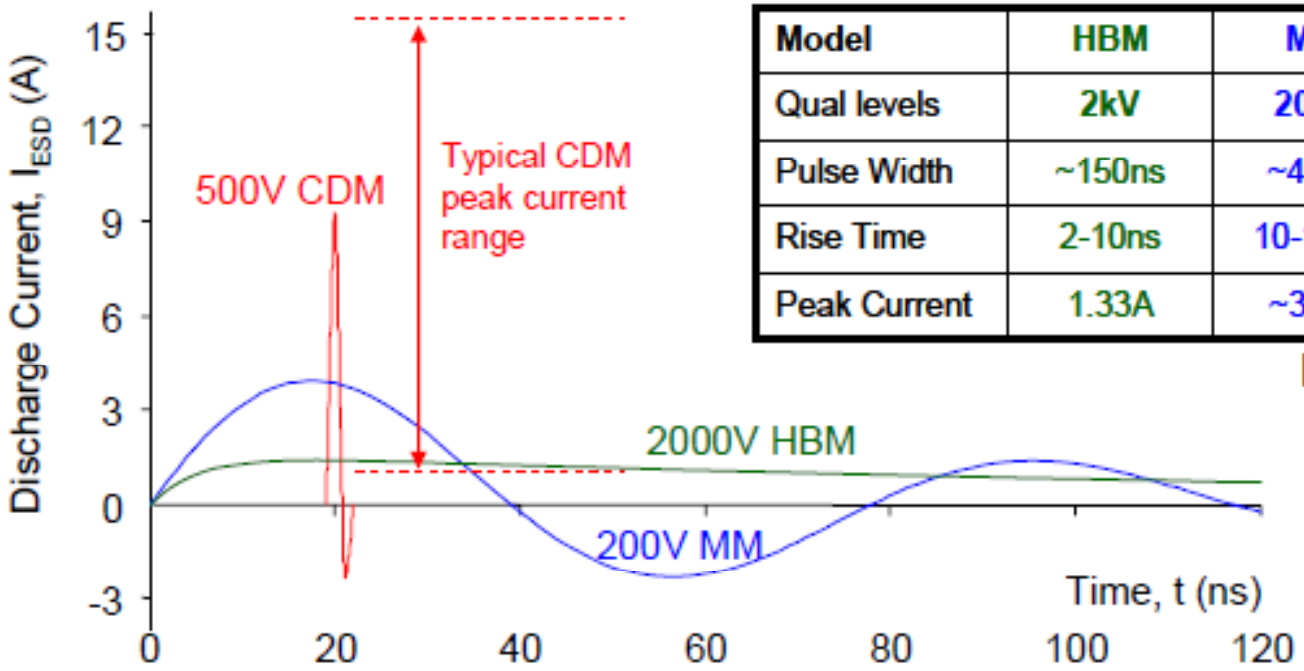
*Courtesy ESP Seattle Inc.*




Voltage discharged through RC or RCL network creates different total energy experienced by the device.






| Model | HBM | MM | CDM |
|---|---|---|---|
| Qual levels | 2kV | 200V | 500V |
| Pulse Width | ~150ns | ~40ns | ~1ns |
| Rise Time | 2-10ns | 10-15ns | 100-500ps |
| Peak Current | 1.33A | ~3.6A | 1-16A |

[Gieser] (modified)

Figure 4: Comparison of current waveforms for CDM, MM, and HBM ESD events.

*White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Industry Council on ESD Target Levels, March 2009*

# ESD Damage Sites are Located Within Semiconductor Die Structure

Damage types can vary depending on event models.

Long, higher Voltage HBM event can look like electrical overstress at die periphery.

Fast, high Current CDM event causes defects in core area which can be latent failures.

Must use advanced FA techniques to locate sites.

*A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices, M. Kelly, G. Servais, T. Diep, S. Twerefour, D. Lin, G. Shah, EOS/ESD Symposium 95*

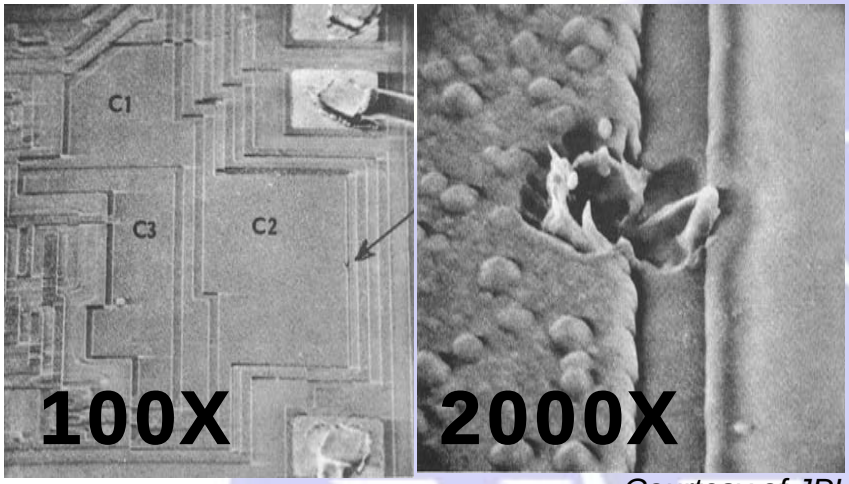
Gate oxide damage

Contact Spiking

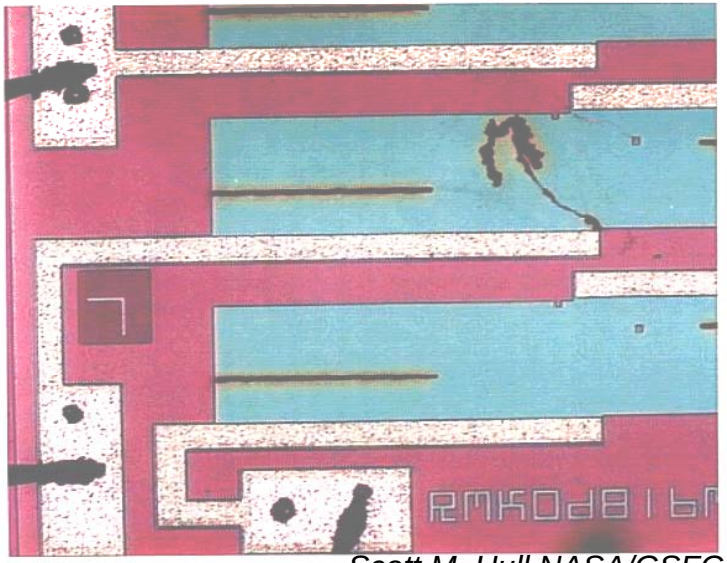
Metal Burn-out

Poly-filament & Poly-extrusion

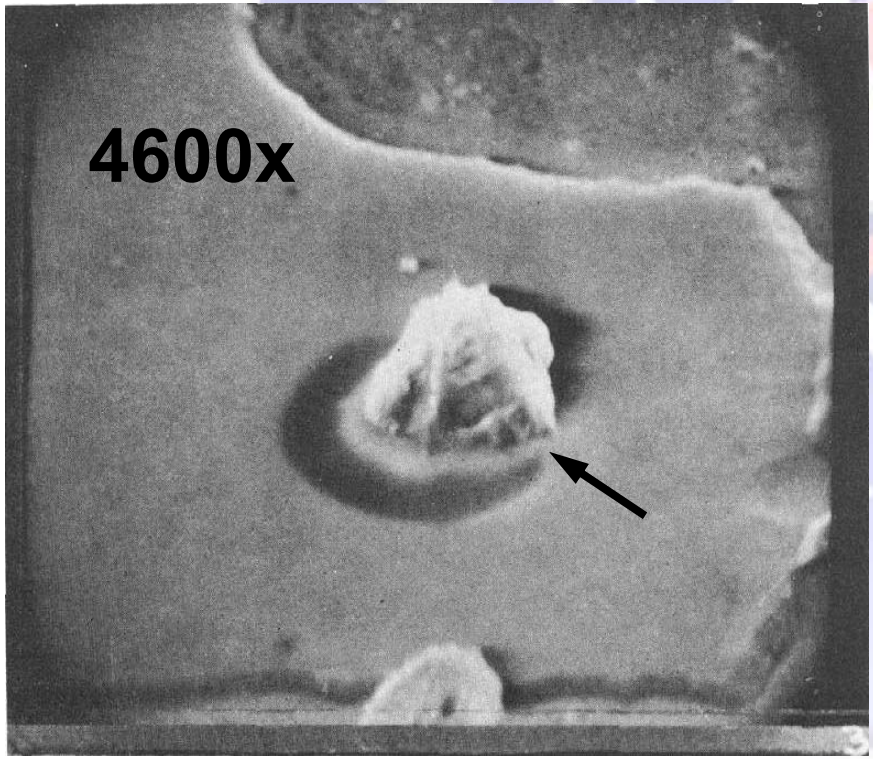
Metal melt filament through a junction




*Courtesy of JPL*



*Scott M. Hull NASA/GSFC*

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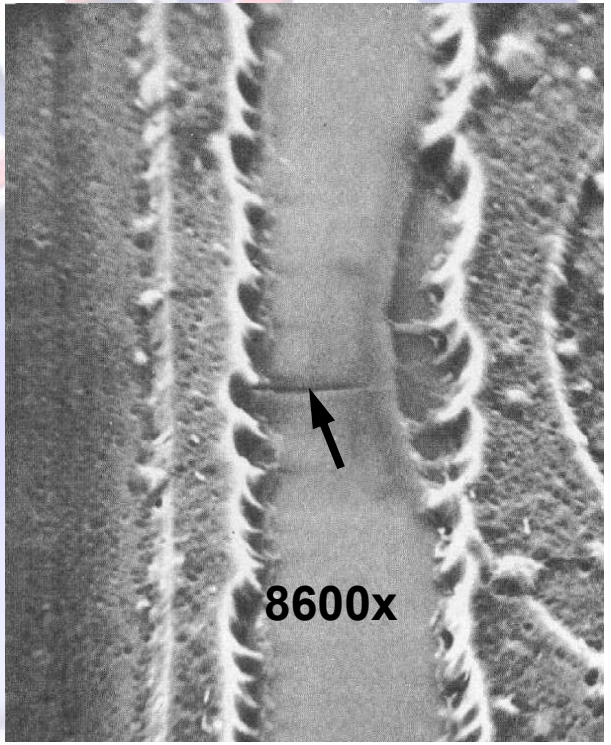



*Courtesy of JPL*

# ESD Event Models

- Three most used models:
  - **Human Body (HBM):** discharging event through the body and the part to ground.
  - **Machine (MM)**: discharge voltage through automated handling equipment or hand-tools and the part to ground.
  - **Charged Device (CDM)**: discharge into or out of a part due to charge accumulation within the part itself.

| Examples of Sources of Threats (charge or discharge path) | HBM | MM | CDM |
|---|---|---|---|
| **Operator** | √ | | |
| **Work bench** | √ | | |
| **Pick and Place Machine** | | √ | |
| **Automatic Test Equipment** | | √ | √ |
| **Device package** | | | √ |
| **Mate/De-mate of harnesses** | | | √ |
| **RF Signals** | | | √ |

# ESD Sensitivity Levels

| Human Body Model | | Machine Model | | Charged Device Model | |
|---|---|---|---|---|---|
| Class 0 | <250 V | Class M1 | < 100 V | Class C1 | < 125 V |
| Class 1A | 250 V to< 500 V | Class M2 | 100 V to < 200 V | Class C2 | 125 V to < 250 V |
| Class 1B | 500 V to < 1 kV | Class M3 | 200 V to < 400 V | Class C3 | 250 V to < 500 V |
| Class 1C | 1 kV to < 2 kV | Class M4 | ≥ 400 V | Class C4 | 500 V to <1 kV |
| Class 2 | 2 kV to < 4 kV | --- | --- | Class C5 | 1 kV to < 1.5 kV |
| Class 3A | 4 kV to < 8 kV | --- | --- | Class C6 | 1.5 kV to < 2 kV |
| Class 3B | ≥ 8 kV | --- | --- | Class C7 | ≥ 2 kV |

***MM correlates to HBM by a factor of 3%-8%***

***CDM does not correlate with the other models and is still evolving***

# *Model Implementation*

- NASA-HDBK-8739.21 (in development) **Guide for Creating an ANSI/ESD S20.20 Implementation Plan**
  - Focus is on HBM: emphasis on operator grounding, dissipative surfaces, reduction in tribocharging
  - For HBM & MM the methods for protective practices and creating protective spaces are highly reproducible and "low tech"
    - Proper implementation requires training and follow-up

*(Every NASA Center should have an ESD Czar)*

- HBM safety methods have brought HBM & MM failures down (now are ~10% of failures encountered industry-wide)

# *Model Implementation*

## Failures continue!

Recent failures of high speed devices (LVDS, FPGAs) drive users to Class 0 HBM…

…But IC manufacturers calculate that about 90% of the failures from the field are due to CDM ESD events.

– CDM-related field returns are associated with low, medium, and high sensitivity devices.

– Safety methods for CDM are highly customized because the model is less mature (many unknown variables and variable relationships, rapidly changing characteristics)

– NASA-HDBK-8739.21 (draft) says ask an expert for help with CDM. (ESDA has several consultants who are members)

# *Special Precautions for Class 0 (NASA-HDBK-8739.21 (draft))*

- Recommended “shalls” related to Class 0 HBM:
  - Dissipative chairs and stools
  - Conductive or dissipative floors or floor mats
  - Relative humidity
  - Ionizers
  - Smocks
  - Mating and de-mating harnesses
  - Soldering irons
  - Signage

# *Class 0 Challenges*

- Higher level of assurance required than Class 1A (Default). Extra oversight is required. Some special equipment may apply.

- Custom assessment and practices may be required for very low levels (<50V). **Arrange for access to expert support in advance** (ESDA has several consultants as members)

Avoid Over-Specifying:

- Will “tie up” work spaces that could be used for less sensitive work.

- Compliance conflicts tend to result when processing less sensitive items at Class 0 stations. Class 1A practice at a Class 0 station can lead to a shut-down of the workstation.

# CDM Challenges

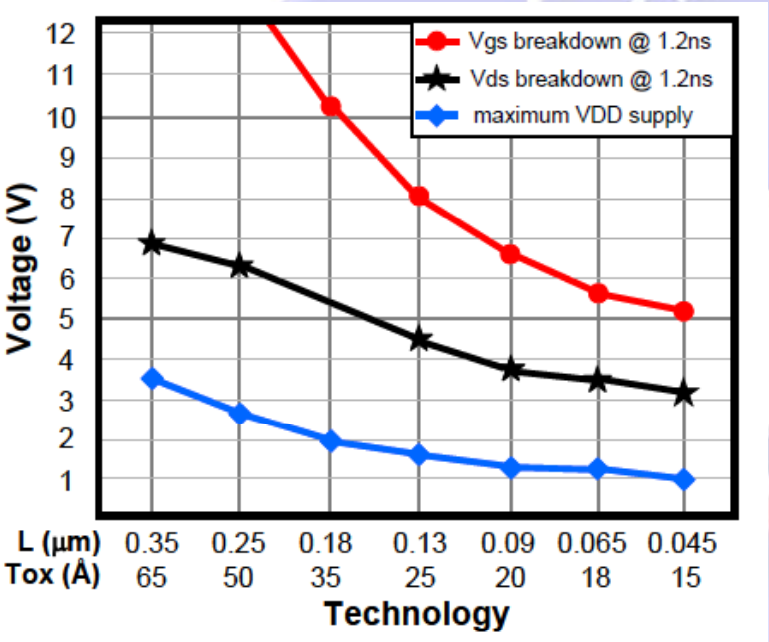
- Opportunities to use on-chip ESD protection reduced in high speed designs
- Reduction in conductor widths on-chip result in higher current densities and thermal stress
- Package capacitances in high pin-count designs increase peak current during CDM ESD event.
- Ionizers work on an HBM time scale and are not effective for mitigating rapid-pulse charging events

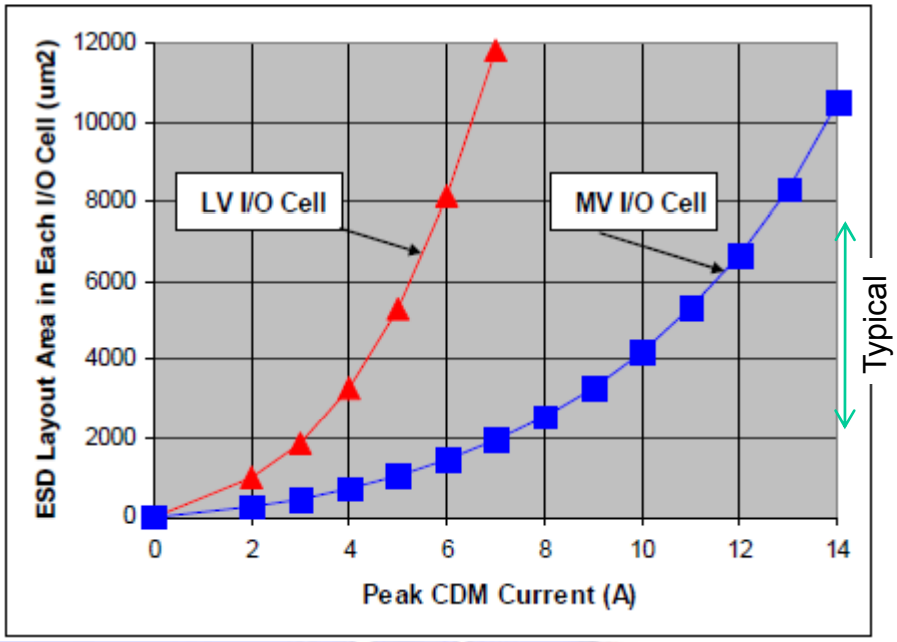
Suppliers have been working to a 500V qualification level for CDM (peak current @ 16A).

Industry position developing to reduce qualification level to 250V (peak current @ 7A). ← *increasing baseline risk*

# CDM Challenges

Gate damage (Vbd) susceptibility is scaling with feature size.

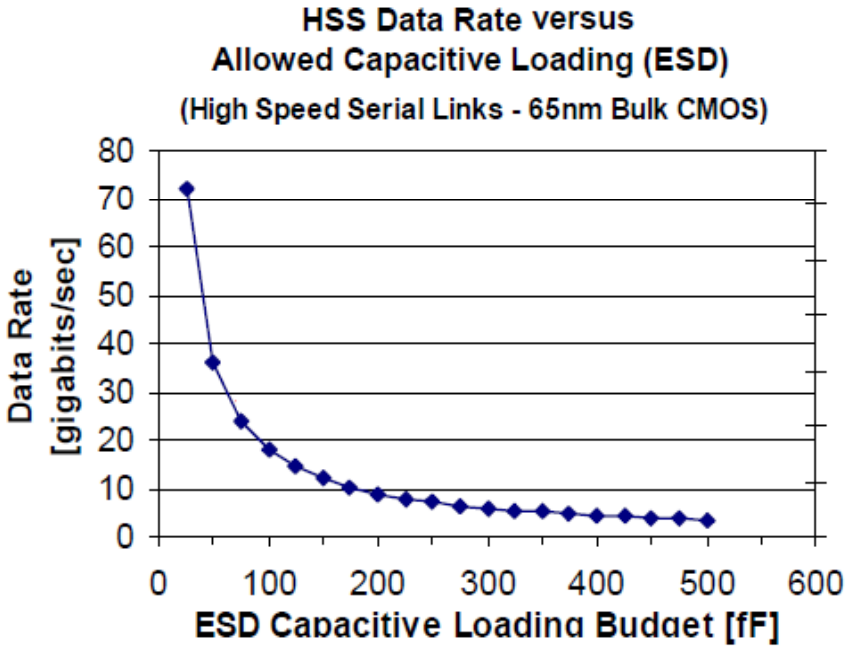


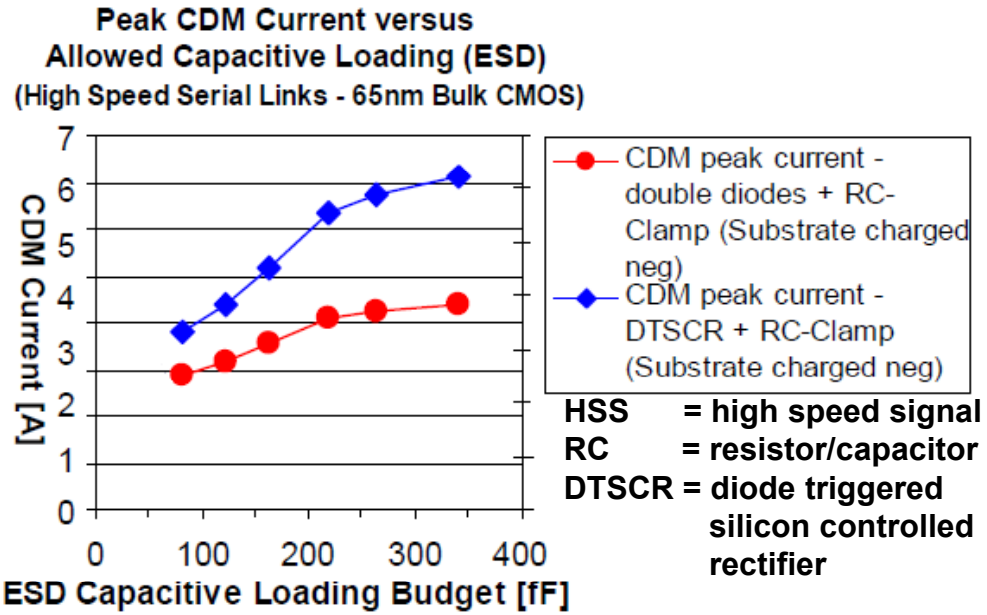




Both are 45 nm technology, LV is Vdd=1.1V, MV is Vdd=1.8V

On-chip ESD protection circuit size scaling up with functional circuitry shrinks (as Vbd ↓).

# CDM Challenges



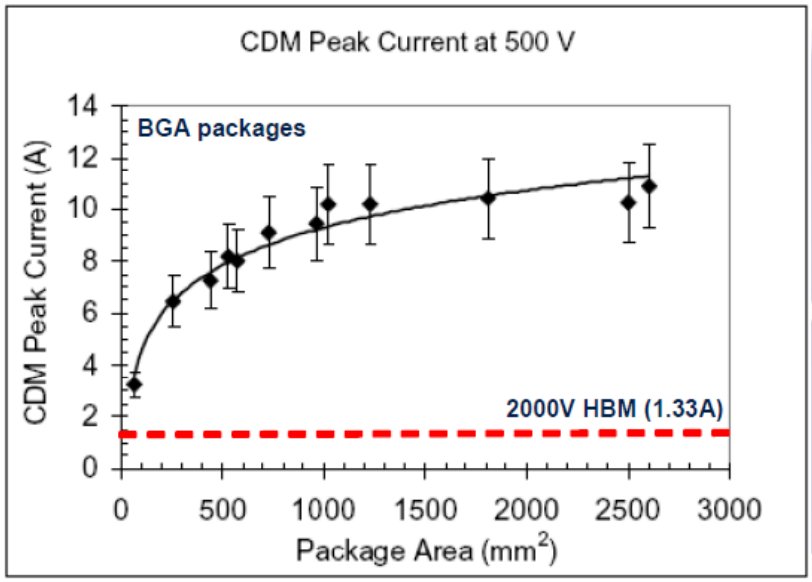




**HSS = high speed signal**
**RC = resistor/capacitor**
**DTSCR = diode triggered silicon controlled rectifier**

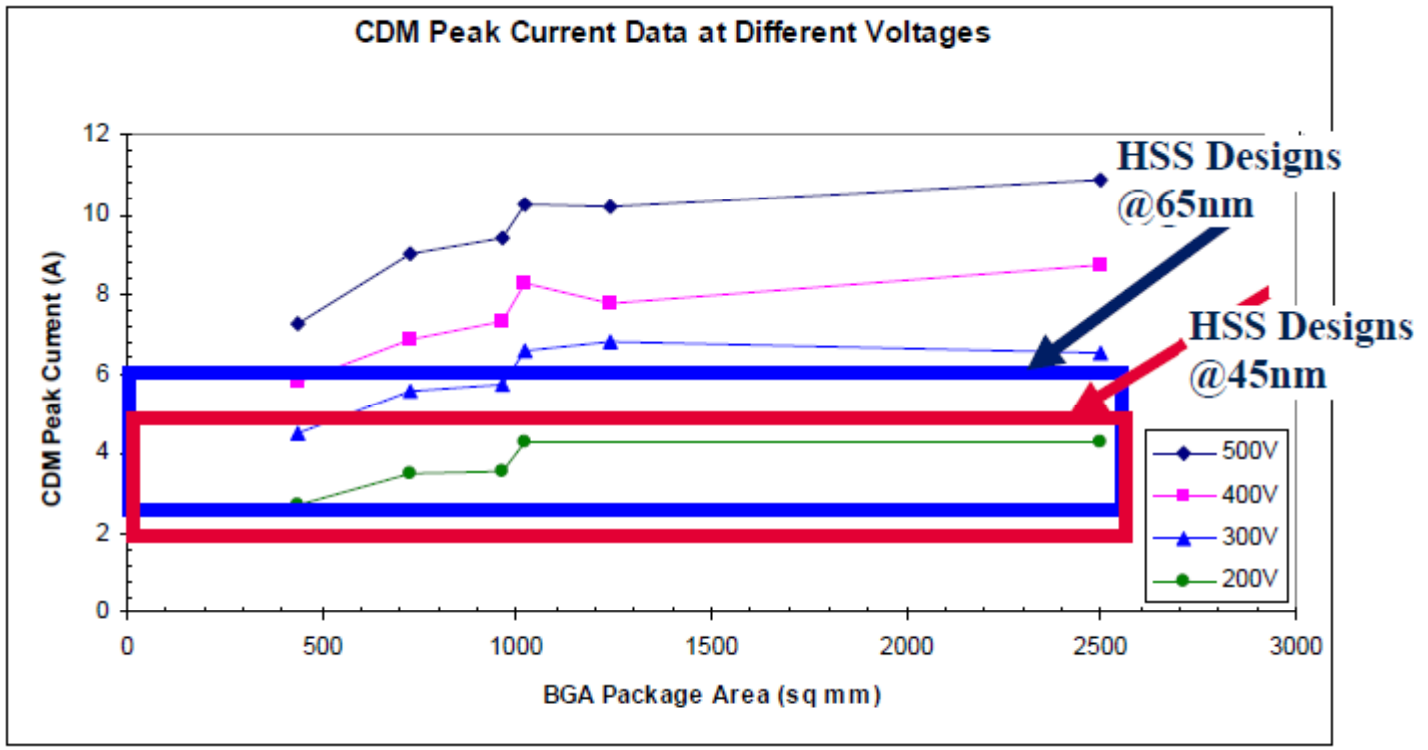
Capacitance must be reduced for high speed operation.

The remaining budget for ESDS circuitry scales downward providing lower levels of ESD protection.

# CDM Challenges




Package size (die size, pin count) causes an increase in CDM event current.



# Summary ESD Issues

- Utilize well understood and proven safety practice for HBM (See NASA-HDBK-8739.21 (draft)).
- Do not use Class 0 as a default safety level. SME help may be required to properly implement Class 0.
- Successful use of HBM & MM safety practices are laying bare CDM susceptibilities.
- Expert help will be needed to work through CDM safety solutions. Complex and evolving event model.
- Technology drivers in high-speed, high pin-count devices make them more susceptible to CDM events.
  - ✓ Suppliers will <u>not</u> “ESD harden” these devices
  - ✓ HBM methods will not protect these devices