Improved On-Chip Measurement of Delay in an FPGA or ASIC

Input and output buffers and the associated delays are eliminated.

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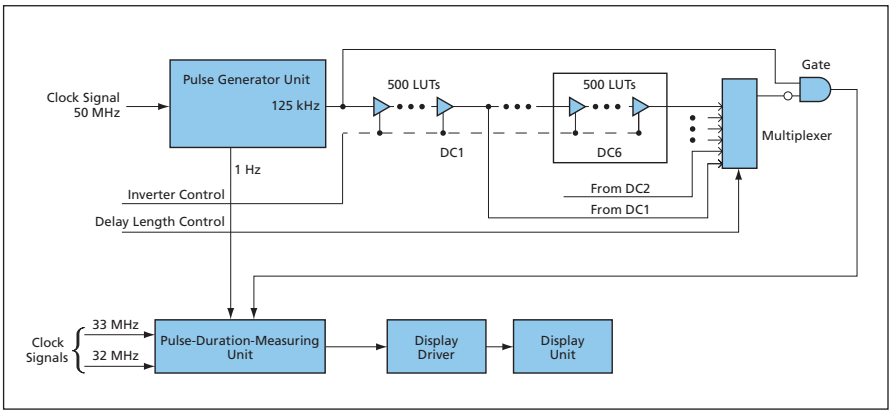
An improved design has been devised for on-chip-circuitry for measuring the delay through a chain of combinational logic elements in a field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC). Heretofore, it has been the usual practice to use either of two other types of on-chip delay-measuring circuits:

- A delay chain of inverters is incorporated into the FPGA or ASIC chip along with an input port for feeding the inverter chain and an output port for feeding a signal to off-chip measurement circuitry. The disadvantage of this design is that the measurement is inaccurate because it includes delays in buffers that are parts of the input and output ports.
- The delay chain is arranged as a ring oscillator. The disadvantage of this design is that the delay chain does not always oscillate as expected.

The improved design overcomes the disadvantages of both older designs. In the improved design, the delay chain does not include input and output buffers and is not configured as an oscillator. Instead, the delay chain is made part of the signal chain of an on-chip pulse generator. The duration of the pulse is measured on-chip and taken to equal the delay.

In this design (see figure) the delay chain comprises six sub-chains denoted DC1 through DC6. Each sub-chain contains 500 lookup tables (LUTs), which are used as universal logic gates that implement the combinational logic in the FPGA or ASIC. The LUTs are programmed to act as either inverters or buffers, depending on the position of a switch on an external circuit board. The output end of each sub-chain except the last one is connected to the input end of the next sub-chain; the output end of each subchain is also connected to one of six input terminals of a multiplexer. By setting of switches in the multiplexer controlled by external circuitry, the length of the delay chain can be set to any value between 500 and 3,000 LUTs in increments of 500 LUTs.



The **Delay Chain** is part of an on-chip instrumentation system that generates pulses and measures their duration. Control and clock signals are generated by external circuitry.

Also on the external board are two crystal-controlled oscillators. One oscillator generates a clock signal at a nominal frequency of 50 MHz; the other generates a clock signal, at a nominal frequency of 33 MHz, which is not synchronized with the 50-MHz signal. The 50-MHz signal is used for the majority of the FPGA logic. The 33-MHz signal is fed to an on-chip pulse-duration-measuring unit.

The on-chip delay-measuring circuitry includes a pulse-generator unit, wherein the 50-MHz signal is divided in frequency to generate two outputs: (1) a 1-pulse-per-second clock signal that is fed to the on-chip pulse-duration-measuring unit and (2) a train of pulses, at frequency of 125 kHz, that is fed as input to the delay chain.

A gate that follows the multiplexer accepts inputs from both ends of the delay chain. In response, the gate generates a 125-kHz train of pulses, the duration of which equals the delay. This pulse train is fed to the pulse-duration-measuring unit. The duration of the pulses in this train is what is measured. The complexity of the pulse-duration-measurement process is such that a complete description is not possible within the space available for this article. It must suffice to summarize by saying that the process involves a combination of sampling the 125-kHz pulses by use of the 33-MHz clock signals during a fixed period of 1 second, counting the numbers of sampling periods during which the pulses are on, then averaging and displaying the result.

This work was done by Yuan Chen, Gary Burke, and Douglas Sheldon of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, NASA Management Office–JPL. Refer to NPO-43348.