# VLSI Design of a Turbo Decoder

**The design is readily adaptable to diverse applications.**

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A very-large-scale-integrated-circuit (VLSI) turbo decoder has been designed to serve as a compact, high-throughput, low-power, lightweight decoder core of a receiver in a data-communication system. In a typical contemplated application, such a decoder core would be part of a single integrated circuit that would include the rest of the receiver circuitry and possibly some or all of the transmitter circuitry, all designed and fabricated together according to an advanced communication-system-on-a-chip design concept.

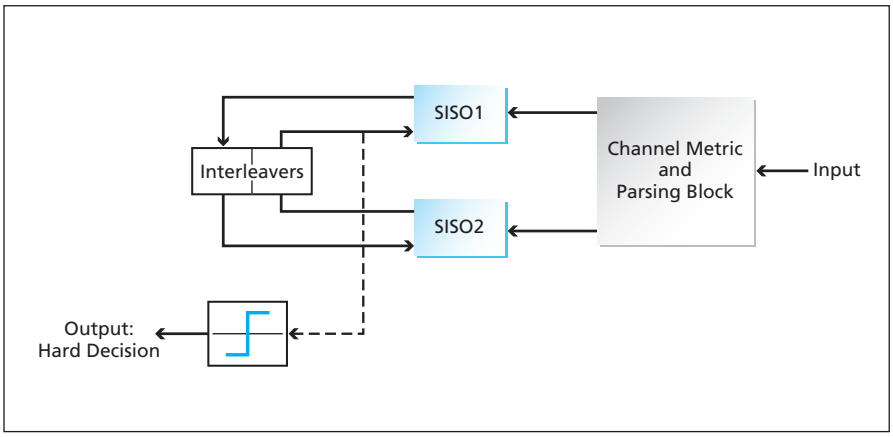
Turbo codes are forward-error-correction (FEC) codes. Relative to older FEC codes, turbo codes enable communication at lower signal-to-noise ratios and offer greater coding gain (closer to the Shannon theoretical limit). In addition, turbo codes can be implemented by relatively simple hardware. Therefore, turbo codes have been adopted as standard for some advanced broadband communication systems.

In general, a turbo encoder is equivalent to two convolutional encoders plus a lookup table that stores interleaver addresses; a turbo decoder (see figure) includes a channel metric and parsing block, two soft-input/soft-output (SISO) decoders (denoted SISO1 and SISO2), and a random-access memory (RAM) for interleaving/deinterleaving functions. The received signal is first processed and parsed through the channel metric and parsing block, the output of which is a sequence of estimates that indicate how closely each received bit is deemed to resemble a one or a zero. On the basis of these estimates, SISO1 makes "soft" decisions: a soft decision is a statement of the probability that each received bit is a one or a zero, based on the preceding sequence of bits.

The soft decisions made by SISO1 are interleaved to be included in the input to SISO2, which then makes soft decisions based on both the estimates from the channel metric and parsing block and the soft decisions from SISO1. These soft decisions are again interleaved and sent as input to SISO1. Now, SISO1 has more information to use than it had on the previous iteration and it strives to use the additional information to make a more accurate decision. The iterative decoding process is repeated either a fixed number of times or until some other criterion is satisfied. Then hard decisions are made on the basis of the soft decisions. Intuitively, if the probability of a zero exceeds that of a one for a given bit, then the hard decision will be that a zero was transmitted.

A description of the practical implementation of the above-described decoder architecture in terms of functional blocks of circuitry, the functions (including memory reading and writing, calculations, and comparisons) performed by the blocks, and timing of the functions would greatly exceed the space available for this article. It must suffice to summarize by reporting that some details of the architecture of the implementation are especially important for the overall design: The details in question include those of the timing of memory reading and writing operations, a finite state machine in each SISO decoder, a module in each SISO decoder that performs forward and backward calculations, a module in each SISO decoder that performs the soft-output calculations, and the interleaver/deinterleaver module.

Overall, the design of the decoder is paramaterizable: that is, by adjusting the parameters of an otherwise generic design, one can modify the design to fit into such communication-on-a-system products as transceivers in satellite communication systems, transceivers in wireless local-area networks, digital television receivers, cable modems, digital video broadcast receivers, and digital subscriber lines. A prototype of the decoder has been implemented in a field-programmable gate array (FPGA) chip that performs forward error correction on data streaming at a rate of 15 Mb/s while consuming a power of only 0.1 W.




A **Turbo Decoder** engages in an iterative process in which incoming data are considered along with prior soft decisions in an effort to reach more accurate hard decisions concerning received bits. A paramaterizable design for a practical decoder has been implemented in an FPGA.

*This work was done by Wai-Chi Fang of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).*

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