

merically equal to the current that, flowing during a charge or discharge time of one hour, would integrate to the nominal charge or discharge capacity of a cell). This limitation has been attributed to the low electronic conductivity of CF_x for $x \approx 1$. To some extent, the limitation might be overcome by making cathodes thinner, and some battery manufacturers have obtained promising results using thin cathode structures in spiral configurations.

The present approach includes not only making cathodes relatively thin [≈ 2 mils (≈ 0.051 mm)] but also using sub-fluorinated CF_x cathode materials ($x < 1$) in conjunction with electrolytes formulated for use at low temperatures. The reason for choosing sub-fluorinated CF_x cathode materials is that their electronic conductivities are high, relative to those for which $x > 1$. It was known from recent prior research that cells containing sub-fluorinated CF_x cathodes (x between 0.33 and 0.66) are capable of retaining substantial portions of their nominal low-current specific energies when discharged at rates as high as 5C at room tempera-

ture. However, until experimental cells were fabricated following the present approach and tested, it was not known whether or to what extent low-temperature performance would be improved.

For the experimental cells, cathodes were fabricated by spray deposition of multiple layers of cathode mixtures onto roughened 1-mil (≈ 0.025 -mm)-thick aluminum-foil current collectors. Each cathode mixture consisted of a CF_x powder and carbon black suspended in a binder/solvent solution of poly(vinylidene fluoride) in N-methyl-2-pyrrolidone. For some of the cells, the CF_x was sub-fluorinated by various amounts ($x = 0.53$ or $x = 0.65$). For other cells, used as controls, a fully fluorinated industrial CF_x ($x = 1.08$) was used.

Each resulting cathode structure, 1 to 3 mils (about 0.025 to 0.076 mm) thick, was vacuum furnace dried, then incorporated into a standard coin cell case along with a separator, lithium foil anode, and an electrolyte consisting of $LiBF_4$ dissolved at a concentration of 0.5 M in an 80/20 DME/PC (dimethoxy ethane/propylene carbon-

ate) solvent mixture. The cells were tested in galvanostatic discharges at room temperature and -40 °C at currents from 2C to C/40. The fully fluorinated and sub-fluorinated cells performed comparably at rates as high as 2C at room temperature. At -40 °C, the sub-fluorinated cells exhibited approximately 3 times the specific capacities of the fully fluorinated cells when discharged at C/10 and C/5 discharge rates (see figure).

This work was done by Jay Whitacre, Ratanakumar Bugga, Marshall Smart, G. Prakash, and Rachid Yazami of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-43219, volume and number of this NASA Tech Briefs issue, and the page number.

G⁴-FETs as Universal and Programmable Logic Gates

Logic functions could be implemented using fewer active circuit elements.

NASA's Jet Propulsion Laboratory, Pasadena, California

An analysis of a patented generic silicon-on-insulator (SOI) electronic device called a G⁴-FET has revealed that the device could be designed to function as a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer discrete components than are required for conventional transistor-based circuits performing the same logic functions.

A G⁴-FET is a combination of a junction field-effect transistor (JFET) and a metal oxide/semiconductor field-effect transistor (MOSFET) superimposed in a single silicon island and can therefore be regarded as two transistors sharing the same body. A G⁴-FET can also be regarded as a single transistor having four gates: two side junction-based gates, a top MOS gate, and a back gate activated by biasing of the SOI substrate. Each of these gates can be used to control the conduction characteristics of the transistor; this possibility creates new options for designing analog,

radio-frequency, mixed-signal, and digital circuitry.

With proper choice of the specific dimensions for the gates, channels, and ancillary features of the generic G⁴-FET, the device could be made to function as a three-input, one-output logic gate. As illustrated by the truth table in the top part of the figure, the behavior of this logic gate would be the inverse (the NOT) of that of a majority gate. In other words, the device would function as a NOT-majority gate. By simply adding an inverter, one could obtain a majority gate. In contrast, to construct a majority gate in conventional complementary metal oxide/semiconductor (CMOS) circuitry, one would need four three-input AND gates and a four-input OR gate, altogether containing 32 transistors.

The middle part of the figure schematically depicts three ways of realizing an inverter (NOT gate), two ways of realizing an AND gate, and two ways of realizing an OR gate by use of one or two NOT-majority gates. In addition

(not shown in the figure), by using one of the three inputs as a programming or control input that is set to 0 or 1, a NOT-majority could be made to respond to the other inputs as either a NAND or a NOR gate, respectively. Inasmuch as the sets {NOT,AND}, {NOT,OR}, and {NAND,NOR} have previously been shown to be universal (in the sense that any digital computation or logic function could be realized by use of suitable combinations of members of these sets), the possibility of realizing these sets signifies that the NOT-majority gate is also universal.

The bottom part of the figure depicts a full adder, implemented by use of three NOT-majority gates and two inverters, that would put out two one-bit binary numbers in response to three input one-bit binary numbers. The design of this adder exploits the possibility of switching a NOT-majority gate between NAND and NOR functionality to minimize the number of gates needed. In contrast, the simplest implementation of

an equivalent full adder based on Boolean gates would include nine NAND gates and four inverters.

This work was done by Travis Johnson, Amir Fijany, Mohammad Mojarradi, Farrokh Vatan, Nikzad Toomarian, Elizabeth Kolawa, Sorin Cristoloveanu, and Benjamin Blalock of Caltech for NASA's Jet Propulsion

Laboratory. Further information is contained in a TSP (see page 1).

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