pletely supports the redundancy in spacecraft design, allowing for a complete RFR to fail. This design reduces the mass of the bus by incorporating both the Control Unit and the Data Unit in the same hardware.

The standard uses ATM (asynchronous transfer mode) packets, standardized by ITU-T, ANSI, ETSI, and the ATM Forum. The IEEE-1393 standard uses the UNI form of the packet and provides no protection for the data portion of the cell. The JPL design adds optional formatting to this data portion. This design extends fault protection beyond that of the interconnect. This includes adding protection to the data portion that is contained within the Bus Interface Units (BIUs) and by adding to the signal interface between the Data Host and the JPL 1393 Ring Bus. Data transfer on the ring bus does not involve a master or initiator. Following bus protocol, any BIU may transmit data on the ring whenever it has data received from its host. There is no centralized arbitration or bus granting.

The JPL design provides for autonomous synchronization of the nodes on the ring bus. An address-synchronous latency adjust buffer (LAB) has been designed that cannot get out of synchronization and needs no external input. Also, a priority-driven cable selection behavior has been programmed into each unit on the ring bus. This makes the bus able to connect itself up, according to a maximum redundancy priority system, without the need for computer intervention at startup. Switching around a failed or switched-off unit is also autonomous. The JPL bus provides a map of all the active units for the host computer to read and use for fault management.

With regard to timing, this enhanced bus recognizes coordinated timing on a spacecraft as critical and addresses this with a single source of absolute and relative time, which is broadcast to all units on the bus with synchronization maintained to the tens of nanoseconds. Each BIU consists of up to five programmable triggers, which may be programmed for synchronization of events within the spacecraft of instrument. All JPL-formatted data transmitted on the ring bus are automatically time-stamped.

This work was done by Terry Wysocky; Edward Kopf, Jr.; Sunant Katanyoutanant; Carl Steiner; and Harry Balian of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-42112

Nanoionics-Based Switches for Radio-Frequency Applications

These switches might supplant semiconductor and MEMS switches in some applications.

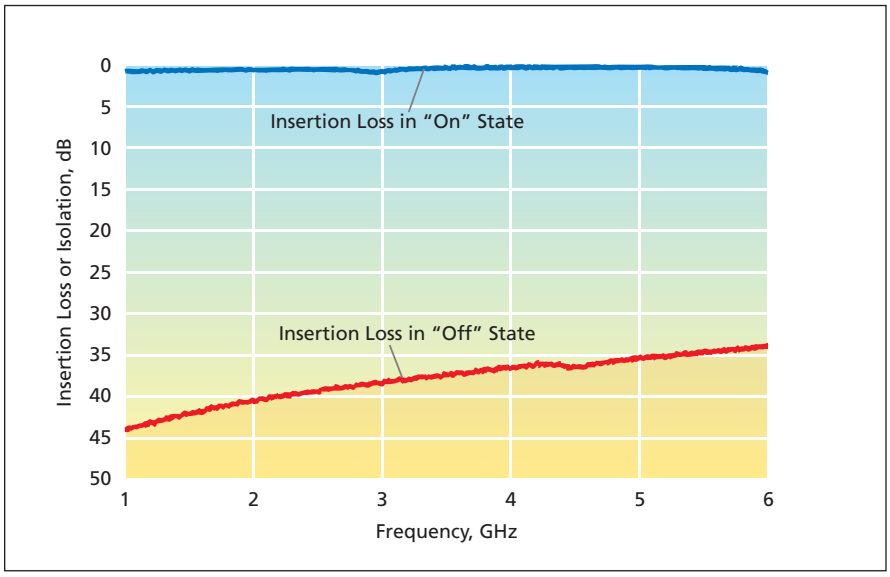
John H. Glenn Research Center, Cleveland, Ohio

Nanoionics-based devices have shown promise as alternatives to microelectromechanical systems (MEMS) and semiconductor diode devices for switching radio-frequency (RF) signals in diverse systems. Examples of systems that utilize RF switches include phase shifters for electronically steerable phased-array antennas, multiplexers, cellular telephones and other radio transceivers, and other portable electronic devices.

Semiconductor diode switches can operate at low potentials (about 1 to 3 V) and high speeds (switching times of the order of nanoseconds) but are characterized by significant insertion loss, high DC power consumption, low isolation, and generation of third-order harmonics and intermodulation distortion (IMD). MEMS-based switches feature low insertion loss (of the order of 0.2 dB), low DC power consumption (picowatts), high isolation (>30 dB), and low IMD, but contain moving parts, are not highly reliable, and must be operated at high actuation potentials (20 to 60 V) generated and applied by use of complex circuitry. In addition, fabrication of MEMS is complex, involving many processing steps.

Nanoionics-based switches offer the superior RF performance and low power consumption of MEMS switches, without need for the high potentials and complex circuitry necessary for operation of MEMS switches. At the same time, nanoionics-based switches offer the high switching speed of semiconductor devices. Also, like semiconductor devices, nanoionics-based switches can be fabricated relatively inexpensively by use of conventional integrated-circuit fabrication techniques. Moreover, nanoionics-based switches have simple planar structures that can easily be integrated into RF power-distribution circuits.

Nanoionics-based switches exploit the properties of some amorphous materials (in particular, chalcogenide glasses) that can incorporate relatively large amounts of metal and behave as solid electrolytes. The ionic conductivity of such a material can be of the same order of magnitude as the electronic conductivity of a semiconductor. Under appropriate bias con-



Insertion Loss and Isolation — two key switch characteristics — were measured in a test of a nanoionics-based switch over the frequency range of 1 to 6 GHz. The switch characteristics plotted here are comparable and/or superior to those of MEMS and semiconductor switches.

ditions (typically between 1 and 3 V), ions of a metal (silver) are formed at an anode made of that metal and migrate into the solid electrolyte while electrons (typically at a current of the order of microamperes to milliamperes) are injected from an electrochemically inert (nickel) cathode into the solid electrolyte. The injected electrons reduce the metal anions in the solid electrolyte, thereby causing the growth of metal nanowires through the electrolyte from the cathode to the corresponding anode.

Once a nanowire has grown sufficiently to form an electrically conductive path between the electrodes, there is no need to continue to apply electric power to maintain the connection. The process of making the connection can be easily reversed by applying a reverse bias to reoxidize the metal atoms in the solid electrolyte to recreate the insulating amorphous layer. Thus, a nanoionics-based switch is a reversible electrochemical switch that can have geometric features as small as nanometers. The process time for making or breaking the connection is about a nanosecond.

Experimental nanoionics based-switches having several different configurations have been built and tested in a continuing effort to gain understanding of the underlying chemical and physical principles and optimize designs. Fabrication of each experimental switch began with deposition of a binary chalcogenide glass on a high-resistivity silicon wafer. Next, a layer of silver was deposited on the glass and exposed to ultraviolet light to induce a photodissolution process in which silver ions migrated into the glass matrix. Then an electrode of silver and an electrode of nickel were deposited on the chalcogenide layer.

The figure shows plots of data from a test of one of the experimental switches. Over the frequency range from 1 to 6 GHz, the insertion loss of the switch in the "on" state was less than 0.5 dB, while the isolation in the "off" state exceeded 30 dB.

This work was done by James Nessel and Richard Lee of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18313-1.

Lunar Dust-Tolerant Electrical Connector

John H. Glenn Research Center, Cleveland, Ohio

An electrical connector was developed that is tolerant of the presence of lunar dust. Novel features of the connector include the use of a permeable membrane to act both as a dust barrier and as a wiper to limit the amount of dust that makes its way into the internal chamber of the connector. The development focused on the Constellation lunar extravehicular activity (EVA) spacesuit's portable life support system (PLSS) battery recharge connector; however, continued research is applying this technology to other lunar surface systems such as lunar rover subsystems and cryogenic fluid transfer connections for *in-situ* resource utilization (ISRU) applications.

Lunar dust has been identified as a significant and present challenge in future exploration missions. In addition to posing contamination and health risks for human explorers, the interlocking, angular nature of lunar dust and its broad grain size distribution make it particularly harmful to mechanisms with which it may come into contact. All Apollo lunar missions experienced some degree of equipment failure because of dust, and it appears that dust accumulation on exposed material is unavoidable and difficult to reverse. Both human EVA and ISRU activities are on the mission horizon and are paramount to the establishment of a permanent human base on the Moon. Reusable and dust-tolerant connection mechanisms are a critical component for mission success.

The need for dust-tolerant solutions is also seen in utility work and repair, mass transit applications, construction, mining, arctic and marine environments, diving (search and rescue), and various operations in deserts, where dust or sand clogging and coating different mechanisms and connections may render them difficult to operate or entirely inoperable.

This work was done by Jason Herman, Shazad Sadick, and Dustyn Roberts of Honeybee Robotics Spacecraft Mechanisms Corporation for Glenn Research Center.

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18400-1.

Compact, Reliable EEPROM Controller

This controller prevents inadvertent writes in an EEPROM.

Goddard Space Flight Center, Greenbelt, Maryland

A compact, reliable controller for an electrically erasable, programmable read-only memory (EEPROM) has been developed specifically for a space-flight application. The design may be adaptable to other applications in which there are requirements for reliability in general and, in particular, for prevention of inadvertent writing of data in EEPROM cells.

Inadvertent writes pose risks of loss of reliability in the original space-flight application and could pose such risks in other applications. Prior EEPROM controllers are large and complex and do not provide all reasonable protections (in many cases, few or no protections) against inadvertent writes. In contrast, the present controller provides several layers of protection against inadvertent writes. The controller also incorporates a write-time monitor, enabling determination of trends in the performance of an EEP-