Reconfigurable Hardware for Compressing Hyperspectral Image Data

Multiple hardware cores can be combined to increase throughput.

NASA's Jet Propulsion Laboratory, Pasadena, California

High-speed, low-power, reconfigurable electronic hardware has been developed to implement ICER-3D, an algorithm for compressing hyperspectral-image data. The algorithm and parts thereof have been the topics of several *NASA Tech Briefs* articles, including "Context Modeler for Wavelet Compression of Hyperspectral Images" (NPO-43239) and "ICER-3D Hyperspectral Image Compression Software" (NPO-43238), which appear elsewhere in this issue of *NASA Tech Briefs*. As described in more detail in those articles, the algorithm includes three main subalgorithms: one for computing wavelet transforms, one for context modeling, and one for entropy encoding. For the purpose of designing the hardware, these subalgorithms are treated as modules to be implemented efficiently in field-programmable gate arrays (FPGAs).

The design takes advantage of industry-standard, commercially available FPGAs. The implementation targets the Xilinx Virtex II pro architecture, which has embedded PowerPC processor cores with flexible on-chip bus architecture. It incorporates an efficient parallel and pipelined architecture to compress the three-dimensional image data. The design provides for internal buffering to minimize intensive input/output operations while making efficient use of off-chip memory. The design is scalable in that the subalgorithms are implemented as independent hardware modules that can be combined in parallel to increase throughput. The on-chip processor manages the overall operation of the compression system, including execution of the top-level control functions as well as scheduling, initiating, and monitoring processes.

The design prototype has been demonstrated to be capable of compressing hyperspectral data at a rate of 4.5 megasamples per second at a conservative clock frequency of 50 MHz, with a potential for substantially greater throughput at a higher clock frequency. The power consumption of the prototype is less than 6.5 W.

The reconfigurability (by means of reprogramming) of the FPGAs makes it possible to effectively alter the design to some extent to satisfy different requirements without adding hardware. The implementation could be easily propagated to future FPGA generations and/or to custom application-specific integrated circuits.

This work was done by Nazeeh Aranki, Jeffrey Namkung, Carlos Villalpando, Aaron Kiely, Matthew Klimesh, and Hua Xie of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-42834

Spatio-Temporal Equalizer for a Receiving-Antenna Feed Array

Suppression of multipath effects and robust pointing would be achieved.

NASA's Jet Propulsion Laboratory, Pasadena, California

A spatio-temporal equalizer has been conceived as an improved means of suppressing multipath effects in the reception of aeronautical telemetry signals, and may be adaptable to radar and aeronautical communication applications as well. This equalizer would be an integral part of a system that would also include a seven-element planar array of receiving feed horns centered at the focal point of a paraboloidal antenna that would be nominally aimed at or near the aircraft that would be the source of the signal that one seeks to receive (see Figure 1). This spatio-temporal equalizer would consist mostly of a bank of seven adaptive finite-impulse-response (FIR) filters — one

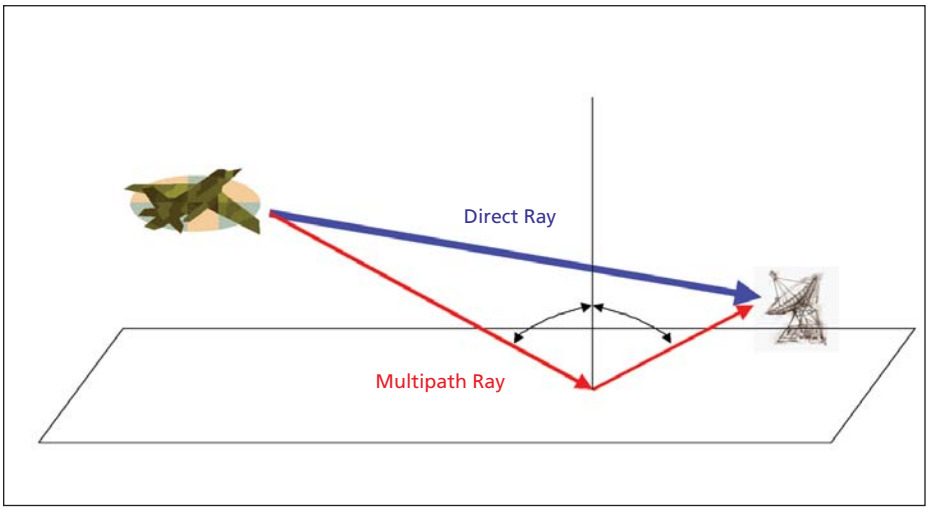

Figure 1. **Signals Received by a Focal-Plane Array** of feed horns would be processed by the spatio-temporal equalizer to suppress multipath effects and extract antenna-pointing information.

for each element in the array — and the outputs of the filters would be summed (see Figure 2). The combination of the spatial diversity of the feed-horn array and the temporal diversity of the filter bank would afford better multipath-suppression performance than is achievable by means of temporal equalization alone.

The seven-element feed array would supplant the single feed horn used in a conventional paraboloidal ground telemetry-receiving antenna. The radio-frequency telemetry signals received by the seven elements of the array would be digitized, converted to complex baseband form, and sent to the FIR filter bank, which would adapt itself in real time to enable reception of telemetry at a low bit error rate, even in the presence of multipath of the type found at many flight test ranges.

Each channel (comprising the signal-processing chain for a receiving feed horn) would contain an N-stage FIR filter. The incoming complex baseband signal in the ith channel at the nth sampling instant is denoted by $y_i(n)$. A filter weight at that instant is denoted generally by $w_{i,j}(n)$, where i is the index number of the channel ($1 \leq i \leq 7$) and j is the index number of the filter stage ($0 \leq j \leq N-1$). The signal-combining operation at the summation (output) point of the FIR filter bank is given by

$$z(n) = \sum_{i=1}^{7} \sum_{j=0}^{N-1} w^{*}_{i,j}(n) y_i(n-j),$$

where $w_{i,0} \equiv 1$. The weights would be adapted by an algorithm known in the art as the constant-modulus algorithm, embodied in the following equation:

$$w_{i,j}(n+1) = w_{i,j}(n) + \alpha y_i(n-j) z^{*}(n) [1 - |z(n)|^2],$$

where α is an adaptation rate parameter.

In addition, the combination of the array and the filter bank would make it possible to extract, in real time, pointing information that could be used to identify both the main beam traveling directly from the target aircraft and the beam that reaches the antenna after reflection from the ground: Information on the relative amplitudes and phases of the incoming signals, which information would be indicative of the difference between the antenna pointing direction and the actual directions of the direct and reflected beams, would be contained in the adaptive FIR weights. This information would be fed to a pointing estimator, which would generate instantaneous estimates of the difference between the antenna-pointing and target directions. The time series of these estimates would be sent to a set of Kalman filters, which would perform smoothing and prediction of the time series and extract velocity and acceleration estimates from the time series. The outputs of the Kalman filters would be sent to a unit that would control the pointing of the antenna, enabling robust pointing even in the presence of multipath.

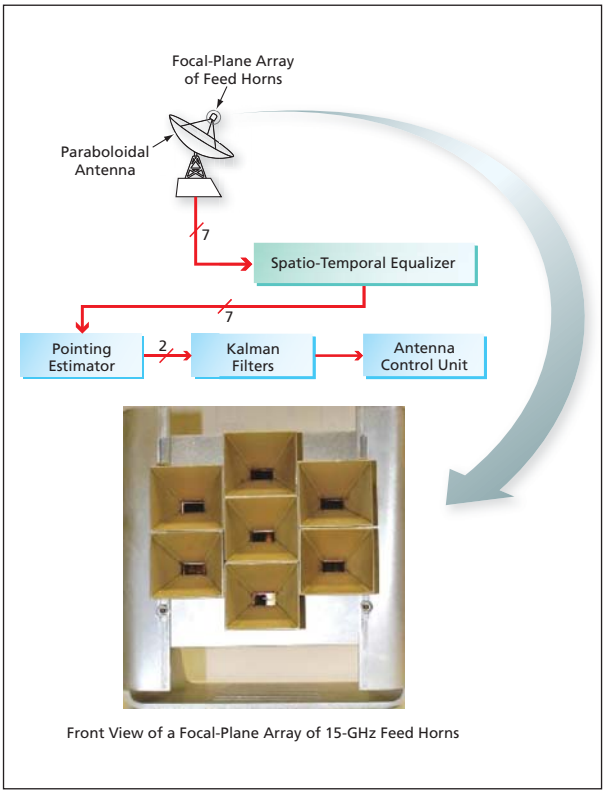

Figure 2. **Seven FIR Filters** would process the seven incoming signals, and the outputs of the filters would be summed.

The performances of several receiving systems with and without multipath and both with and without several conceptual versions of the spatio-temporal equalizer have been demonstrated in computational simulations. It was planned to begin construction of a breadboard version of the spatio-temporal equalizer at or about the time of writing this article.

This work was done by Ryan Mukai, Dennis Lee, and Victor Vilnrotter of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, NASA Management Office–JPL. Refer to NPO-43077.

High-Speed Ring Bus

The ring bus is an enhancement of the general high-speed spacecraft bus.

NASA's Jet Propulsion Laboratory, Pasadena, California

The high-speed ring bus at the Jet Propulsion Laboratory (JPL) allows for future growth trends in spacecraft seen with future scientific missions. This innovation constitutes an enhancement of the 1393 bus as documented in the Institute of Electrical and Electronics Engineers (IEEE) 1393-1999 standard for a spaceborne fiber-optic data bus. It allows for high-bandwidth and time synchronization of all nodes on the ring. The JPL ring bus allows for interconnection of active units with autonomous operation and increased fault handling at high bandwidths. It minimizes the flight software interface with an intelligent physical layer design that has few states to manage as well as simplified testability. The design will soon be documented in the AS-1393 standard (Serial Hi-Rel Ring Network for Aerospace Applications).

The framework is designed for "Class A" spacecraft operation and provides redundant data paths. It is based on "fault containment regions" and "redundant functional regions (RFR)" and has a method for allocating cables that com-