differing power needs, this supply also has a secondary power bus, which can be programmed *a priori* or on-the-fly to boost the primary battery voltage level from 24 to 50 V to accommodate various loads as they are brought on line. Through voltage and current monitoring, the device can also shield the charging source from overloads, keep it within safe operating modes, and can meter available power to the application and maintain safe operations.

*This work was done by Michael J. Krasowski, Lawrence C. Greer, and Norman F. Prokop of Glenn Research Center and Joseph M. Flatico of Ohio Aerospace Institute. Further information is contained in a TSP (see page 1).*

*Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18317-1.*

# Parallel Processing of Broad-Band PPM Signals

## Timing-error correction is independent of timing-error estimation.

*NASA's Jet Propulsion Laboratory, Pasadena, California*

A parallel-processing algorithm and a hardware architecture to implement the algorithm have been devised for time-slot synchronization in the reception of pulse-position-modulated (PPM) optical or radio signals. As in the cases of some prior algorithms and architectures for parallel, discrete-time, digital processing of signals other than PPM, an incoming broadband signal is divided into multiple parallel narrower-band signals by means of sub-sampling and filtering. The number of parallel streams is chosen so that the frequency content of the narrower-band signals is low enough to enable processing by relatively-low-speed complementary metal oxide semiconductor (CMOS) electronic circuitry.

The algorithm and architecture are intended to satisfy requirements for time-varying time-slot synchronization and post-detection filtering, with correction of timing errors independent of estimation of timing errors. They are also intended to afford flexibility for dynamic reconfiguration and upgrading. The architecture is implemented in a reconfigurable CMOS processor in the form of a field-programmable gate array. The algorithm and its hardware implementation incorporate three separate time-varying filter banks for three distinct functions: correction of sub-sample timing errors, post-detection filtering, and post-detection estimation of timing errors. The design of the filter bank for correction of timing errors, the method of estimating timing errors, and the design of a feedback-loop filter are governed by a host of parameters, the most critical one, with regard to processing very broadband signals with CMOS hardware, being the number of parallel streams (equivalently, the rate-reduction parameter).

*This work was done by Andrew Gray, Edward Kang, Norman Lay, Victor Vilnrotter, Meera Srinivasan, and Clement Lee of Caltech for NASA's Jet Propulsion Laboratory.*

*In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:*

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*Refer to NPO-40711, volume and number of this* NASA Tech Briefs *issue, and the page number.*

# Inexpensive Implementation of Many Strain Gauges

## Arrays of metal film resistors would sense strains at multiple locations.

*NASA's Jet Propulsion Laboratory, Pasadena, California*

It has been proposed to develop arrays of strain gauges as arrays of ordinary metal film resistors and associated electronic readout circuitry on printed-circuit boards or other suitable substrates. This proposal is a by-product of a development of instrumentation utilizing metal film resistors on printed-circuit boards to measure temperatures at multiple locations. In the course of that development, it was observed that in addition to being sensitive to temperature, the metal film resistors were also sensitive to strains in the printed-circuit boards to which they were attached. Because of the low cost of ordinary metal film resistors (typically <$0.01 apiece at 2007 prices), the proposal could enable inexpensive implementation of arrays of many (e.g., 100 or more) strain gauges, possibly concentrated in small areas. For example, such an array could be designed for use as a computer keyboard with no moving parts, as a device for sensing the shape of an object resting on a surface, or as a device for measuring strains at many points on a mirror, a fuel tank, an airplane wing, or other large object.

Ordinarily, the effect of strain on resistance would be regarded as a nuisance in a temperature-measuring application, and the effect of temperature on resistance would be regarded as a nuisance in a strain-measuring application. The strain-induced changes in resistance of the metal film resistors in question are less than those of films in traditional strain gauges. The main novel aspect of present proposal lies in the use of circuitry affording sufficient sensitivity to measure strain plus means for compensating for the effect of temperature.

For an array of metal film resistors used as proposed, the readout circuits would include a high-accuracy analog-to-digital converter fed by a low noise current source, amplifier chain, and an analog multiplexer chain. Corrections would be provided by use of

high-accuracy calibration resistors and a temperature sensor. By use of such readout circuitry, it would be possible to read the resistances of as many as 100 fixed resistors in a time interval of 1 second at a resolution much greater than 16 bits. The readout data would be processed, along with temperature calibration data, to deduce the strain on the printed-circuit board or other substrate in the areas around the resistors. It should also be possible to also deduce the temperature from the readings.

*This work was done by Andrew C. Berkun of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45711*