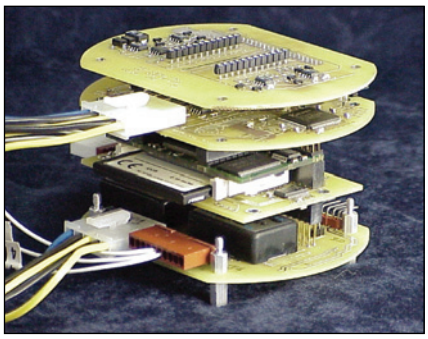
content, in that it can contain multiple fluorescence signatures. By use of deconvolution and/or other mixture-analyses techniques, it is often possible to isolate the spectral signature of compounds of interest, even when their fluorescence spectra overlap.

What distinguishes the present 2D EEMF over prior laboratory-type 2D EEMFs are several improvements in packaging (including a sealed housing) and other aspects of design that render it suitable for use in natural underwater settings. In addition, the design of the present 2D EEMF incorporates improvements over the one prior commercial underwater 2D EEMF, developed in 1994 by the same company that developed the present one. Notable advanced features of the present EEMF include the following:

- High sensitivity and spectral resolution are achieved by use of an off-the-shelf grating spectrometer equipped with a sensor in the form of a commercial astronomical-grade 256×532-pixel charge-coupled-device (CCD) array.



This **Assembly of Electronic-Circuit Boards** takes up significantly less room than would a conventional assembly containing circuits that perform the same variety of functions. The CCD, shown here, is mounted onto pins on the top board.

- All of the power supply, timing, control, and readout circuits for the illumination source and the CCD, ancillary environmental monitoring sensors, and circuitry for controlling a shutter or filter motor are custom-designed and mounted compactly on three circuit boards below a fourth circuit board that holds the CCD (see figure).
- The compactness of the grating spectrometer, CCD, and circuit assembly makes it possible to fit the entire instrument into a compact package that is intended to be maneuverable underwater by one person.
- In mass production, the cost of the complete instrument would be relatively low — estimated at approximately $30,000 at 2005 prices.

This work was done by Casey Moore, John da Cunha, Bruce Rhoades, and Michael Twardowski of Western Environmental Technology Laboratories, Inc. for Stennis Space Center.

Inquiries concerning rights for its commercial use should be addressed to:

Western Environmental Technology Laboratories
P.O. Box 518
620 Applegate St.
Philomath, OR 97370
(541) 929-5650

Refer to SSC-00235, volume and number of this NASA Tech Briefs *issue, and the page number.*

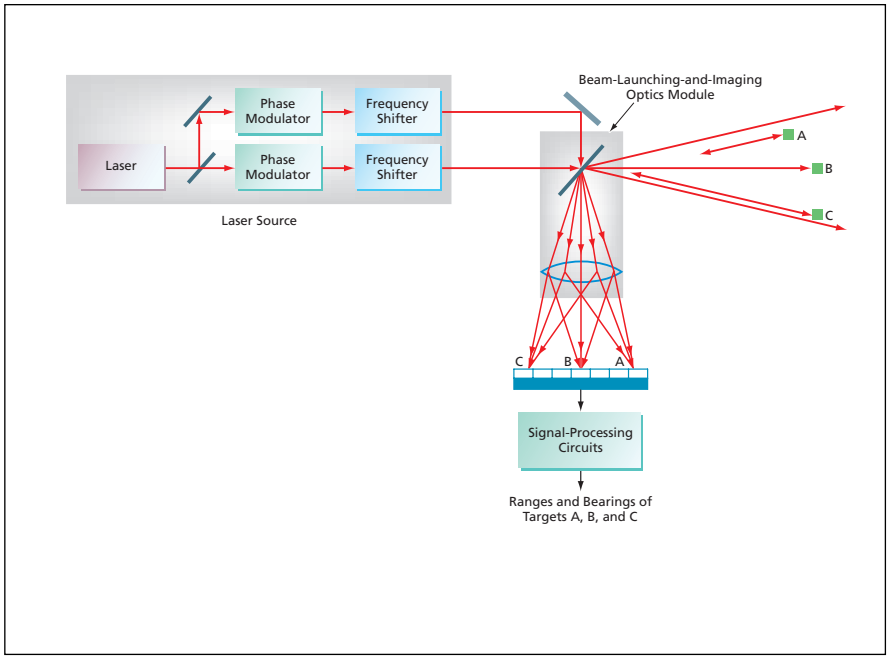
Metrology Camera System Using Two-Color Interferometry

3D locations of multiple targets are determined without mechanical scanning.

NASA's Jet Propulsion Laboratory, Pasadena, California

A metrology system that contains no moving parts simultaneously measures the bearings and ranges of multiple reflective targets in its vicinity, enabling determination of the three-dimensional (3D) positions of the targets with submillimeter accuracy. The system combines a direction-measuring metrology camera and an interferometric range-finding subsystem. Because the system is based partly on a prior instrument denoted the Modulation Sideband Technology for Absolute Ranging (MSTAR) sensor and because of its 3D capability, the system is denoted the MSTAR3D. Developed for use in measuring the shape (for the purpose of compensating for distortion) of large structures like radar antennas, it can also be used to measure positions of multiple targets in the course of conventional terrestrial surveying.

A diagram of the system is shown in the figure. One of the targets is a reference target having a known, constant distance with respect to the system. The system comprises a laser for generating local and target beams at a carrier frequency; a frequency shifting unit to introduce a frequency shift offset between the target and local beams; a pair of high-speed modulators that apply modulation to the carrier frequency in the local and target beams to produce a series of modulation sidebands, the high-speed modulators having modulation



The **MSTAR3D** measures the bearings of targets in the manner of a star tracker and the ranges of targets by use of heterodyne interferometry.

frequencies of F_L and F_M; a target beam launcher that illuminates the targets with the target beam; optics and a multi-pixel photodetector; a local beam launcher that launches the local beam towards the multi-pixel photodetector; a mirror for projecting to the optics a portion of the target beam reflected from the targets, the optics being configured to focus the portion of the target beam at the multi-pixel photodetector; and a signal-processing unit connected to the photodetector.

The portion of the target beam reflected from the targets produces spots on the multi-pixel photodetector corresponding to the targets, respectively, and the signal-processing unit centroids the spots to determine bearings of the targets, respectively. As the spots oscillate in intensity because they are mixed with the local laser beam that is flood illuminating the focal plane, the phase of oscillation of each spot is measured, the phase of sidebands in the oscillation of each spot being proportional to a distance to the corresponding target relative to the reference target A.

This work was done by Serge Dubovitsky, Carl Christian Liebe, Robert Peters, and Oliver Lay of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-42187

Design and Fabrication of High-Efficiency CMOS/CCD Imagers

Economical production of back-illuminated CMOS/CCD imagers should soon become possible.

NASA's Jet Propulsion Laboratory, Pasadena, California

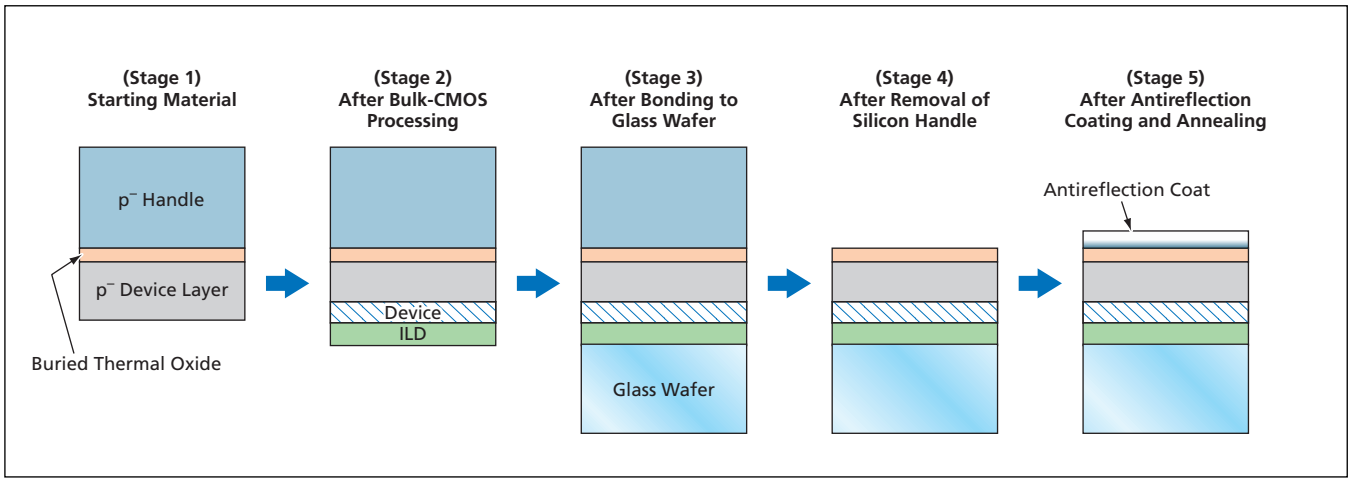
An architecture for back-illuminated complementary metal oxide/semiconductor (CMOS) and charge-coupled-device (CCD) ultraviolet/visible/near infrared-light image sensors, and a method of fabrication to implement the architecture, are undergoing development. The architecture and method are expected to enable realization of the full potential of back-illuminated CMOS/CCD imagers to perform with high efficiency, high sensitivity, excellent angular response, and in-pixel signal processing. The architecture and method are compatible with next-generation CMOS dielectric-forming and metallization techniques, and the process flow of the method is compatible with process flows typical of the manufacture of very-large-scale integrated (VLSI) circuits.

The architecture and method overcome all obstacles that have hitherto prevented high-yield, low-cost fabrication of back-illuminated CMOS/CCD imagers by use of standard VLSI fabrication tools and techniques. It is not possible to discuss the obstacles in detail within the space available for this article. Briefly, the obstacles are posed by the problems of generating light-absorbing layers having desired uniform and accurate thicknesses, passivation of surfaces, forming structures for efficient collection of charge carriers, and wafer-scale thinning (in contradistinction to die-scale thinning).

A basic element of the present architecture and method — the element that, more than any other, makes it possible to overcome the obstacles — is the use of an alternative starting material: Instead of starting with a conventional bulk-CMOS wafer that consists of a p-doped epitaxial silicon layer grown on a heavily-p-doped silicon substrate, one starts with a special silicon-on-insulator (SOI) wafer that consists of a thermal oxide buried between a lightly p- or n-doped, thick silicon layer and a device silicon layer of appropriate thickness and doping. The thick silicon layer is used as a handle: that is, as a mechanical support for the device silicon layer during micro-fabrication.

Although one starts with an SOI wafer, one uses a conventional bulk-CMOS process to fabricate the CMOS imager. The process includes implantation, oxidation, deposition of inter-layer dielectrics [ILDs (dielectric layers interspersed among metal and semiconductor structures)], and deposition and patterning of metals. Any bulk-CMOS process can be used, but it is more appropriate to use a bulk-CMOS process that has been optimized for fabrication of imagers. The bulk-CMOS process yields the structure depicted at stage 2 in the figure.

In order to prepare for back-side illumination, the CMOS structure is bonded to a glass wafer for mechanical support, as shown at stage 3. The silicon handle is then removed through a combination of wet and/or reactive-ion etching, yielding the structure shown at stage 4. The buried SiO_2 layer serves as a built-in etch stop, making it possible to form a uniformly planar back surface. In addition, the resultant



Partly Schematic Cross Sections of a wafer are shown at selected stages of processing for manufacturing CMOS imagers.