frequencies of F_L and F_M; a target beam launcher that illuminates the targets with the target beam; optics and a multi-pixel photodetector; a local beam launcher that launches the local beam towards the multi-pixel photodetector; a mirror for projecting to the optics a portion of the target beam reflected from the targets, the optics being configured to focus the portion of the target beam at the multi-pixel photodetector; and a signal-processing unit connected to the photodetector.

The portion of the target beam reflected from the targets produces spots on the multi-pixel photodetector corresponding to the targets, respectively, and the signal-processing unit centroids the spots to determine bearings of the targets, respectively. As the spots oscillate in intensity because they are mixed with the local laser beam that is flood illuminating the focal plane, the phase of oscillation of each spot is measured, the phase of sidebands in the oscillation of each spot being proportional to a distance to the corresponding target relative to the reference target A.

This work was done by Serge Dubovitsky, Carl Christian Liebe, Robert Peters, and Oliver Lay of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-42187

Design and Fabrication of High-Efficiency CMOS/CCD Imagers

Economical production of back-illuminated CMOS/CCD imagers should soon become possible.

NASA's Jet Propulsion Laboratory, Pasadena, California

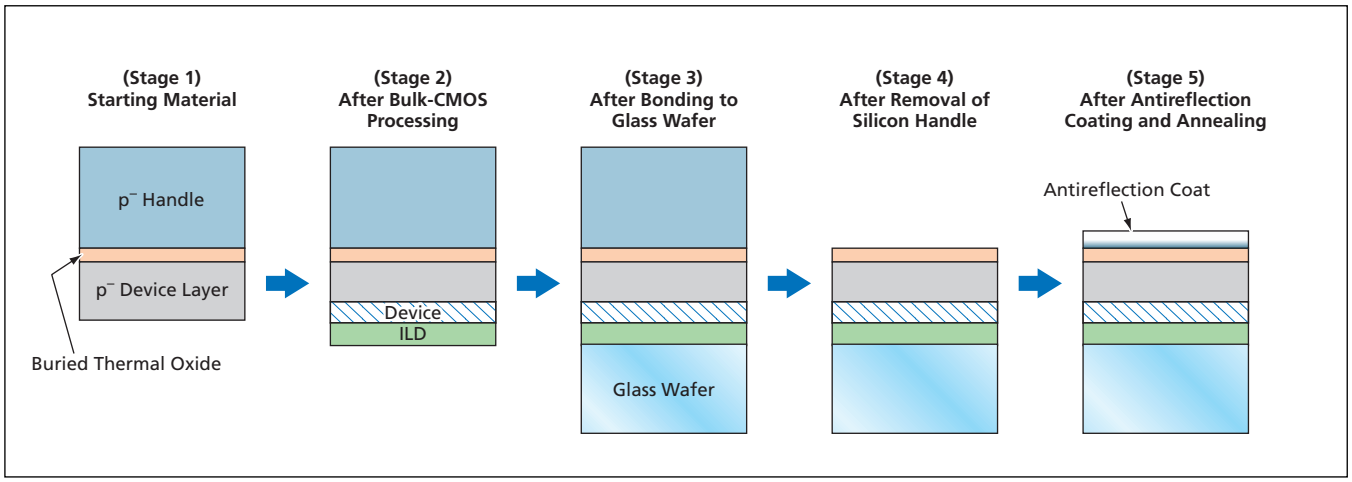
An architecture for back-illuminated complementary metal oxide/semiconductor (CMOS) and charge-coupled-device (CCD) ultraviolet/visible/near infrared-light image sensors, and a method of fabrication to implement the architecture, are undergoing development. The architecture and method are expected to enable realization of the full potential of back-illuminated CMOS/CCD imagers to perform with high efficiency, high sensitivity, excellent angular response, and in-pixel signal processing. The architecture and method are compatible with next-generation CMOS dielectric-forming and metallization techniques, and the process flow of the method is compatible with process flows typical of the manufacture of very-large-scale integrated (VLSI) circuits.

The architecture and method overcome all obstacles that have hitherto prevented high-yield, low-cost fabrication of back-illuminated CMOS/CCD imagers by use of standard VLSI fabrication tools and techniques. It is not possible to discuss the obstacles in detail within the space available for this article. Briefly, the obstacles are posed by the problems of generating light-absorbing layers having desired uniform and accurate thicknesses, passivation of surfaces, forming structures for efficient collection of charge carriers, and wafer-scale thinning (in contradistinction to die-scale thinning).

A basic element of the present architecture and method — the element that, more than any other, makes it possible to overcome the obstacles — is the use of an alternative starting material: Instead of starting with a conventional bulk-CMOS wafer that consists of a p-doped epitaxial silicon layer grown on a heavily-p-doped silicon substrate, one starts with a special silicon-on-insulator (SOI) wafer that consists of a thermal oxide buried between a lightly p- or n-doped, thick silicon layer and a device silicon layer of appropriate thickness and doping. The thick silicon layer is used as a handle: that is, as a mechanical support for the device silicon layer during micro-fabrication.

Although one starts with an SOI wafer, one uses a conventional bulk-CMOS process to fabricate the CMOS imager. The process includes implantation, oxidation, deposition of inter-layer dielectrics [ILDs (dielectric layers interspersed among metal and semiconductor structures)], and deposition and patterning of metals. Any bulk-CMOS process can be used, but it is more appropriate to use a bulk-CMOS process that has been optimized for fabrication of imagers. The bulk-CMOS process yields the structure depicted at stage 2 in the figure.

In order to prepare for back-side illumination, the CMOS structure is bonded to a glass wafer for mechanical support, as shown at stage 3. The silicon handle is then removed through a combination of wet and/or reactive-ion etching, yielding the structure shown at stage 4. The buried SiO_2 layer serves as a built-in etch stop, making it possible to form a uniformly planar back surface. In addition, the resultant



Partly Schematic Cross Sections of a wafer are shown at selected stages of processing for manufacturing CMOS imagers.

structure is self-passivated, since the device silicon layer is not exposed during etching and is protected by a high quality thermally grown oxide layer. Termination of silicon by the high quality buried oxide provides a Si-SiO_2 interface with very low interface state-density. Therefore, no additional processing is necessary, a processing step that would not only be difficult but would also be incompatible with standard VLSI processing. Inasmuch as there exists a high-selectivity etch-stop and the post-etching passivation is automatic, the process represented by the figure is fully CMOS-compatible and can be carried out at the wafer level.

Furthermore, because the device silicon is separated from the handle through the buried oxide, no unintentional doping of the device silicon occurs during CMOS fabrication. Thus, it becomes possible to start with an SOI wafer with an appropriate doping of the device silicon layer to optimize imaging performance (e.g. high quantum efficiency, high modulation transfer function, low cross-talk, and low dark current).

The final step in the process is anti-reflection coating to increase optical coupling. Since the resultant structure is fully planar and includes only a single SiO_2 layer, one has freedom to deposit anti-reflection layer in ways that would not be possible if light were required to travel through multilayer, nonuniform ILD as in the front-illumination case.

This work was done by Bedabrata Pain of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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