

characterization of multichip modules using existing InP. Following processing, a test campaign was carried out using single-chip modules at 100 GHz. Successful development of the chips will lead to development of multichip modules, with simultaneous Q and U Stokes parameter detection.

This MMIC (monolithic microwave integrated circuit) amplifier takes advantage of performance improvements intended for higher frequencies, but in this innovation are applied at 90 GHz. The large amount of available gain ultimately leads to lower possible noise performance at 90 GHz.

This work was done by Lorene A. Samoska, Todd C. Gaier, Stephanie Xenos, Mary M. Soria, Pekka P. Kangaslahti, and Kieran A. Cleary of Caltech; and Linda Ferreira, Richard Lai and Xiaobing Mei of Northrop Grumman Corporation for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-46627

A 311-GHz Fundamental Oscillator Using InP HBT Technology

This is the first fundamental HBT oscillator operating above 300 GHz.

NASA's Jet Propulsion Laboratory, Pasadena, California

This oscillator uses a single-emitter 0.3- μm InP heterojunction bipolar transistor (HBT) device with maximum frequency of oscillation (f_{max}) greater than 500 GHz. Due to high conductor and substrate losses at submillimeter-wave frequencies, a primary challenge is to efficiently use the intrinsic device gain. This was done by using a suitable transmission-line media and circuit topology. The passive components of the oscillator are realized in a two-metal process with benzocyclobutene (BCB) used as the primary transmission line dielectric. The circuit was designed using microstrip transmission lines.

The oscillator is implemented in a common-base topology due to its inherent instability, and the design includes an on-chip resonator, output-matching circuitry, and an injection-locking port, the port being used to demonstrate the injection-locking principle. A free-running frequency of 311.6 GHz has been measured by down-converting the signal. Additionally, injection locking has

been successfully demonstrated with up to 17.8 dB of injection-locking gain. The injection-locking reference signal is generated using a 2–20 GHz frequency synthesizer, followed by a doubler, active tripler, a W-band amplifier, and then a passive tripler. Therefore, the source frequency is multiplied 18 times to obtain a signal above 300 GHz that can be used to injection lock the oscillator. Measurement shows that injection locking has improved the phase noise of the oscillator and can be also used for synchronizing a series of oscillators.

A signal conductor is implemented near the BCP-InP interface and the top side of the BCB layer is fully metallized as a signal ground. Because the fields are primarily constrained in the lower permittivity BCB region, this type of transmission line is referred to as an inverted microstrip. In addition, both common-emitter and common-base circuits were investigated to determine optimum topology for oscillator design. The common-base topology required smaller amount of

feedback than the common-emitter design, therefore preserving device gain, and was chosen for the oscillator design.

The submillimeter-wave region offers several advantages for sensors and communication systems, such as high resolution and all-weather imaging due to the short-wavelength, and improved communication speeds by access to greater frequency bandwidth. This oscillator circuit is a prototype of the first HBT oscillator operating above 300 GHz. Additional development is necessary to increase the output power of the circuit for radar and imaging applications.

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FPGA Coprocessor Design for an Onboard Multi-angle Spectro-Polarimetric Imager

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A multi-angle spectro-polarimetric imager (MSPI) is an advanced camera system currently under development at JPL for possible future consideration on a satellite-based Aerosol-Cloud-Environment (ACE) interaction study. The light in the optical system is subjected to a complex modulation designed to make the overall system robust against many instrumental artifacts that have plagued

such measurements in the past. This scheme involves two photoelastic modulators that are beating in a carefully selected pattern against each other. In order to properly sample this modulation pattern, each of the proposed nine cameras in the system needs to read out its imager array about 1,000 times per second. The onboard processing required to compress this data involves

least-squares fits (LSFs) of Bessel functions to data from every pixel in real-time, thus requiring an onboard computing system with advanced data processing capabilities in excess of those commonly available for space flight.

As a potential solution to meet the MSPI onboard processing requirements, an LSF algorithm was developed on the Xilinx Virtex-4FX60 field programmable

gate array (FPGA). In addition to configurable hardware capability, this FPGA includes Power-PC405 microprocessors, which together enable a combination hardware/software processing system.

A laboratory demonstration was carried out based on a hardware/software co-designed processing architec-

ture that includes hardware-based data collection and least-squares fitting (computationally), and software-based transcendental function computation (algorithmically complex) on the FPGA. Initial results showed that these calculations can be handled using a combination of the Virtex-

4TM Power-PC core and the hardware fabric.

This work was done by Paula J. Pingree and Thomas A. Werne of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-46614