use of SUMPLE. At the beginning of the simulated reception process, the signal phases were taken to be random, resulting in a very large combining loss. The combining loss was found to decrease to a few tenths of a decibel in about eight iterations and to remain at this level thereafter (see Figure 2). Simulations of many different array configurations yielded essentially the same results.

Answering the question of phase wandering, the simulations did, indeed, show slow phase variations of a few degrees over time intervals of 10 to 20 iterations. However, it was found that this wandering could be prevented by forcing, to zero, the total phase correction obtained by summing the individual corrections over all the antennas. Inasmuch as the phase corrections are meant to bring the antenna signals into alignment with each other, forcing the total phase correction to zero does not pose an obstacle to the achievement of array coherence.

SUMPLE has been tested on an array of 34-m-diameter antennas in the DSN. The results of this test have been found to agree with those of the simulations.

This work was done by David Rogstad of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*

The software used in this innovation is available for commercial licensing. Please contact Karina Edmonds of the California Institute of Technology at (818) 393-2827. Refer to NPO-40574.
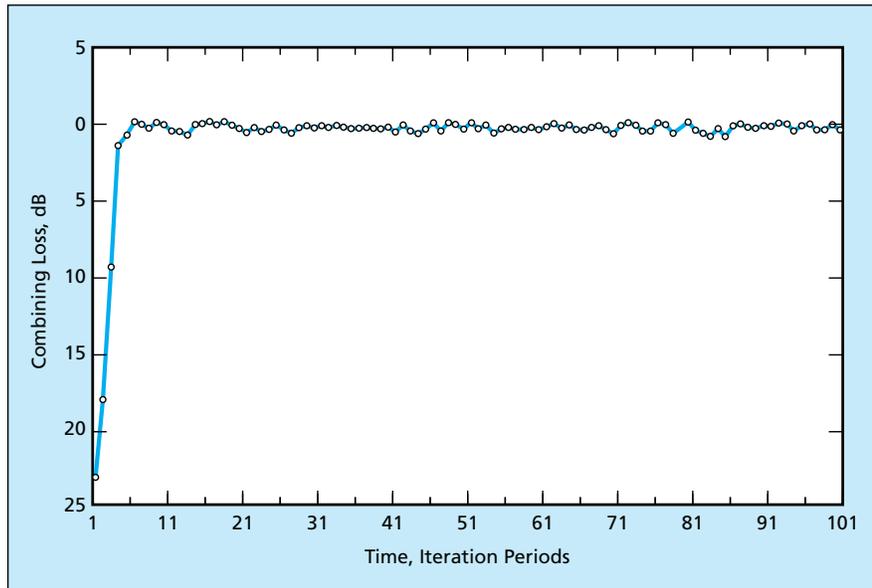

Figure 2. The **Combining Loss** of a 100-antenna array using SUMPLE was simulated for reception of a representative telemetry signal. The unit of time on the abscissa is an iteration period defined, for the purpose of this specific example, as an integration time of 5,000 telemetry-symbol periods.

Single-Chip T/R Module for 1.2 GHz

T/R modules can be made smaller and at lower cost.

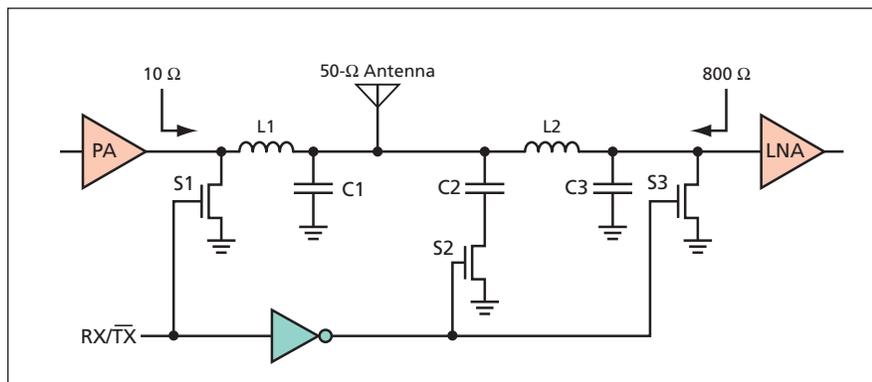*NASA's Jet Propulsion Laboratory, Pasadena, California*

A single-chip CMOS-based (complementary-metal-oxide-semiconductor-based) transmit/receive (T/R) module is being developed for L-band radar systems. Previous T/R module implementations required multiple chips employing different technologies (GaAs, Si, and others) combined with off-chip transmission lines and discrete components including circulators. The new design eliminates the bulky circulator, significantly reducing the size and mass of the T/R module.

Compared to multi-chip designs, the single-chip CMOS can be implemented with lower cost. These innovations enable cost-effective realization of advanced phased array and synthetic aperture radar systems that require integration of thousands of T/R modules.

The circulator is a ferromagnetic device that directs the flow of the RF (radio frequency) power during transmission and reception. During transmission, the circulator delivers the transmitted power from the amplifier to the antenna, while preventing it from damaging the sensitive receiver circuitry. During reception, the circulator directs the energy from the antenna to the low-noise amplifier (LNA) while isolating the output of the power amplifier (PA). In principle, a circulator could be replaced by series transistors acting as electronic switches. However, in practice, the integration of conventional series transistors into a T/R chip introduces significant losses and noise.

The prototype single-chip T/R module contains integrated transistor switches, but not connected in series; instead, they are connected in a shunt configuration with resonant circuits (see figure). The shunt/resonant circuit topology not only reduces the losses associated with conventional semiconductor switches but also provides beneficial transformation of impedances for the PA and the LNA. It provides full single-pole/double-throw switching for the antenna, isolating the LNA from the transmitted signal and isolating the PA from the received signal. During reception,

A **1.2-GHz Single-Chip T/R Circuit** for a radar system eliminates a bulky circulator.

the voltage on control line RX/$\overline{TX}$ is high, causing the field-effect transistor (FET) switch S1 to be closed, forming a parallel resonant tank circuit L1‖C1. This circuit presents high impedance to the left of the antenna, so that the received signal is coupled to the LNA. At the same time, FET switches S2 and S3 are open, so that C2 is removed from the circuit (except for a small parasitic capacitance). The combination of L2 and C3 forms a matching network that transforms the antenna impedance of 50 ohms to a higher value from the perspective of the LNA input terminal. This transformation of impedance improves LNA noise figure by increasing the received voltage delivered to the input transistor. This allows lower transconductance and therefore a smaller transistor, which makes it possible to design the CMOS LNA for low power consumption. During transmission, the voltage on control line RX/$\overline{TX}$ is low, causing switch S1 to be open. In this configuration, the combination of L1 and C1 transforms the antenna impedance to a lower value from the perspective of the PA. This low impedance is helpful in producing a relatively high output power compatible with the low CMOS operating potential. At the same time, switches S2 and S3 are closed, forming the parallel resonant tank circuit L2‖C2. This circuit presents high impedance to the right of the antenna, directing the PA output signal to the antenna and away from the LNA. During this time, S3 presents a short circuit across the LNA input terminals to guarantee that the voltage seen by the LNA is small enough to prevent damage.