



• Demonstration of a Submillimeter-Wave HEMT Oscillator Module at 330 GHz

This low-mass, low-power module may be useful for hidden weapons detection and airport security.

NASA's Jet Propulsion Laboratory, Pasadena, California

In this work, radial transitions have been successfully mated with a HEMT-based MMIC (high-electron-mobility-transistor-based monolithic microwave integrated circuit) oscillator circuit. The chip has been assembled into a WR2.2 waveguide module for the basic implementation with radial E-plane probe transitions to convert the waveguide mode to the MMIC coplanar waveguide mode. The E-plane transitions have been directly integrated onto the InP substrate to couple the submillimeter-wave energy directly to the waveguides, thus avoiding wirebonds in the RF path. The oscillator demonstrates a measured 1.7 percent DC-RF efficiency at the module level.

The oscillator chip uses 35-nm-gate-length HEMT devices, which enable the high frequency of oscillation, creating the first demonstration of a packaged

waveguide oscillator that operates over 300 GHz and is based on InP HEMT technology. The oscillator chip is extremely compact, with dimensions of only $1,085 \times 320 \mu\text{m}^2$ for a total die size of 0.35 mm^2 . This fully integrated, waveguide oscillator module, with an output power of 0.27 mW at 330 GHz, can provide low-mass, low DC-power-consumption alternatives to existing local oscillator schemes, which require high DC power consumption and large mass.

This oscillator module can be easily integrated with mixers, multipliers, and amplifiers for building high-frequency transmit and receive systems at submillimeter wave frequencies. Because it requires only a DC bias to enable submillimeter wave output power, it is a simple and reliable technique for generating power at these frequencies. Future work will be directed to further improving the

applicability of HEMT transistors to submillimeter wave and terahertz applications. Commercial applications include submillimeter-wave imaging systems for hidden weapons detection, airport security, homeland security, and portable low-mass, low-power imaging systems.

This work was done by Vesna Radisic, W. R. Deal, X.B. Mei, Wayne Yoshida, P.H. Liu, Jansen Uyeda, and Richard Lai of Northrop Grumman Corporation (NGC); and Lorene Samoska, King Man Fung, Todd Gaier, and David Pukala of Caltech for NASA's Jet Propulsion Laboratory. The contributors would like to acknowledge the support of Dr. Mark Rosker and the Army Research Laboratory. This work was supported by the DARPA SWIFT Program and Army Research Laboratory under the DARPA MIPR no.06-U037 and ARL Contract no. W911QX-06-C-0050. Further information is contained in a TSP (see page 1). NPO-45736

• Flexible Peripheral Component Interconnect Input/Output Card

The card has applications in quality and testing systems for product design verification and manufacturing testing.

Lyndon B. Johnson Space Center, Houston, Texas

The Flexible Peripheral Component Interconnect (PCI) Input/Output (I/O) Card is an innovative circuit board that provides functionality to interface between a variety of devices. It supports user-defined interrupts for interface synchronization, tracks system faults and failures, and includes checksum and parity evaluation of interface data. The card supports up to 16 channels of high-speed, half-duplex, low-voltage digital signaling (LVDS) serial data, and can interface combinations of serial and parallel devices. Placement of a processor within the field programmable gate array (FPGA) controls an embedded application with links to host

memory over its PCI bus. The FPGA also provides protocol stacking and quick digital signal processor (DSP) functions to improve host performance. Hardware timers, counters, state machines, and other glue logic support interface communications.

The Flexible PCI I/O Card provides an interface for a variety of dissimilar computer systems, featuring direct memory access functionality. The card has the following attributes:

- 8/16/32-bit, 33-MHz PCI r2.2 compliance,
- Configurable for universal 3.3V/5V interface slots,
- PCI interface based on PLX Technol-

- ogy's PCI9056 ASIC,
- General-use 512K×16 SDRAM memory,
- General-use 1M×16 Flash memory,
- FPGA with 3K to 56K logical cells with embedded 27K to 198K bits RAM,
- I/O interface: 32-channel LVDS differential transceivers configured in eight, 4-bit banks; signaling rates to 200 MHz per channel,
- Common SCSI-3, 68-pin interface connector.

The Flexible PCI I/O Card was integrated into the Shuttle Mission Simulator (SMS) as a more efficient means of interfacing between the Silicon Graphic Inc. (SGI) simulation host and the Simulator Interface Device (SID). The

FPGA was developed to memory map the SID I/O data stream. The card eliminated the previous protocol that required generation of command word and word count I/O data blocks, and added functionality much like direct memory access.

The card was integrated into the Shuttle Avionics Integration Laboratory (SAIL) as an improved interface to the Linux-based Hosting Interface Device

(HID). This card allowed replacement of a serial port to parallel data handling, thereby decreasing general-purpose computer (GPC) load times by about 10 minutes.

Finally, the Flexible PCI card was integrated in the SMS, and ready for implementation in the SAIL and to the KSC Avionics Test Set (KATS) Lab, to interface a Windows XP host to a dual channel MIA (media interface adapter) data

bus device, providing a means of simulating solid-state mass memory units to load Shuttle general purpose computers (GPCs).

This hardware and firmware work was done by Kirk K. Bigelow and software work was done by Albert L. Jerry, Alisha G. Barcio, and Jon K. Cummings of United Space Alliance for Johnson Space Center. Further information is contained in a TSP (see page 1). MSC-24615-1

Interface Supports Lightweight Subsystem Routing for Flight Applications

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A wireless avionics interface exploits the constrained nature of data networks in flight systems to use a lightweight routing method. This simplified routing means that a processor is not required, and the logic can be implemented as an intellectual property (IP) core in a field-programmable gate array (FPGA). The FPGA can be shared with the flight subsystem application. In addition, the router is aware of redundant subsystems, and can be configured to provide hot standby support as part of the interface. This simplifies implementation of flight applications requiring hot standby support.

When a valid inbound packet is received from the network, the destination node address is inspected to determine whether the packet is to be processed by this node. Each node has routing tables for the next neighbor node to guide the packet to the destination node. If it is to be processed, the final packet destination is inspected to determine whether the packet is to be forwarded to another node, or routed locally. If the packet is local, it is sent to an Applications Data Interface (ADI), which is attached to a local flight application. Under this scheme, an interface can support many applications in a subsystem supporting a high level of

subsystem integration. If the packet is to be forwarded to another node, it is sent to the outbound packet router. The outbound packet router receives packets from an ADI or a packet to be forwarded. It then uses a lookup table to determine the next destination for the packet. Upon detecting a remote subsystem failure, the routing table can be updated to autonomously bypass the failed subsystem.

This work was done by James P. Lux, Gary L. Block, Mohammad Ahmad, William D. Whitaker, and James W. Dillon of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-46322

MMIC Amplifiers and Wafer Probes for 350 to 500 GHz

Amplifiers like these are needed for submillimeter-wavelength imagers and scientific instruments.

NASA's Jet Propulsion Laboratory, Pasadena, California

Several different experimental monolithic microwave integrated circuit (MMIC) amplifiers have been designed to operate in frequency bands ranging from 350 to 500 GHz and were undergoing fabrication at the time of reporting the information for this article. Probes for on-wafer measurement of electrical parameters [principally, the standard scattering parameters ("S" parameters)] of these amplifiers have been built and tested as essential components of systems to be used in quantifying the performances of the amplifiers. These accomplishments are intermediate products of a continuing effort to develop solid-state electronic amplifiers capable of producing gain at ever-higher

frequencies, now envisioned to range up to 800 GHz. Such amplifiers are needed for further development of compact, portable imaging systems and scientific instruments for a variety of potential applications that include detection of hidden weapons, measuring winds, and measuring atmospheric concentrations of certain molecular species.

Seven of the experimental MMIC amplifiers are single-stage amplifiers; two are three-stage amplifiers. Conceptually, each amplifier is built around an InP-based high-electron-mobility transistor (HEMT) having a gate length of 35 nm, which has been developed at Northrop Grumman Corporation. It was previously demonstrated that the particular

HEMT can be fabricated with a high degree of reproducibility, that its electrical characteristics are accurately represented by a device model needed to design an MMIC that incorporates it, and that an experimental single-stage MMIC built around it exhibits 5 dB of gain at 345 GHz.

The seven present single-stage amplifier designs were derived from that of the 345-GHz MMIC amplifier. They were designed by use of the aforementioned device model, with modified layouts chosen to satisfy requirements for both (1) compatibility with the HEMT manufacturer's fabrication rules and (2) matching impedances at the affected frequency bands in the 350-to-500 GHz range. The