FPGA was developed to memory map the SID I/O data stream. The card eliminated the previous protocol that required generation of command word and word count I/O data blocks, and added functionality much like direct memory access.

The card was integrated into the Shuttle Avionics Integration Laboratory (SAIL) as an improved interface to the Linux-based Hosting Interface Device (HID). This card allowed replacement of a serial port to parallel data handling, thereby decreasing general-purpose computer (GPC) load times by about 10 minutes.

Finally, the Flexible PCI card was integrated in the SMS, and ready for implementation in the SAIL and to the KSC Avionics Test Set (KATS) Lab, to interface a Windows XP host to a dual channel MIA (media interface adapter) data bus device, providing a means of simulating solid-state mass memory units to load Shuttle general purpose computers (GPCs).

This hardware and firmware work was done by Kirk K. Bigelow and software work was done by Albert L. Jerry, Alisha G. Barcio, and Jon K. Cummings of United Space Alliance for Johnson Space Center. Further information is contained in a TSP (see page 1).
MSC-24615-1

Interface Supports Lightweight Subsystem Routing for Flight Applications

NASA's Jet Propulsion Laboratory, Pasadena, California

A wireless avionics interface exploits the constrained nature of data networks in flight systems to use a lightweight routing method. This simplified routing means that a processor is not required, and the logic can be implemented as an intellectual property (IP) core in a field-programmable gate array (FPGA). The FPGA can be shared with the flight subsystem application. In addition, the router is aware of redundant subsystems, and can be configured to provide hot standby support as part of the interface. This simplifies implementation of flight applications requiring hot standby support.

When a valid inbound packet is received from the network, the destination node address is inspected to determine whether the packet is to be processed by this node. Each node has routing tables for the next neighbor node to guide the packet to the destination node. If it is to be processed, the final packet destination is inspected to determine whether the packet is to be forwarded to another node, or routed locally. If the packet is local, it is sent to an Applications Data Interface (ADI), which is attached to a local flight application. Under this scheme, an interface can support many applications in a subsystem supporting a high level of subsystem integration. If the packet is to be forwarded to another node, it is sent to the outbound packet router. The outbound packet router receives packets from an ADI or a packet to be forwarded. It then uses a lookup table to determine the next destination for the packet. Upon detecting a remote subsystem failure, the routing table can be updated to autonomously bypass the failed subsystem.

This work was done by James P. Lux, Gary L. Block, Mohammad Ahmad, William D. Whitaker, and James W. Dillon of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov.
NPO-46322

MMIC Amplifiers and Wafer Probes for 350 to 500 GHz

Amplifiers like these are needed for submillimeter-wavelength imagers and scientific instruments.

NASA's Jet Propulsion Laboratory, Pasadena, California

Several different experimental monolithic microwave integrated circuit (MMIC) amplifiers have been designed to operate in frequency bands ranging from 350 to 500 GHz and were undergoing fabrication at the time of reporting the information for this article. Probes for on-wafer measurement of electrical parameters [principally, the standard scattering parameters ("S" parameters)] of these amplifiers have been built and tested as essential components of systems to be used in quantifying the performances of the amplifiers. These accomplishments are intermediate products of a continuing effort to develop solid-state electronic amplifiers capable of producing gain at ever-higher frequencies, now envisioned to range up to 800 GHz. Such amplifiers are needed for further development of compact, portable imaging systems and scientific instruments for a variety of potential applications that include detection of hidden weapons, measuring winds, and measuring atmospheric concentrations of certain molecular species.

Seven of the experimental MMIC amplifiers are single-stage amplifiers; two are three-stage amplifiers. Conceptually, each amplifier is built around an InP-based high-electron-mobility transistor (HEMT) having a gate length of 35 nm, which has been developed at Northrop Grumman Corporation. It was previously demonstrated that the particular HEMT can be fabricated with a high degree of reproducibility, that its electrical characteristics are accurately represented by a device model needed to design an MMIC that incorporates it, and that an experimental single-stage MMIC built around it exhibits 5 dB of gain at 345 GHz.

The seven present single-stage amplifier designs were derived from that of the 345-GHz MMIC amplifier. They were designed by use of the aforementioned device model, with modified layouts chosen to satisfy requirements for both (1) compatibility with the HEMT manufacturer's fabrication rules and (2) matching impedances at the affected frequency bands in the 350-to-500 GHz range. The

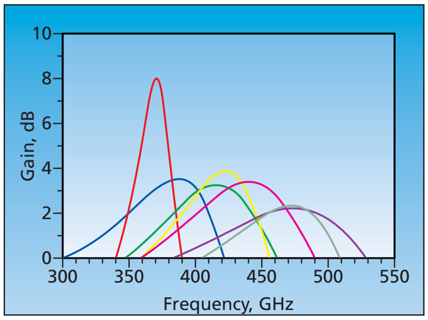

Figure 1. **Gains of Seven Single-Stage MMIC Amplifiers** built around advanced InP HEMTs were predicted in computational simulations.

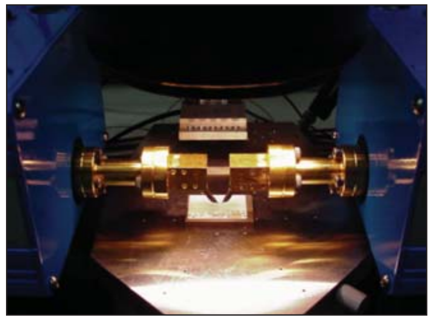

Figure 2. **Wafer Probes** are mounted on the terminals of a network analyzer, with the probe tips in contact with a calibration substrate.

designs utilize several different matching-circuit topologies, some of which resemble topologies heretofore required for multi-stage amplifiers. Figure 1 shows the gains of the single-stage amplifiers as predicted by computational simulations. The two three-stage amplifiers were designed to operate at frequencies from 400 to 500 GHz, with peak gains in the approximate range of 11 to 13 dB.

The wafer probes were designed and built for use with a two-port swept-vector network analyzer that operates in the frequency range of 325 to 500 GHz. This network analyzer has been fully characterized for reproducibility and dynamic range. The probes include WR2.2 waveguides and waveguide-to-coaxial transitions developed at Cascade Microtech and Portland State University (see Figure 2). The insertion loss of the waveguide-to-coaxial transitions has been measured to be about 7 dB at 325 to 500 GHz.

This work was done by Lorene A. Samoska and King Man Fung of Caltech; Michael Andrews of Cascade Microtech, Inc.; Richard Campbell of Portland State University; and Linda Ferreira and Richard Lai of Northrop Grumman Corp. for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). **.** *NPO-45588*