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Title : **IXO/XMS detector Trade-Off Study**

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Abbreviations and acronyms

Item	Meaning
CDM	Code-Division Multiplexing
DRIE	Deep Reactive Ion Etching
FDM	Frequency-Division Multiplexing
FOV	Field of View
GSFC	Goddard Space Flight Center
ISAS	Institute for Space and Astronautical Studies
MUX	MUltipleXer
NIST	National Institute of Standards and Technology
RIE	Reactive Ion Etching
RRR	Residual Resistivity Ratio (a measure of metal film quality)
SQUID	Superconducting Quantum Interference Device
SRON	Netherlands Institute for Space Research
TBC	To Be Confirmed
TDM	Time-Division Multiplexing
TES	Transition-Edge Sensor

Applicable Documents

[AD#]	Doc. Reference	Rev	Title
[AD1]	IXO-TN-001141 (combines XMS_noise_budget_v2.2.doc and XMS_noise_budget_v2.2.xls)	–	Noise Budget for the X-ray Microcalorimeter Spectrometer (XMS) Core Array
[AD2]	SRON-XMS-RP-2010-008	–	Focal-Plane Assembly Trade-off Teport
[AD3]	SRON-XMS-RP-2010-007	–	XMS Multiplexed Read-Out Trade-Off
[AD4]	SRON-XMS-PL-2009-003	Proposal dated 6 June 2009	Assessment study of the X-ray Micro-calorimeter Spectrometer on IXO
[AD5]	IXO_MUX_NIST_GSFC_v1.pdf	–	Combined TDM and detector optimization report

Other Cited Reference Documents

[RD#]	Doc. Reference

[RD1] "Uniform high spectral resolution demonstrated in arrays of TES x-ray microcalorimeters", Kilbourne CA, et al., 2007, Proc. SPIE, 6686, 668606.

[RD2] "Characterization and reduction of noise in Mo/Au transition edge sensors", Lindeman MA, et al., 2004, Nucl. Inst. and Meth. A, 520, 348.

[RD3] "Characterization and reduction of unexplained noise in superconducting transition-edge sensors", Ullom JN, et al., 2004, Appl. Phys. Lett., 84, 4206.

[RD4] "Thermodynamics of nonlinear bolometers near equilibrium", Irwin, KD, 2006, Nucl. Inst. and Meth.

[RD#] Doc. Reference

A 559, 718.

[RD5] "Optimal filtering, record length, and count rate in transition-edge-sensor microcalorimeters", Doriese WB, et al., 2009, AIP Conf. Proc. 1185 (LTD13), 450.

[RD6] "Performance of TES X-ray Microcalorimeters with a Novel Absorber Design", Bandler SR, et al., 2008, J. Low Temp. Phys. 151, 400.

[RD7] "Multiplexed readout of uniform arrays of TES x-ray microcalorimeters suitable for Constellation-X", Kilbourne CA, Doriese WB, et al., 2008, Proc. SPIE, 7011, 701104.

[RD8] "Impedance measurement and excess-noise behavior of a Ti/Au bilayer TES calorimeter", Akamatsu H, et al., 2009, AIP Conf. Proc. 1185 (LTD13), 195.

[RD9] "Large Arrays of TES X-ray Microcalorimeters for Dark Baryon Search", Ezoe Y, et al., 2009, AIP Conf. Proc. 1185 (LTD13), 60.

[RD10] Yoshitake Master Thesis (University of Tokyo) 2008

[RD11] "Characterization of a High-Performance Ti/Au TES Microcalorimeter with a Central Cu Absorber", Takei Y, et al., 2008, J. Low Temp. Phys. 151, 161.

[RD12] "Development of arrays of position-sensitive microcalorimeters for Constellation-X", Smith SJ, et al., 2008, Proc. SPIE 7011, 701126.

[RD13] "Development of position-sensitive transition-edge sensor X-ray detectors", Smith SJ, et al., 2009, IEEE Trans. Appl. Superconductivity, 19, 451.

[RD14] "Implementation of complex signal processing algorithms for position-sensitive microcalorimeters", Smith SJ, 2009, Nucl. Instr. and Meth. A 602, 533.

[RD15] "Extended focal-plane array development for the International X-ray Observatory", Smith SJ, 2009, AIP Conf. Proc. 1185 (LTD13), 707.

I. Introduction

This document presents the outcome of the detector trade-off for the XMS instrument on IXO. This trade-off is part of the Cryogenic instrument Phase-A study as proposed to ESA in the Declaration of Interest SRON-XMS-PL-2009-003 dated June 6, 2009.

The detector consists of two components: a core array for the highest spectral resolution and an outer array to increase the field of view substantially with modest increase in the number of read-out channels. Degraded resolution of the outer array in comparison with the core array is accepted in order to make this scheme possible. The two detector components may be a single unit or separate units. These arrays comprise pixels and the components that allow them to be arrayed. Each pixel comprises a thermometer, an absorber, and the thermal links between them and to the rest of the array. These links may be interfaces or distinct components. The array infrastructure comprises the mechanical structure of the array, the arrangement of the leads, and features added to improve the integrated thermal properties of the array in the focal-plane assembly.

II. Reference Technologies and Evaluations

1 Reference configurations

For the detector trade-off studies the options for the core array and for the outer array will be analyzed separately. The following reference configurations will be studied:

Core array:

Option GSFC/NIST-type: Mo/Au TES + electroplated Au/Bi absorber + square grid of Si beams to support the pixel membranes

Option SRON/ISAS-type: Ti/Au TES + evaporated Cu/Bi absorber + linear Si beams (extending the full width of the array) to support the pixel membranes

The distinct features of each option are not required to be used together. The final optimization may mix the most effective elements of the reference options.

Outer array:

Option Hydra: 4 absorbers connected to one TES with 4 different thermal links

Option Large: Large single pixels, larger scale MUX (including option of coupling more than one pixel to an input SQUID)

2 Requirements

2.1 Common requirements

The instrument requirements that affect the design of the detectors are tabulated below. These requirements apply to all options.

Table 2.1 Requirements for the XMS detectors that are independent of implementation

Parameter	Requirement	Comment
Inner Array		
Energy Resolution (E < 6 keV)	2.5 eV FWHM	
FOV	2 arcmin	40x40 with 0.3 mm pixel size
Count rate for 80% high-resolution live time	50/s/pixel	80% high energy resolution events at 50 c/s input rate requires record length + pre-record exclusion window < -ln(0.8)/50 = 4.463 ms.
Outer Array		
Energy Resolution (E < 6 keV)	10 eV FWHM	
FOV	5.4 arcmin	52x52 pixel array implemented on a 0.6 mm pitch (with the space of inner 20x20 pixels occupied by the 40 x 40 inner array on a 0.3 mm pitch).
Count rate for 80% high-resolution live time	2/s/pixel (0.6 mm pixels)	80% high energy resolution events at 2 c/s input rate (= 8 c/s for a coupled 4-pixel unit) requires record length + pre-record exclusion window < -ln(0.8)/8 = 27.89 ms.
Full Array		
Energy Range	0.3 – 12 keV	Goal 0.1 – 12 keV
Quantum efficiency @ 7 keV	>80%	Defines absorber composition and thickness
Relative uncertainty in QE between pixels	<3%	At 7 keV
Energy resolution uniformity	1 eV	FWHM, fit by a gaussian distribution
Detector dead area	<5%	This requires a spacing of < 7.5 μm between pixel absorbers for the inner array, < 15 μm between absorbers of the outer array, and a similar gap between the two arrays
Bad pixels	< 2%	Pixels with E-resolution > 3 * nominal or QE < 0.5 nominal QE

2.2 Derived requirements for the different reference arrays

The design-dependent derived parameters are presented in the Trade-Off Tables Section (Section 5).

3 Description of principle

At the highest level, the configurations under study share a common operating principle, and even some of the details of their designs are shared in common. The XMS detectors will be arrays of microcalorimeters, which are devices that measure the heat pulses from incident X-ray photons via sensitive thermometry. All of the configurations addressed in this trade study use Transition-Edge Sensor (TES) thermometers. The temperature and current dependence of the transition from the zero-resistance to normal-resistance state of

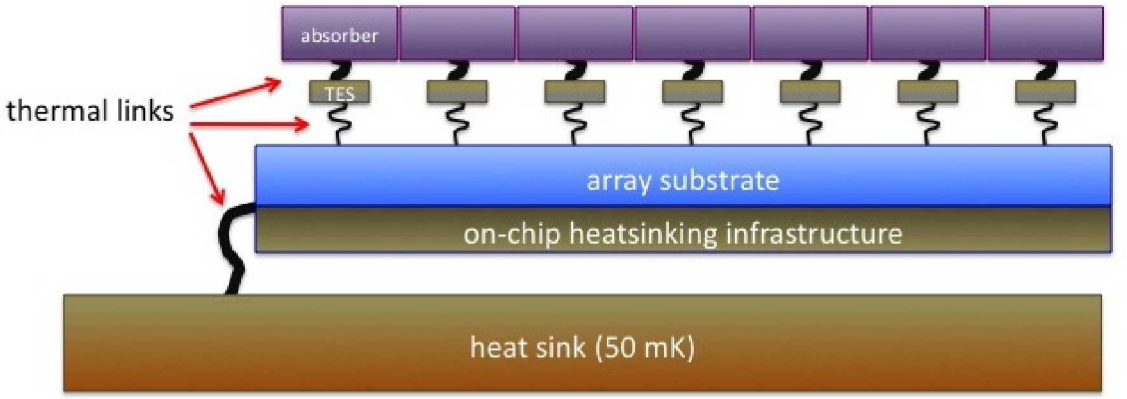

Fig. 3.1 – Block diagram of the core array. The basic components shown are the same for both options being studied for the core array, and they apply at a higher level to the outer array, as well.

a superconductor is used for thermometry. In fact, all the configurations in this study use bilayers made of an elemental superconductor and Au. The thicknesses of the superconducting layer and the Au layer, as well as other details of the device design, are tuned to achieve a transition temperature at the desired operating temperature for an electrically biased device. All of the configurations in this study use silicon-nitride membranes to control the thermal link between the TES and the substrate of the array, which is presumed to be at the temperature of the heat sink. Furthermore, all of the configurations use cantilevered X-ray absorbers based on bismuth (with gold or copper). These absorbers extend beyond the limited area of contact with the TES in order to enable high filling factors.

Fig. 3.1 is a block diagram that illustrates the basic thermal components of the core array for both core-array options. The point of showing the array substrate, on-chip heat-sinking features, and the link to the 50-mK stage is to emphasize that the trade study needs to be conducted at the array scale, and not the pixel scale. The outer array is also made of these basic components at the highest level. However, the outer array requires an additional multiplexing factor, which may be taken either in the MUX itself, at the coupling to a shared input SQUID, or via the thermal coupling of multiple absorbers to a single TES. In the latter case, the schematic would show several cantilevered absorbers coupled to each TES. This option is discussed in detail in Section 3.3. Fig. 3.2 is a schematic of the composite XMS array. For separate optimization of the inner and outer array design parameters, these two main components should be fabricated independently. The outer array may or may not be sub-divided further into small sub-arrays. The details of the layout are the subject of the Focal-Plane Assembly trade study (SRON-XMS-RP-2010-008).

All array options need heat-sinking features to reduce thermal crosstalk and to minimize temperature gradients across the array. The requirements for this heat sinking will depend on the power dissipated, the electrothermal loop gain of the pixels, and the array architecture. Heat sinking will be an important factor to use in comparing design options.

The electrical connection to each TES is made via Nb microstrip leads, presumably ending in aluminum wirebond pads at the perimeter of the chip. Microstrip technology minimizes electrical crosstalk in high-density leads. All options will need to use microstrip leads, but the relative reliability of their integration could potentially be used to distinguish between options.

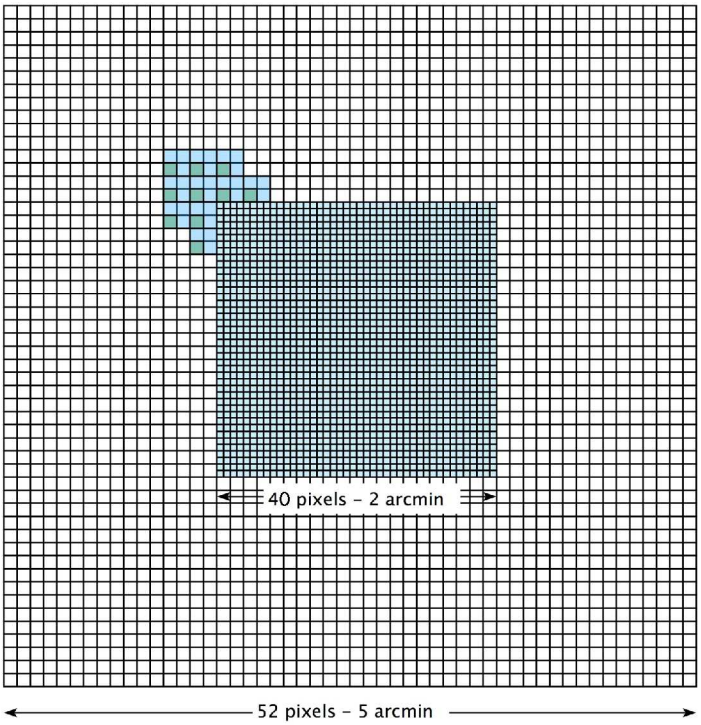

Fig. 3.2 – Schematic of XMS composite calorimeter. The core array covers a 2-arcmin FOV and consists of 3 arc sec pixels (0.3 x 0.3 mm) with one absorber per TES. The full array covers a 5-arcmin FOV. In one option, the outer consistst of 6-arcsec pixels that are read out by one TES per four absorbers (shown in one area by coloring groups of 4 pixels, each with one TES indicated in green).

3.1 Core array: GSFC/NIST option

3.1.1 Description of principle

Table 3.2.1 summarizes the parameters of the reference pixel design for the GSFC/NIST approach. The values for C, G, R, T_c, α_I , and β_I apply to the quiescent bias point. The reference design presumes use of a 0.24 mΩ biasing shunt resistor; though not a detector parameter, the shunt resistor affects the performance and thus is specified for the purpose of comparing the performance of the two approaches.

Table 3.2.1 GSFC/NIST reference pixel parameters

Parameters	Value	Comments
T_C	90 mK	A bath temperature of T_{bath} = 50 mK is assumed
TES normal resistance	8 mΩ/□	Based on existing devices
Bias resistance	1 mΩ	Based on existing devices
α_I	75	Based on existing devices
β_I	1.25	Based on existing devices
n	3	Typical measured value
C	0.8 pJ/K	Total device heat capacity
G	200 pW/K	Typical measured value, results in ~ 5 pW bias power

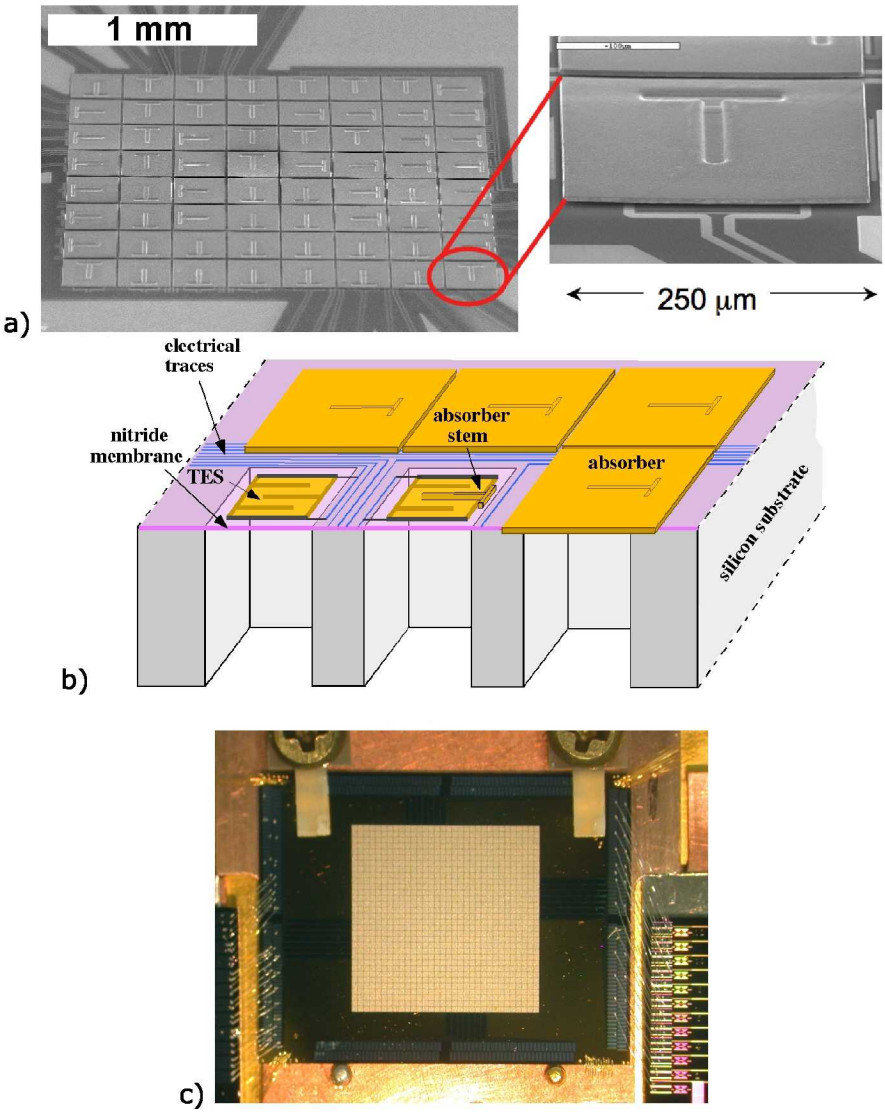

Fig 3.3– a) Electron micrograph of a Goddard uniform TES array with Au absorbers. The close-up view on the right shows an individual pixel. The absorber is cantilevered over the underlying substrate everywhere except in the T-shaped contact area. b) Schematic showing the structure of a TES array made in the Goddard style. c) 32x32 array with Au/Bi absorbers

The basic TES device of the GSFC/NIST option, described in RD1, consists of a 0.14-mm-square Mo/Au bilayer transition-edge thermometer, a silicon-nitride membrane (typically 1 μm thick) to form an engineered thermal link to the heat sink, and an X-ray absorber to increase the quantum efficiency. The membranes are defined by using deep reactive ion etching (DRIE) to etch straight from the back of a 0.3-mm-thick silicon wafer to the front-side nitride layer (see Fig. 3.3). The Mo/Au bilayers are produced using electron-beam deposition under ultra-high vacuum conditions. Atop the bilayer, additional Au features are patterned (refer

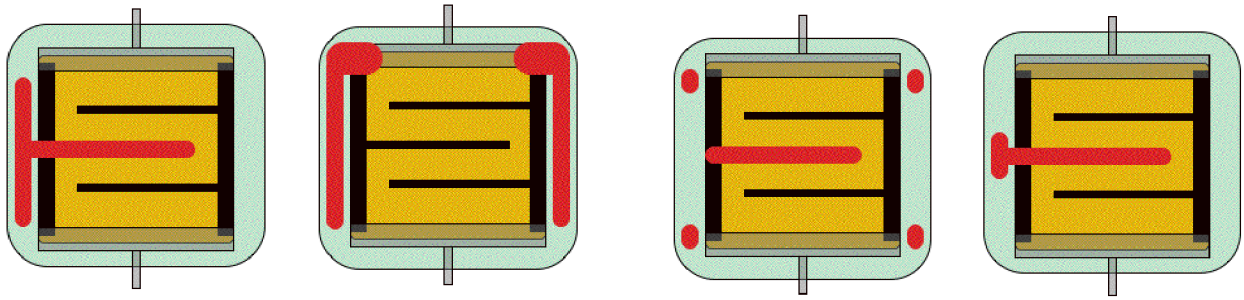

Fig. 3.4 – Several successful configurations for the absorber stem. The layout of the square bi-layer TES, gold stripes, and superconducting electrical contacts (orange, black, and gray) is shown schematically. The nitride membrane is shown in pale green. The absorber makes contact only in the red regions.

to Figs. 3.3b and 3.4). Banks of thick Au are put along the edges parallel to the current flow to define the superconducting boundary condition and make the transition shape more uniform than if the superconducting boundary were etch-defined. Interdigitated gold stripes are oriented perpendicularly to the current flow, which has been shown to diminish the excess white noise associated with TES devices [RD2, RD3]. For the reference design, three interdigitated Au stripes are presumed, because devices with such features have been the most extensively characterized. The superconducting transitions of these devices are about 0.5-mK wide when measured with low current. Under bias, the logarithmic temperature sensitivity, α_I = dlog(R)/dlog(T) at constant I, ranges from about 50 - 150 at a bias resistance around 20% of the normal resistance. The logarithmic current sensitivity, β_I = dlog(R)/dlog(I) at constant T, ranges from about 1 -2 at the same bias point (for a G ~ 200 pW/K and an operating temperature ~ 90 mK). Noise models infer a Johnson voltage noise of $[4kTR(1+2\beta)]^{0.5}$, in agreement with Irwin's prediction for a non-Ohmic resistance near equilibrium [RD4]). There is no significant excess noise.

In order to achieve detector-noise-limited energy resolution, the X-ray absorber must thermalize the energy of incident photons rapidly, reproducibly, and without dependence on the location of absorption. The reference design uses absorbers that are cantilevered over the active part of the TES itself, making contact only at the normal metal features that are already part of the design. These regions are available for making good thermal contact between the TES and absorber without destroying the sensitivity of the TES. The normal-state resistance of these TES devices is 8 – 10 mΩ, and they are typically operated at a resistance of ~1 mΩ. The design of the absorber contacts must not only avoid the active region of the TES, but also avoid contact that would provide a parallel current path through the absorber. The absorber designs include contacts to the membrane outside of the TES to provide adequate mechanical support for the cantilevered absorber. Various absorber attachment schemes are shown in Fig. 3.4. In each of the figures, the absorber is supported only at the regions shown in red. Early success with the T-shaped absorber contacts led to their incorporation into all the GSFC tests of uniform arrays, thus that is the presumed configuration of this reference design. The absorbers consist of a layer of electroplated Au capped by electroplated Bi, adjusted to optimize the combined thermalization, heat capacity, and quantum efficiency. The heat capacity goal is 0.8 pJ/K at 90 mK.

The bias power in reference design is 5 pW/pixel, or 80 nW distributed across the entire core array. The primary means of heatsinking the arrays is via gold wirebonds from gold-coated regions of the top of the

array to the detector housing. Analysis of the thermal properties of 8x8 arrays has indicated that the grid of 0.3-mm-thick silicon in which the pixel membranes are suspended is not adequate to carrying this load. Thus, it is planned to include a metallic heatsinking grid. This is also not adequate if simply deposited on the back of the silicon grid, because the heat needs to spread out over several unit cells of the silicon grid before it can effectively couple into the metal on the back (due to electron-phonon coupling and boundary resistances). The metallization needs to be brought toward the device side of the chip. Metallization of the sidewalls of the wells under each membrane will soon be characterized. Top-side metallization, using planarized electroplated microtrenches capped by an insulator, atop which the microtrench leads are run, would allow for even higher heatsinking.

3.1.2 Performance limits

The resolution requirement is a system requirement. Therefore, the intrinsic TES performance must be considerably better than 2.5 eV. Margin must be allocated to amplifier noise, bias noise, temperature instability, gain instability, and photon shot noise. We have made a preliminary noise budget (IXO-TN-001141) that is based on allocating an upper limit on the combination of intrinsic detector resolution, MUX noise, and finite record length of 2.3 eV FWHM. These terms are grouped together because the detector and readout characteristics need to be optimized in conjunction for a required counting rate. In IXO_MUX_NIST_GSFC_v1.pdf, the allocations within that 2.3 eV limit are described for the reference pixel presented in 3.1.1 for a Time-Division Multiplexer. The pixel itself has intrinsic performance of 1.71 eV FWHM. The MUX noise allocation raises that to 2.01 eV FWHM, and the choice of record length (and pre-record exclusion interval) required to meet the count rate requirement brings the total to 2.3 eV. (See RD5 for discussion of the dependence of resolution on record length. Note that for observations that don't require counting rates at the high-count-rate limit, longer records may be used to obtain higher resolution.)

The resolution of 1.71 eV is predicted by an ideal calorimeter model (no internal thermal decoupling) with no additional noise sources. (The first-order expanded form for the Johnson noise of a non-Ohmic resistor is used.) We have found that simple calorimeter models well describe the complex impedance of calorimeters with parameters similar to those of the reference design. The actual measured resolution at 6 keV (and inferred from the measured NEP, scaled to the pulse heights) tends to agree with the model when the intrinsic resolution of the model has been larger than about 2.2 eV (e.g. for a series of devices with solid gold absorbers). Devices with lower heat capacity and better expected resolution generally have not demonstrated the model resolution, but no careful accounting has yet been attempted to put limits on the various non-intrinsic terms (all the other terms in the noise budget) that are relevant in the laboratory measurements. An example of the impact of such terms was presented in RD6 which describes a TES that exhibited 2.1 eV resolution without data cuts. When data were selected based on the DC level of the signal channel prior to a pulse, which is representative of the TES temperature just before the X-ray is absorbed, a fit to the resulting histogram indicated a resolution of 1.8 eV FWHM. Such a data cut removes sensitivity to slight variations in the TES bias point that may be due to any of a number of systems issues. Therefore, limiting the impact of systems issues, and quantifying the impacts when they can no longer be reduced, will be essential in actually demonstrating that the required performance has been achieved.

The parameters of the reference pixel are based on the parameters of a series of uniform 8x8 arrays made at GSFC (see RD7). The transition temperature of the reference design has been reduced slightly compared with measured devices to provide more margin. More significantly, the baseline pixel pitch is now 0.3 mm, compared with the 0.25 mm of the basis array. Thus, the thicknesses of the Bi and Au layers need to be

adjusted to achieve 0.8 pJ/K at 90 mK in a larger area. As the Bi thickness is increased relative to the Au, prevailing uncertainties in the actual specific heat of the electroplated Bi become more important. The current target is 1 μm of Au and 4 μm of Bi.

3.2 Core array: SRON/ISAS option

3.2.1 Description of principle

a) SRON option

The following parameters, see table 3.2.1, define the SRON reference pixel for the core array. Use of a shunt resistor of 3 mΩ is presumed for the purpose of comparing the performance of the two approaches.

Table 3.2.1 SRON reference pixel parameters

Parameters	Value	Comments
T_C	100 mK	A bath temperature of T_{bath} = 50 mK is assumed
TES normal resistance	100 mΩ/□	About a 4x lower value than in standard SRON-pixels to guarantee better heat conductance and prevent decoupling (≈ 20nmTi/100nmAu)
Bias resistance	20 mΩ	Well tuned to FDM and its SQUID noise levels.
α_I	100	At 20 mΩ biaspoint. Tuned by tuning structures on the Ti/Au bilayer
β_I	0.65	Based on measured Ginzburg-Landau relations between α_I and β_I on standard SRON-pixels and an critical current estimated of 16 μA
n	3.5	Typical measured value
C_{TES}	0.03 pJ/K	Based on 150 x 150 μm^2 TES of 20 nm Ti and 100 nm Au (TBC)
C_{ABS}	0.95 pJ/K	For a 290 x 290 μm^2 of Cu/Bi absorber of 300 nm Cu and 4.5 μm Bi. This has an absorption efficiency of 77% @ 7 keV.
G	192 pW/K	Pixels designed to 5 pW bias power at nominal 20 mΩ biaspoint

The above values are different from SRON-pixels made and tested so far. The existing pixels suffer from an increase of excess noise for device with a full absorber attached to it, which seems to be related to the chosen absorber coupling scheme with the large central stem. SRON is in the process of revisiting their pixel design with the following aims:

- An absorber coupling interface with the TES that minimizes impact on TES parameters and bias current flow
- Improvement of the heat conductance of the TES (thicker TES) to reduce potential internal decoupling of TES and absorber (internal noise source) and an increase of the critical current (which decreases β_I) by making the TES thicker (from 15/40 nm Ti/Au to about 20/100 nm Ti/Au)
- Reduction of pixel speed (IXO requirements are significant relaxed compared to those of XEUS) by reducing the heat conductance G top the bath
- Include α_I tuning structures on TES to enable tuning it to the design value of 100, and potentially also suppressing excess noise

The interface of these pixels with the already developed pixel array support structure and heat sinking structures remains unchanged.

The SRON pixel support structure is made out of Si with a 110 crystal orientation That allows for the fabrication of long extremely smooth support bars by wet etching techniques. The Si-support beams are coated with Cu (0.75 μm) to increase the heat conductivity and heat capacity of the bars. Heat sinking is required to get a uniform base temperature over the array, to reduce thermal crosstalk between pixels, and to suppress cosmic ray events in the detector support structure. For typical values (90 μm Si bar width, 0.75 μm Cu on side walls, and 1.5 μm Cu on the wafer bottom) the central pixels of a 32 x 32 array are sunk to a 2 mK higher bath temperature than the pixels at the edge for 5 pW bias power per pixel. These calculations have been verified by measurements. Heat sinking also reduces the measured thermal crosstalk between neighboring pixels to a measured value of 4 10^{-4} , close to the 2 10^{-4} modeled value.

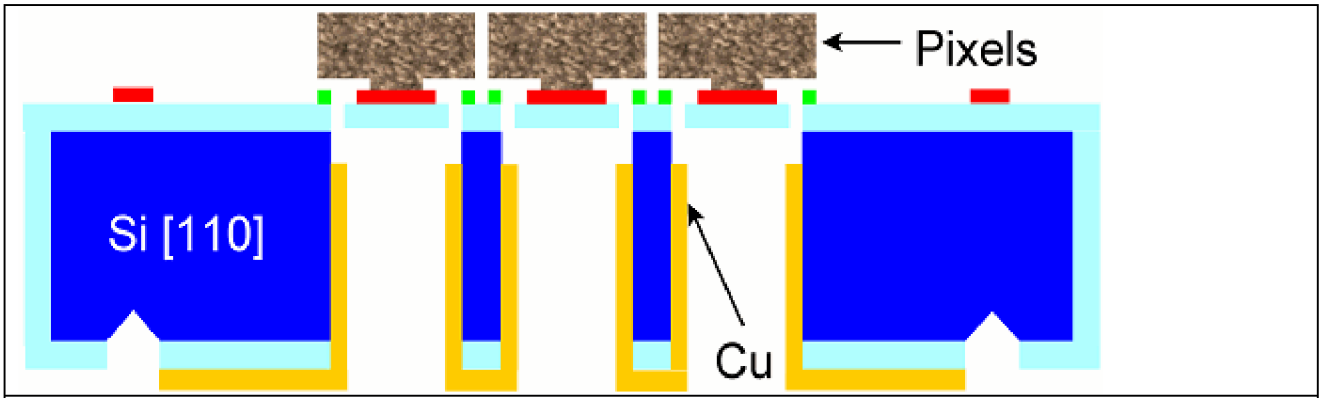

Figure 3.2.1: Dark blue (110 Si), Light blue (1 μm Si_3N_4), red (Ti/Au TES), green (Nb leads), brown (CuBi absorbers. The supporting structure is formed by etching deep, vertical slots in the backside of a Si [110] wafer, using anisotropic wet etching. The pixel structure on top is formed by e-beam evaporation, sputter deposition, etching and lift-off processing techniques. Cu is shadow deposited on the backside and side walls of the Si-beam structure to improve the thermal conductivity and heat capacity of the pixels support stucture

The TES bilayer is evaporated on top of the Si_3N_4 membrane after wet etching of the Si-bar support structure. After patterning these layers by RIE, the Nb-leads are deposited using lift-off. The development of high density microstrip lines might actually change this fabrication flow. Finally slots are etched in the Si_3N_4 membrane to thermally separate pixels supported by the same two Si-bars. A top view of such a wafer is shown in figure 3.2.2 for a 5 x 5 array.

The last steps in this process are the production of CuBi overhanging absorber structures. The process makes use of sputtered layers of Cu (0.15 – 0.3 μm) and Bi (up to 4 μm) in a single resist mould structured by various illuminations. The process successfully produced full CuBi absorbers of the indicated thicknesses. Different absorber coupling structures as envisaged for the *new* SRON pixels, which most probably will set higher requirements on heat conduction (diffusion speed) in the absorbers. That might require absorber deposition technology with a higher RRR (electroplating).

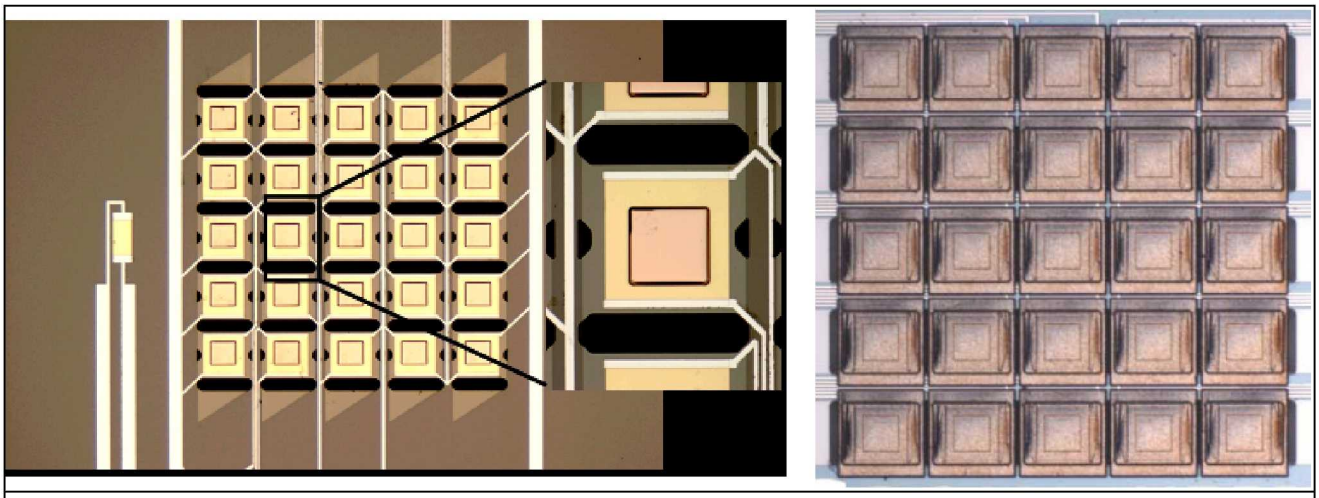

Figure 3.2.2: Top view of a 5 x 5 array. Left: The 5 x 5 array is carried by 4 Si-bars (vertical) created by wet etching the 110 Si. The yellow structures are the Ti/Au TES structured to about 150 x 150μm^2 using RIE. The Nb electrical leads run over the Si-bars. These pixels have central 100 x 100 x 1 μm^3 Cu absorbers. On the right side one of the pixels is shown in an enlarged view. Right: Similar array equipped with CuBi absorbers

b) ISAS/MTU option

The parameters shown below define the ISAS reference pixel for the core array.

Table 3.2.2 ISAS/MTU reference pixel parameters

Parameters	Value	Comments
T_C	100 mK	A bath temperature of T_{bath} = 50 mK is assumed
TES normal resistance	100 mΩ/□	A typical measured value based on 200 x 200 μm^2 TES of 40 nm Ti/ 100 nm Au.
Bias resistance	20 mΩ	A typical measured value.
α_I	80	At 20 mΩ bias point.
β_I	0.5	Based on measured relation between α_I and β_I.
n	3.5	A typical measured value
M	2.7	Excess noise factor. Based on measured relation between α_I and M.
C_{TES}	0.05 pJ/K	Based on 150 x 150 μm^2 TES of 40 nm Ti and 100 nm Au.
C_{ABS}	0.75 pJ/K	Based on 290 x 290 μm^2 of Au/Bi absorber of 300 nm Au and 5 μm Bi. Heat capacity of Bi has to be measured.
G	300 pW/K	A typical measured value.

Similar to the SRON case, the pixel geometry is different from a standard ISAS pixel (200 x 200 μm^2 TES of 40 nm Ti/ 100 nm Au with 120x120 μm^2 Au absorber. The best energy resolution of this type is 2.8 eV (FWHM) [RD8].

Figure 3.2.3 shows the aimed structure of the ISAS pixel. First, the Au/Ti TES bilayer is sputtered on a 300 μm-thick Si (100) wafer with a 300 nm SiN_x and 400 nm SiO_2 layer. Next, the Au and Ti layers are patterned by using wet etching processes. Then, superconducting readout wires are deposited upon the TES. The TES

deposition process may take place between the upper and lower wiring formation. Next, the overhanging absorber is deposited on the TES by electron-beam evaporation. The deep reactive ion etching (DRIE) process (and a additional wet etching technique at last if necessary) is used to form the SiN_x and SiO_2 membrane structure. Here the SiO_2 film is used as etch stop for DRIE. Finally, a thin Au layer as a heat path is deposited by electron beam deposition or sputtering on the backside of the wafer.

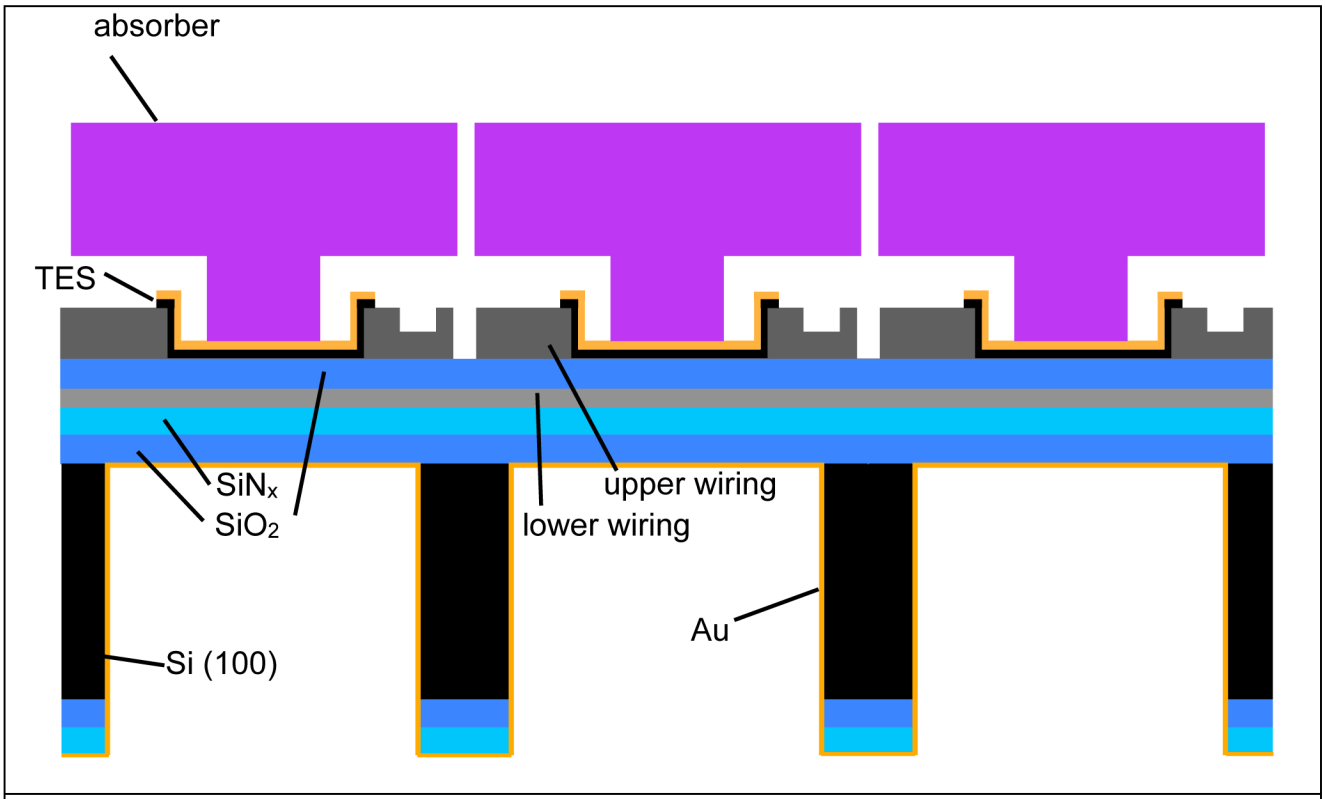

Figure 3.2.3: Schematic view of the ISAS reference pixel. The supporting structure is formed by DRIE (+ KOH wet etching). The pixel structure on top is formed by sputter (TES, readout wirings), e-beam evaporation (absorber) deposition, etching and lift-off processing techniques. Multilayer wiring is used to save spaces of readout wirings. Au is deposited on the backside to improve the thermal conductivity and heat capacity of the pixels support structure.

The necessary array fabrication technologies, namely multilayer wiring, overhanging absorber, and backside Au deposition, are under development. Figure 3.2.4 shows a top view of a 16 x 16 TES array sample [RD9] and a multilayer wiring sample for a 20 x 20 TES array.

The estimated intrinsic resolution of the ISAS pixel considering β_I and the excess noise M factor is 2.3 eV, which can satisfy the IXO XMS requirement (2.5 eV). However, the margin is small, hence the addition of an excess-noise-mitigation pattern upon the TES is being investigated [RD10].

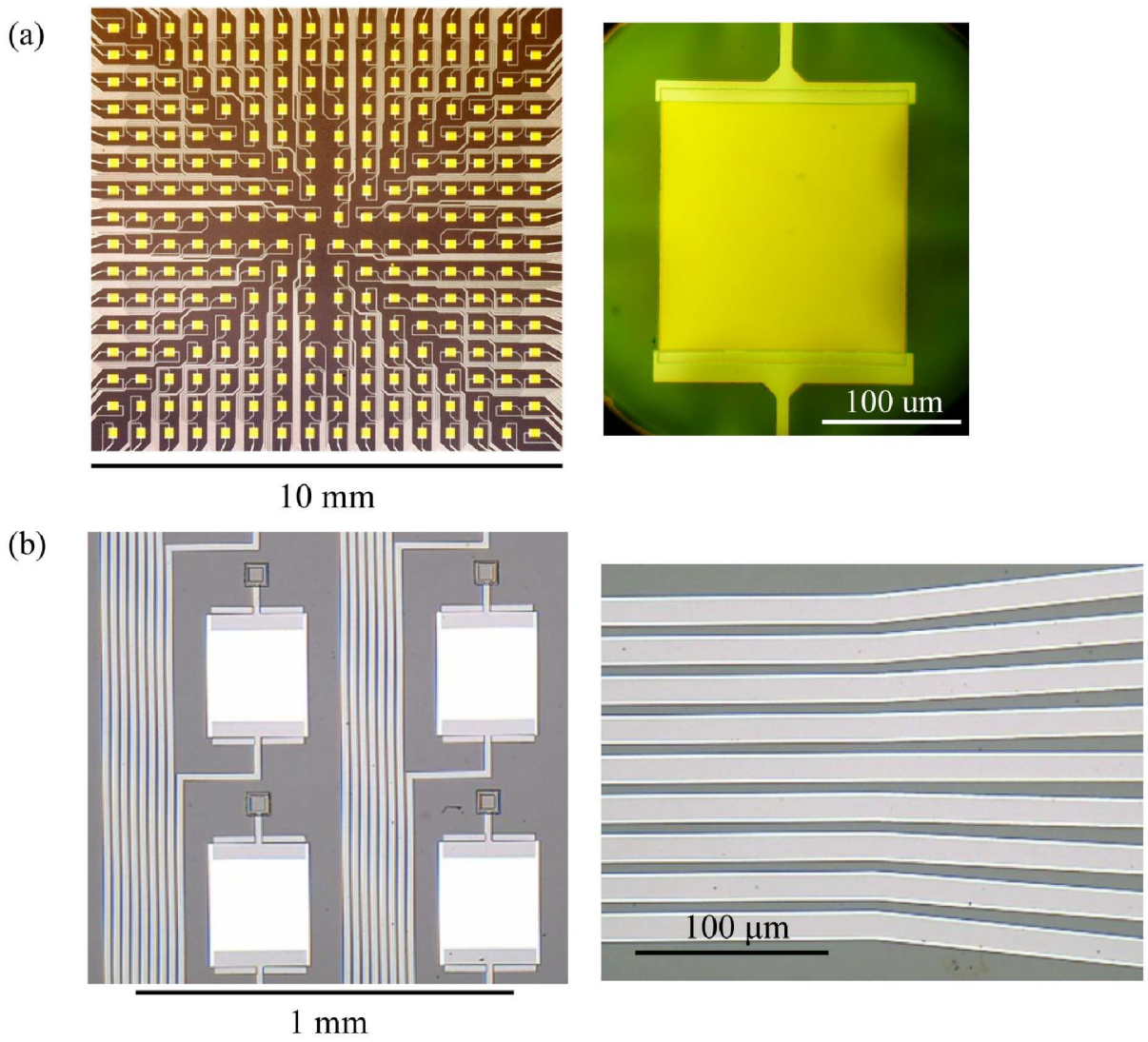

Figure 3.2.4: (a) Top view of 16 x 16 TES pixel without absorbers. The left viewgraph shows the central part of the array before DRIE, while the right is the close up view of a single pixel after DRIE. (b) Top view of a multilayer readout wiring sample for a 20x20 TES array. The upper (Nb) and lower (Al) wirings, whose widths are 10 and 15 µm, respectively, sandwich a thin PECVD-deposited SiO2 insulation layer with a thickness of 100 nm. Because of the thinness, the insulation layer is difficult to see in the picture. These two wiring layers are connected via a contact hole which is located above each pixel (square structure). On this array, the TES and absorber will be formed.

c) Common SRON/ISAS detector for the trade-off

To facilitate ease of the trade-off we will use a single SRON/ISAS design based upon:

- SRON pixel reference parameters in Table 3.2.1 (The ISAS parameters are actually very similar)
- SRON pixel layout enhanced by developments at ISAS, especially with regard to the development of double layer wiring

3.2.2 Performance limits

The actual measured energy resolution limit on SRON devices is 1.56 eV @ 250 eV, and 2.5 eV @ 6 keV on devices without high-fill-factor absorbers. The performance can be described in terms of nominal performance degraded by a dangling heat capacity of about 0.04 pJ/K, and excess noise consistent with M ≈ 1. Performance in devices with appropriate absorbers has been limited to about 4 eV by higher excess noise values (M > 1).

Using the TES parameters given in Table 3.2.1 the small signal energy resolution can be calculated. In the ideal case, no decoupled heat capacities and no excess noise above the non-Ohmic Johnson voltage noise of $[4kTR(1+2\beta_I)]^{0.5}$, the energy resolution equals 1.60 eV for a detector read-out by noise-free electronics. In case of the use of TDM this results in a resolution of about 2.3 eV, including TDM read-out noise and finite record length (2.81 ms) contributions. Together with additional errors from drifts, etc this guarantees a total pixel resolution of 2.5 eV FWHM.

In case of read-out by FDM and CDM the system has margin to lower the noise contribution from the read-out electronics to the total energy resolution. This allows for some margins on the pixel performance, since ideal pixel performance might be difficult to achieve. So far the SRON pixels show evidence for a decoupled heat capacity, most likely due to the membrane. For typical parameters (C < 0.04 pJ/K, G ≈ 4 10^{-10} W/K; [RD11]), which seem to be device geometry dependent, the energy resolution is raised from 1.6 to about 2.0 eV. More work is needed to characterize this effect and find means to suppress it.

In the current SRON devices some excess noise exists, which can be described by M ≈ 1 (RD11). If still present in the new type of devices this would raise the energy resolution from 1.6 to 1.9 eV. It is expected that the α_I-tuning structure will also reduce the excess noise.

3.3 Outer array: Hydras

3.3.1 Description of principle

One approach under development by GSFC for the IXO extended focal-plane array is the Hydra. The Hydra [RD12] is a position-sensitive microcalorimeter consisting of multiple absorber pixels each with a different thermal coupling to a single read-out TES. Depending upon which pixel a photon has been absorbed in, the TES will measure a different characteristic signal. After this initial position-dependent equilibration signal, the pulses decay with the same exponential rate. Position information is encoded in the pre-equilibration pulse shape, which can be determined using simple rise-time algorithms [RD13] or if increased sensitivity is required (typically at lower energies), more complicated signal processing algorithms may be implemented [RD14]. The photon energy is then calculated using a single stored digital optimal filter referenced for each absorber element. Fig. 3.3.1.1 shows a simple thermal model of a 4-pixel Hydra, also shown is the time evolution of the measured signals at the TES. The motivation for the development of the Hydra is to provide an extended focal-plane array of 2304 6" pixels surrounding the core-array, thus expanding the field-of-view

from 2' to 5.4' while only adding an extra 576 read-out channels to the total focal-plane array (36% of the core array). This is equivalent to an extra 18 TDM columns each having 32 rows.

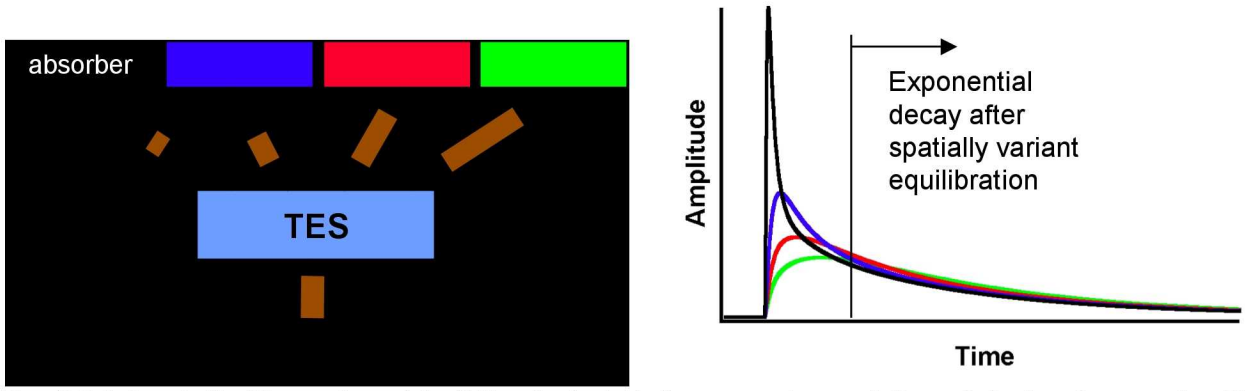

Fig. 3.3.1.1 – Left: Thermal model of the 4-pixel Hydra concept, consisting of 4 absorbers each with a different thermal conductance link to the TES. Right: Time evolution of pulse shape measured by the TES corresponding to photon absorption in each of the 4 absorbers. Position discrimination between the absorbers is achieved using the pre-equilibration signal, typically from the pulse rise-time.

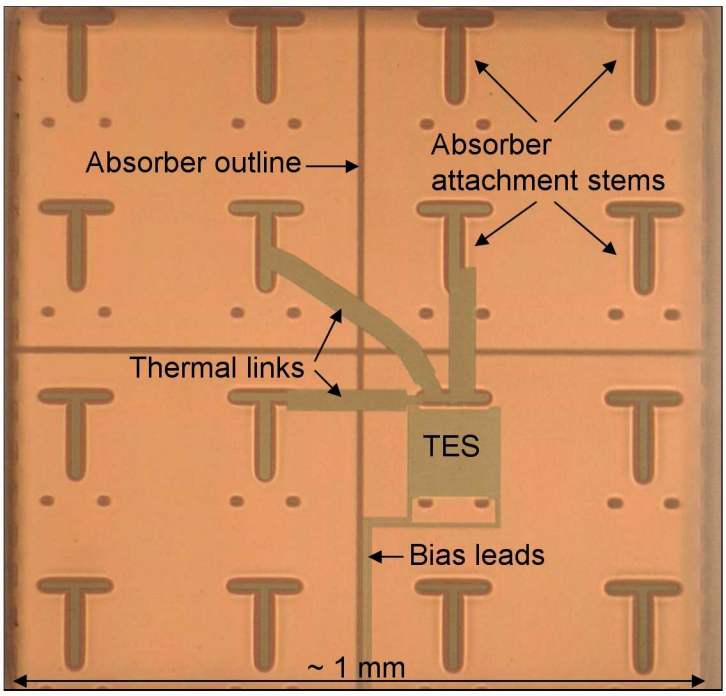

Fig. 3.3.1.2 – Optical micrograph of a 4-pixel Hydra. The image is taken looking through the back of the SiN_x membrane. Clearly visible is the outline of the TES, absorber stems and internal thermal links that couple each absorber to the TES. Each absorber pixel is 600 μm x 600 μm.

The basic approach to the Hydra design utilizes identical Mo/Au bilayer technology as the GSFC/NIST core array reference pixel (described in Section 3.1.1.). Because the pixel size is increased by a factor of two over

the core array, each 600 μm pixel now has four attachment stems supporting the absorber above the SiN_x membrane. For the most strongly coupled absorber, one of the attachment stems is directly deposited over the TES (the same as the core array). The three other absorbers are coupled to the TES via thin (200-400 nm) evaporated Au links deposited directly on the membrane. By varying the length and width of these links the thermal conductance can be tuned to give the appropriate position discrimination between pixels. The absorber thickness and composition will be identical to that of the core array. The entire structure is fabricated on a single 1 mm x 1 mm SiN_x membrane. By adding perforations around the edge of the membrane, the thermal conductance to the heat sink can be tuned as required. Fig. 3.3.1.2 shows an optical micrograph of a 4-pixel (600 um) GSFC Hydra. The image, taken looking through the back of the membrane, clearly shows the different components that make up the Hydra design. The parameters for the extended array Hydra reference pixel are listed Table 3.3.1.1.

Table. 3.3.1.1 – Table of parameters for 4-pixel Hydra

Parameter	Value	Comments
T_c	75 mK	Transition temperature
T_{bath}	50 mK	Heat sink temperature
$C(T_c)$	10.8 pJ/K	Total heat capacity
$G(T_c)$	1.8 nW/K	Heat sink conductance
$G_{L1}(T_c)$	~ 1 mW/K	Conductance to TES of most strongly coupled absorber (pixel 1)
$G_{L2}(T_c)$	45 nW/K	Link conductance between decoupled absorber and TES (pixel 2)
$G_{L3}(T_c)$	28 nW/K	Link conductance between decoupled absorber and TES (pixel 3)
$G_{L4}(T_c)$	19 nW/K	Link conductance between decoupled absorber and TES (pixel 4)
n	3	Temperature exponent of thermal conductance
α_I	75	TES resistance-temperature sensitivity
β_I	2.29	TES resistance-current sensitivity, estimated from GL theory
R	1 mΩ	Operating point resistance (R_N ~ 7 mΩ)
L	250 nH	Input inductance to SQUID (not critically damped)
R_L	200 μΩ	Voltage bias load resister value
τ_{eff}	1.19 ms	Electro-thermal decay time
τ_L	936.22 μs	Fitted decay time in presence of inductance L
Ibias	176.8 μA	TES bias current at operating point
Power	31.3 pW	TES bias power at operating point
Total Power	18 nW	Total power dissipation from all 576 TES's

The power dissipated within the entire extended array is estimated to be 18 nW and will require identical heat-sinking approaches as discussed in Section 3.1.1 for the core array.

3.3.2 Performance limits

Since four 6" absorber pixels are thermally coupled to a single TES, the measured energy resolution will, to first order, be ~ 2 times degraded compared to a single 6" pixel with identical design parameters ($\Delta E \propto \sqrt{C}$). In addition, the thermal links between the absorbers and the TES affects both the detector signal and noise. The links add internal thermal fluctuation noise between the absorber elements and the sensor, which can have a degrading effect on resolution. These links also attenuate the signal for the decoupled absorbers relative to the noise and result in a further resolution degradation depending upon pixel. Thus the ability to distinguish position comes at some expense in detector energy resolution. For typical design optimizations

requiring good energy resolution coupled with position sensitivity over the keV energy range, this degradation is ~ 30%. In order to meet the ~ 10 eV target resolution, the operating temperature is reduced to 75 mK (compared to 90 mK for the core array). The target thicknesses are 1 μm Au and 4 μm Bi and the estimated total heat capacity is then 10.8 pJ/K. The reduction in operating temperature comes at some penalty in temperature stability. However, since the baseline resolution is already ~ 10 eV, a 0.2 eV / uK broadening at 75 mK does not impact performance significantly. The total estimated error budget degrades the average energy resolution across all 4 pixels to ~ 11 eV. A SQUID noise level of 20 pA/rt(Hz) for a 32 row TDM system is assumed (2 pA/rt(Hz) per row). The area of the Hydra per readout sensor is 16 times larger than a pixel in the core array, and the total device heat capacity is > 10 times larger. Consequently the count-rate capability is degraded by approximately two orders of magnitude. Thus in order to meet the required count-rate of 2 cps per 6" position-sensing element (equivalent to 8 cps per Hydra) an order of magnitude increase in the heat sink thermal conductance is required, as a result the bias current and dissipated power per TES are all also significantly increased (see Table 3.3.1.1). The energy resolution including effects of TDM degradation and finite record length are listed in Table 3.3.2.1.

Table 3.3.2.1 - Energy resolution (FWHM) for each pixel. Included is the intrinsic baseline resolution, resolution including TDM aliased SQUID noise degradation and resolution including finite record length degradation.

	Pixel 1	**Pixel 2**	**Pixel 3**	**Pixel 4**	**Average**
Baseline	6.58 eV	8.29 eV	8.64 eV	9.01 eV	8.13 eV
TDM degradation	7.71 eV	8.51 eV	8.83 eV	9.19 eV	8.56 eV
Finite record length degradation	7.00 eV	9.16 eV	9.62 eV	10.13 eV	8.98 eV
TDM and finite record length degradation	8.39 eV	9.42 eV	9.84 eV	10.33 eV	9.50 eV

3.4 Outer array: Large-scale MUX

3.4.1 Description of principle

An alternative approach for the IXO extended focal-plane is to multiplex a larger number of single (600 micron pitch) pixel TESs. By designing these pixels for reduced bandwidth compared to the core array pixels, the entire 2304 elements in the extended array can in principle be read out without requiring addition resources from the read-out electronics compared the Hydra approach. In TDM this means increasing the number of multiplexed rows in a column so that the total number of columns is maintained for the entire extended array.

In this approach, either every pixel can be inductively coupled to a single SQUID or, alternatively, multiple pixels (typically 2 or 4) can be coupled to the SQUID. In the latter case, position discrimination between different pixels coupled to the same SQUID can be achieved from pulse shape by using pixels with different coupling polarities to the SQUID, operational bias points, heat-sink conductances or coupling inductances [*RD15*] (see Fig. 3.4.1.1). These different approaches lead to different optimizations of the detector design parameters to meet the performance requirements, which will be discussed further in the next sections. Compared to the thermal multiplexing used in the Hydra concept, the large-scale electrical multiplexing approach requires each 6" position element to have its own TES with electrical bias circuit, which (depending

upon the number of pixels ultimately coupled to each SQUID) has implications for design of the read-out chain, focal-plane assembly and cooling chain.

As with the Hydra design discussed in the previous section, the single pixel MUXing approach uses the same Mo/Au bilayer technology as the GSFC/NIST core array reference pixel (described in Section 3.1.1.). Each 600 μm pixel has four attachment stems supporting the absorber above a single 500 μm SiN_x membrane. Fig. 3.4.1.2 shows optical and SEM imagines of typical test arrays under development at GSFC.

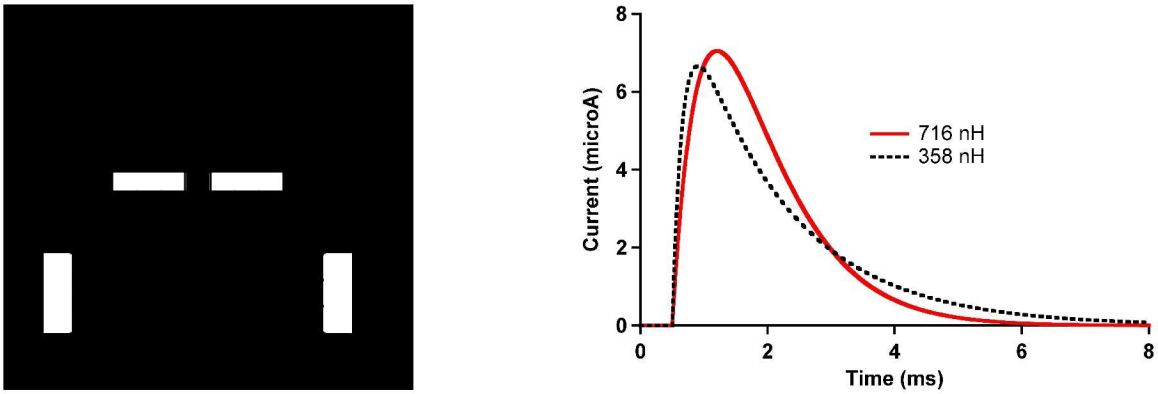

Fig. 3.4.1.1 – Left: Schematic circuit diagram showing 4 TESs inductively coupled to a single SQUID readout. Right: Simulated pulse shapes for 2 TESs coupled to a single SQUID using different input inductances. Two additional, identical pixels can be coupled to the same SQUID using opposite coupling polarities to enable position discrimination across a four-pixel device.

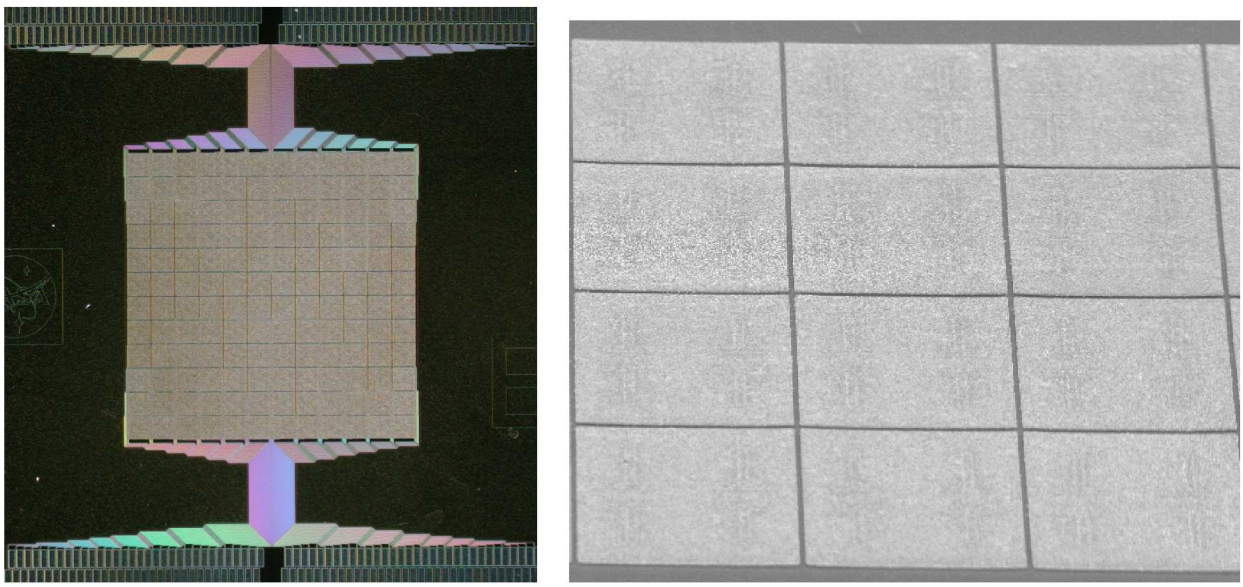

Fig. 3.4.1.2 – Left: Optical photograph of a 12 x 12 test array of 600 μm x 600 μm single pixel TESs under development at GSFC for the IXO extended array. Right: Scanning electron microscope image showing a similar array of 500 μm x 500 μm detectors with composite Au/Bi absorbers.

Table. 3.4.1.1 – Table of parameters for 1, 2 and 4 pixels coupled to a single SQUID readout. For N = 2, we assume position discrimination by pulse polarity, for N = 4 a combination of pulse polarity and different input inductances are used.

Parameter	Value			Comments
N	1	2	4	Number of TES's / SQUID
T_c	90 mK	90 mK	90 mK	Transition temperature
T_{bath}	50 mK	50 mK	50 mK	Heat sink temperature
$C(T_c)$	3.2 pJ/K	3.2 pJ/K	3.2 pJ/K	Heat capacity per pixel
$G(T_c)$	200 pW/K	400 pW/K	800 pW/K	Heat sink conductance
n	3	3	3	Temperature exponent of G
α_I	75	75	75	Resistance-temperature sensitivity
β_I	1.25	1.56	1.97	Resistance-current sensitivity, from GL
R	1 mΩ	1 mΩ	1 mΩ	Operating point resistance (R_N ~ 7 mΩ)
L	608.4 nH	361.5 nH	220 nH, 110 nH	Input inductance
R_L	200 μΩ	200 μΩ	200 μΩ	Voltage bias load resister value
τ_{eff}	2.06 ms	1.14 ms	642 μs	Electro-thermal decay time (L = 0)
τ_{crit}	608 μs	387 μs	211 μs, 487 μs*	Critically damped decay time
I_{bias}	70.5 μA	100 μA	141 μA	TES bias current at operating point
P_{bias}	5.0 pW	9.7 pW	19.9 pW	TES bias power at operating point
P_{array}	11.5 nW	22.3 nW	45.8 nW	Total power from array: P_{bias} x 2304

** Since different inductances are used for position discrimination, this is the fitted decay time to the non-critically damped pulse.*

3.4.2 Performance limits

The number of TES pixels coupled to the SQUID makes a significant difference to the energy resolution and the count-rate ability of the detector. Since all detector noise sources add to the single readout SQUID the resolution will scale as the square root of the total number of pixels *N*. Similarly the area coupled to a single SQUID increases with *N* so the maximum count-rate ability will scale inversely with *N*. In TDM, increasing the number of rows per column increases the aliased SQUID noise. This scales with the square root of the total number of rows. Thus, the total SQUID noise is estimated at 20, 28 and 40 pA/rt(Hz) for a 32, 64 and 128 row TDM respectively (assuming 2 pA/rt(Hz) per SQUID). Since we are using one TES per 6" element (as opposed to one per four 6" elements in the Hydra case), each TES sees a lower total heat capacity and the detector intrinsically offers better maximum count-rate abilities. Consequently it is possible to design for higher maximum count rates than the specified 2 cps / 6" element requirement while maintaining the energy resolution requirement of ΔE < 10 eV. This is a significant advantage over the Hydra extended array concept. For this study we assume an input rate of 10 cps / 6" at 80% live time for *N* of 1 and 2, and 5 cps / 6" for *N* = 4. Since the count-rate scales with 1/*N*, the heat sink thermal conductances are scaled by *N* to compensate. For the case of *N* = 4, two different inductance values are assumed (see Table 3.4.1.1). This is required to achieve position sensitivity through pulse shape discrimination. Since the non-critically damped pulses are designed to be ~ 2x slower than the critically damped ones, the maximum count-rate for *N* = 4 will suffer a further reduction. Further increases in *G* are undesirable because the TDM bandwidth is assumed fixed, thus increasing the signal bandwidth will result in under-sampling of the pulses. Consequently, a reduced input rate of 5 cps / 6" is assumed. Table 3.4.2.1 summarizes the energy resolution for the cases of *N* = 1, 2 and 4.

Table 3.4.2.1 - Energy resolution (FWHM) for 1, 2, 4 pixels coupled to a single SQUID.

TES's per SQUID, *N*	**1**	**2**	**4**
Number of TDM rows	128	64	32
Number of TDM columns	18	18	18
Input rate / 6" pixel at 80% live time	10 cps	10 cps	5 cps
Baseline	3.39 eV	4.97 eV	7.34 eV
TDM degradation	3.87 eV	5.26 eV	7.52 eV
Finite record length degradation	3.91 eV	5.85 eV	8.12 eV
TDM and finite record length degradation	4.58 eV	6.29 eV	8.36 eV

Although the predicted resolution and count-rate performance of these extended array options offer significant advantages compared to the Hydra design, there are disadvantage from a number of practical considerations [RD15]. First, each pixel is required to have its own electrical bias circuit, thus increasing the density of wiring within the array. Furthermore, the number of required bond-pads sets the physical size of the focal-plane detector chips, so a four times increase in the number of bond pads (compared to the Hydra design) will require more space and add complexity to the focal-plane assembly design. Increasing the number TDM rows will increase the wiring from higher temperature stages, which in turn increases the conductive heat load to the cold stage. Increasing the number of rows also requires some redesign of the current TDM readout electronics. These factors will all need to be considered in the respective trade-studies before a final extended array design can be baselined.

4 Actual implementation and performance

In the following section, we discuss actual devices that have been made and the differences between the tests done and the implementations assumed in the different reference designs. Thus we establish the gap between each reference design and the closest actual devices made to date, and then we discuss the steps needed to close that gap in each case.

4.1 Core array: GSFC/NIST option

4.1.1 Actual devices

The parameters of the reference pixel are based on the parameters of a series of uniform 8x8 arrays made at GSFC. The transition temperature of the actual devices was slightly higher (96 mK) than that prescribed for the reference (90 mK). The values of C and G of the reference are the same as the basis pixels, just scaled appropriately by temperature. The values for α_I , and β_I and the bias point are taken directly from the best fits to impedance measurements of the basis pixels. No change is presumed in either the design of the thermometer element or the contact between the absorber and the thermometer. The reference design for the pixel in GSFC/NIST approach is meant to be a re-creation of these existing devices, with the absorber composition being the single exception. Since the baseline pixel pitch is now 0.3 mm, compared with the 0.25 mm of the basis array, the thicknesses of the Bi and Au layers need to be adjusted to achieve 0.8 pJ/K at 90 mK in a larger area. The nominal thicknesses of these layers in the basis array was 2.7 μm of Au and 3 μm of Bi, but post-facto attempts to verify this suggest both thicknesses were likely at least 25% lower. As the Bi thickness is increased relative to the Au, prevailing uncertainties in the actual specific heat of the electroplated Bi become more important. The current target is 1 μm of Au and 4 μm of Bi. This sort of

composition has been used successfully in even larger pixel designs and thus is expected to provide an adequately fast thermal equilibration time across the absorber. Occasional incidents of significantly higher heat capacity in the Bi underline the need for investment in process control.

Most data taken on the basis arrays were multiplexed, but during non-multiplexed operation, a spectral resolution of 2.30 eV was measured. This measurement was consistent, within statistical error, with the measured noise level of 2.18 eV. A detector model using fit detector parameters, with measured read-out noise, predicts 2.2 eV; this model indicates that the detector alone would be 1.9 eV. A careful accounting of the terms in the noise budget in the laboratory test platforms will be needed to confirm that the reference design actually has an intrinsic resolution of 1.7 eV.

Some tests of the larger pixel size have occurred within the context of developing larger (32x32) arrays. So far, the best resolution achieved is 2.7 eV, but performance thus far has been limited by equipment failure, insufficient process control, and process development associated with integrating microstrip leads.

In terms of array architecture, it has not yet become routine to add back-side heat-sinking to these arrays. Thus, most data have been taken on arrays with no back-side heatsinking, limiting the X-ray flux to minimize the noise from crosstalk and frame hits. When heat-sinking has been added, its characterization showed it to be about a factor of two too low (more discussion of this in Section 5.)

4.1.2 Steps needed for large arrays

Concepts for key components of a large array, high-density wiring, and array-scale heat sinking are well defined and are presently under development. The integration of microstrip wiring with the TES process has already gone through several refining iterations and no major change in approach is anticipated. Pixels in 32x32 arrays are already being characterized through microstrip leads, and, in a recent test, 12 out of 14 channels showed identical IV curves.

The needed improvements in heatsinking are understood and are achievable. The application of a Cu layer to the back of the array grid has already been demonstrated sufficient to handle the bias power of a full 40x40 array (via measurement of its conductance and calculation of the resulting thermal gradient expected in the XMS array). This metalized grid is not adequate for controlling thermal crosstalk, however, because the heat needs to spread out over several unit cells of the silicon grid before it can effectively couple into the metal on the back (due to electron-phonon coupling and boundary resistances). Coupling to that heat-sinking grid needs to be improved by a factor of 2-3 to maintain crosstalk noise below the level allocated in the noise budget. The short-term plan to achieve this is to remove processing residue from the sidewalls of the silicon frame that define the membrane area of each pixel and to coat those walls with heat-sinking Cu via angled evaporation. This increases the area for coupling into the Cu by a factor of 3. Metallization of the sidewalls of the wells under each membrane will soon be characterized. Top-side metallization, using planarized electroplated microtrenches capped by an insulator, atop which the microstrip leads are run, would allow for even stronger heat sinking. Such structures have been developed, but have not yet been integrated into array processing.

Heat sinking of alumina detector boards via gold wire bonds to thick gold-coated regions of the boards has achieved conductances at 50 mK at the required 10 μW/K needed for the array as a whole, but similar heat sinking of detector chips thus far has not achieved better than about 1 μW/K, despite similar quantities and

lengths of the wire bonds. An important difference may be the thickness of the gold (6 μm for the alumina boards, typically 1 μm for the detector heat sinks), thus the use of a thicker heat sinking layer on the detector frame, at least under the region of the wire-bond contacts, will be investigated.

4.2 Core array: SRON/ISAS option

4.2.1 Actual devices

The reference design for the SRON/ISAS option actually represents a re-optimization of that approach. Devices with the prescribed parameters have not yet been built. The existing pixels suffer from an increase of excess noise for device with a full absorber coverage, which seems to be related to the chosen absorber coupling scheme with the large central stem, limiting the resolution in high-fill-factor designs to 4 eV. Specific changes planned are, as noted earlier, 1) devising an absorber coupling interface with the TES that minimizes impact on TES parameters and bias current flow, 2) improving the thermal conductance of the TES (changing TES thickness from 15/40 nm Ti/Au to about 20/100 nm Ti/Au) to reduce internal thermal-fluctuation noise and to increase of the critical current (which decreases β_I), 3) reducing the pixel bias power by reducing G to the bath, and 4) incorporating α_I tuning structures on the TES to enable tuning it to the design value of 100, and potentially also suppressing excess noise.

The crosstalk levels achieved in SRON arrays is about a factor of two lower than in GSFC arrays. Heat sinking in the SRON design is simplified by the back-etch process, which etches smooth-walled slots in <111> silicon. These smooth walls promote the growth of a high quality metal heat sinking layer, which then can provide a continuous thermal conduit from the interior of the array to the frame. It should be possible to incorporate this back-etch design, or one based on it, into the GSFC/NIST approach, if needed.

4.2.2 Steps needed for large arrays

Current estimate indicate the heat-sinking scheme is adequate for a full-sized XMS array, so the main effort in scaling up is in implementing microstrip signal leads. Because the slotted back-etch structure requires slots in the nitride membrane between adjacent pixels in the same slot, this array architecture has less room for signal leads than the GSFC/NIST approach.

4.3 Outer array: Hydras

4.3.1 Actual devices

The basic concept of a four-pixel Hydra has been demonstrated with 0.25 mm pixels of the basic GSFC design. Resolution of 6 eV and position discrimination were achieved. More significantly, a robust model has been established that describes the device behavior, and when scaled to the pixel size of the baseline outer array, verifies the suitability of the approach for the XMS reference. Four-pixel Hydras with 0.6 mm pixels have been fabricated (see Fig. 3.3.1.2*)*, and are in the process of being tested.

4.3.2 Steps needed for large arrays

Hydra arrays need the same development for large arrays as do the core array options. They need no additional development. However, optimization of the packing of the outer array with the core array remains to be done. In order to minimize the gap between the inner and outer arrays, the outer array pixels must

extend all the way to the physical edge of the chip that defines the boundary between the inner and outer array.

4.4 Outer array: Large-scale MUX

4.4.1 Actual devices

The concept of coupling multiple pixels into a single SQUID electrically, with different inductances and signal polarity, was successfully tested on four 0.5 mm pixels of the GSFC type. This proof-of-concept achieved better than 9 eV resolution in each of the four pixels.

4.4.2 Steps needed for large arrays

Arrays of independent big pixels need the same development as do the core array options and the Hydra array. They need no additional development.

5 Comparisons

There are two main categories of comparisons that can be made between the reference designs. The first is a comparison of the reference implementations themselves. Given ideal detectors of each type, what differences would there be in their implementation? Just as the studied options share a common operating principle and many common design details, they also largely share a common implementation scheme. Thus, we discuss only the differences in implementation, and what impacts those differences would have on the ease of implementation (development risk) of the detector system and other systems of the instrument. The second category compares the actual performance and the necessary improvements needed for each approach.

The reference pixels for the two core-array options under consideration are similar in many respects. They are both designed for 5 pW of bias power per pixel and similar absorber composition. The only differences between them that have an impact on implementation (where implementation encompasses manufacturing as well as instrumentation) are the TES composition, the back-etch method and resulting structure, and the operating resistance (and the associated choice of biasing shunt resistor). At this point in time, integration of microstrip leads has progressed further with the GSFC approach, but there is no expectation that ease of integration of a microstrip process will distinguish the two approaches. The differences between the outer array options are more substantial, but basically all relate to the number of wires that need to be brought through and off of the array.

Since a trade study of different read-out options is also being conducted, a comparison that accounts for all the possible variations potentially could become quite complex. Fortunately, the basic detector implementation is independent of the multiplexer scheme. Time-division (TDM), code-division (CDM), and frequency-division (FDM) multiplexing each place some components at 50 mK near the detectors and others at the next highest stable temperature stage, so the major features of the design of the focal-plane assembly (see SRON-XMS-RP-2010-008) are largely independent of the read-out scheme. The read-out trade-study (SRON-XMS-RP-2010-007) has shown the simple accommodations (changes in choice of coupling, resistance,

inductance, and capacitance) that can be made to read either detector option with any read-out scheme. Therefore, we will compare the implementations independent of the choice of read out.

Additionally, the comparison of the inner array options is fundamentally different from the outer array options. For the inner array, we have a fixed implementation, 1600 individual pixels, and we are comparing the details of the pixel design and array infrastructure. For the outer array, we are presuming the same pixel materials (the examples are based on the GSFC approach to the inner array, but an equivalent set of references could be based on the SRON designs), and what we are comparing is fundamental performance limits and the wiring and read-out requirements. Thus, in the rest of the section, we will present the inner and outer array comparisons separately, and we will not compare the outer array options using the same metrics as for the inner array.

5.1 Core array comparisons

The following discussion and Table 5.1 compare key derived requirements of the two approaches for the inner array.

For the thermal crosstalk requirement, which is based on noise rather than triggered events, we have considered 8 nearest neighbor pixels with 50 counts/s each, a typical source photon of 1 keV, and crosstalk pulses of similar shape as primary pulses. We calculate the noise impact via $dE_{rms} \sim xE(R\tau_{BW})^{0.5}$, where R is the rate, E is the energy, x is the crosstalk factor, and $\tau_{BW} = 1/f_{eff}$, the high signal-to-noise bandwidth portion of the TES bandwidth. We solve for the value of x required to get dE_{FWHM} <0.3 eV. To convert this to the crosstalk level without the effects of electrothermal feedback (and thus to indicate the needed conductance away from a pixel), we multiply by $(1+L_0)$. In the current GSFC devices, thermal crosstalk is about a factor of 2 too high (8×10^{-4}) for pixels that share a common edge (crosstalk from diagonal neighbors is already at 4×10^{-4}), but planned improvements to the backside heatsinking are expected to reduce it by at least a factor of 2. Using the same formula for the SRON device the crosstalk level limit equals $4.6\ 10^{-4}$, while the measured crosstalk level equals 3-4 10^{-4} for the nearest neighbors (horizontal and vertical) and 6×10^{-5} for the next nearest neighbors (diagonal). So the SRON design meets the requirement with margin. It is interesting to note that the nearest-neighbor crosstalk in the SRON devices is lower than that in the GSFC devices by a factor similar to the ratios of their $(1+L_0)$. This implies that the two array designs are actually heat sunk to a comparable degree, and the difference in measured cross talk is mostly a result of the higher loop gain in the SRON devices, which results from the lower ratio of shunt resistance to TES resistance.

The higher loop gain affords the SRON devices better stability against fluctuations in the ADR control point, as well. It is important to note that the choice of shunt resistor is still a free parameter, and the higher ratio of device resistance to shunt resistance presumed for the higher-resistance SRON devices could also be implemented on lower-resistance GSFC devices. (The resulting 0.15 mΩ shunt resistance is feasible.) Thus the higher loop gain for the SRON approach is not fundamental. The choice of a lower shunt resistor value, relative to the TES resistance, for a given power dissipated in the TES, also implies a higher power dissipated in the shunt resistor. (In the case of FDM readout, capacitive voltage division is used instead of a shunt resistor.)

The limit on electrical crosstalk cannot be set without knowledge of the electrically coupled pulse shape, which if inductively coupled, is a high-pass-filtered version of the thermal pulse. For a placeholder for both designs, we've set it at roughly twice the thermal crosstalk requirement.

In preliminary experiments, the measured magnetic sensitivity of the current SRON pixels is considerably smaller (≈ 25x) than for the GSFC pixels, although more work is needed to determine whether the reason for the apparent difference is fundamental, geometrical, or environmental.

For more details on the terms in the derived parameters table, consult the noise budget table and discussions, e.g. IXO-TN-001141.

Table 5.1 Derived requirements

Derived parameters	Inner GSFC	Inner SRON
Thermal cross talk limit	4.3×10^{-4}	4.6×10^{-4}
Equivalent thermal cross talk without ETF	3.1×10^{-3}	7.7×10^{-3}
Electrical cross talk	1×10^{-3}	1×10^{-3}
Thermal stability of bath for 0.4 eV FWHM contribution	1 uK RMS + 4 uK drift	2.5 uK rms + 8 uK drift
Sensitivity to chaging magnetic fields	140 pT drift	3.4 nT drift
Sensitivity for optimal bias conditions (width of good bias region in terms of % R_n)	3 - 5%	5 – 10%
Wires required for read-out (defines # of interconnections)	3200	3200
Tightest wiring pitch required, presuming microstrips	10 um	5 um

The implementation differences follow directly from Table 5.3. The GSFC approach needs to be heat sunk about a factor of 2 better than the SRON approach, and it may need to impose stricter limits on the magnetic-field environment. There are no fundamental differences in their mechanical integration into the focal plane assembly.

There are a number of relevant production issues, as shown if Table 5.4. The biggest difference between the approaches lies in the very different diffusivity of Ti in Au compared with Mo in Au, which makes Ti/Au bilayers vulnerable to exposure to temperatures commonly experienced in standard microlithographic processing.

At this stage in development, there are not expected any differences in sensitivities to the launch or space environment (radiation or vibration), or to thermal cycles (between room temperature and operating temperature).

Table 5.4 Production issues

Production issues	Inner GSFC	Inner SRON
Sensitivity for thermal cycles and high temperatures	Mo/Au non-reactive and immiscible. Main effect of annealing is increase in RRR and few mK suppression in T_c (for anneal at 150°C, for an hour)	Significant T_c shift for short anneals at modest temperatures (e.g. 30 mK shift for 6 minutes at 170 °C)
Robustness (mechanical handling)	Robust to handling	Robust to handling
Ease of heat sinking	Adding Cu to sidewalls effectively requires careful cleaning of DRIE residue and depositions over four angles	Adding Cu sidewalls relatively straightforward
Production reproducibility (yield)	Insufficient resources invested thus far to assess ultimate production yield	Insufficient resources invested thus far to assess ultimate production yield
Wiring pitch	Easy 10 um pitch	Tighter 5 um pitch

5.2 Outer array comparisons

Table 5.5 pulls together for comparison the relevant parameters for the outer-array options from Section 3.3. Because the Hydra option has so little margin against meeting the resolution requirement, it is forced into a lower-T_c design, which then increases its sensitivity to base-temperature fluctuations. Crosstalk has not been rigorously addressed for the outer array options yet. Determination of crosstalk noise is complicated in the Hydra and shared-SQUID options, which have 4 different pulse shapes and 4 different optimal filter templates. However, the lower T_c of the Hydra option, and the higher G required to meet the minimum count-rate requirement for the outer array, indicate that the Hydra option will be the most sensitive to thermal perturbations on the frame of the array. It is clear that the only advantage of the Hydra approach is the lower number of wires required to read it out. Given the complexity of the focal-plane assembly, however, this is a significant advantage that outweighs all its disadvantages at this point in time.

Table 5.5 Comparison of outer array parameters and sensitivities

Parameter	Hydra (4 absorbers)	Single pixels – large scale MUX	Single pixels – 4 per input SQUID
T_c	75 mK	90 mK	90 mK
dE from 1 uK RMS + 4 uK drift	1 eV	0.4 eV	0.4 eV
Wires required for read-out	1052	4608	4608
Total power dissipated in outer array	18 nW	11.5 nW	45.8 nW
dE (prior to adding noise budget terms)	9.5 eV	4.6 eV	8.4 eV
Per-pixel rate for 80% live time	2/s	10/s	5/s

6 Pros and Cons

Since we are not comparing fundamentally different technologies, but different design choices within the same technology, a clear-cut comparison is not possible for the core array. (The outer array candidates, on the other hand, do present distinct choices in optimization.) Therefore, both approaches can legitimately claim the ability to meet the requirements on all fronts. The two reference designs differ most substantially in terms of their heritage. The GSFC approach is a minor perturbation on an existing and well characterized pixel design, with the main development lying in putting together the large array. The SRON/ISAS reference design requires a redesign of both the TES (thickness and α tuning) and the interface between the absorber and TES. Thus, there is much more uncertainty in that approach. The GSFC approach has a solid track record, with over 40 separate studied pixels of the same basic design achieving better than 4 eV resolution at 6 keV (and most better than 3 eV). (The range was widened to 4 eV to include pixels that were only viewed via non-optimized MUXing.)

Technologically, the main differences between the approaches are the operating resistance of the TES and the array support structure for the membranes (dry-etched wells vs. wet-etched slots).

As recognized at the start of this trade study, the best detector may end up taking the best aspects from a range of designs currently or soon-to-be in operation.

CORE	GSFC/NIST type	SRON/ISAS type
Pro	• Reference design based on well-established and proven existing design, with absorber size and array scale the only changes. • Low resistance design is good for stability and negligible internal thermal fluctuation noise.	• Measured thermal crosstalk is about a factor of two lower than in GSFC devices. • Higher resistance design permits use of higher resistance shunt and is less vulnerable to stray resistances in the bias circuit.
Con	• Lower resistance design more vulnerable to stray resistance in the bias circuit. • So far, have not demonstrated low enough thermal cross talk.	• Reference design is based on projected improvements that have not yet been verified • Higher resistance design more prone to thermal fluctuation noise.

OUTER	Hydra	Big single pixels
Pro	• Lower wire count simplifies the design of focal plane assembly.	• This option offers the highest spectral resolution and faster count rates.
Con	• Spectral resolution is degraded, and is intrinsically variable across the pixels of a Hydra • Pulse processing more complex.	• Many connections to the chip needed, greatly complicating packaging. • In order to keep the room-temperature electronics from growing, larger scale multiplexing or SQUID sharing (in TDM) is required, leading to differences between the front-end readouts for the inner and outer arrays.

III. Recommendations

Because we need to present a design with the highest TRL, the reference design based on the array type used for GSFC/NIST 2x8 demo is recommended as the baseline. We may want to identify aspects of the SRON and ISAS arrays for consideration for possible incorporation into the baseline, as well endorsing their independent parallel development. Other improvements to the GSFC/NIST baseline should be pursued in order to increase margin (such as increases to the critical current).

While the independent-pixel options are attractive because of their much greater margins with respect to the requirements, the large number of signal contacts greatly complicates the design of the focal-plan assembly. In the present activities, FPA designs with more pixel contacts have not been developed. In order to present as complete an implementation scheme as possible, we recommend selecting as the baseline an outer array scheme compatible with the most developed FPA design. Therefore, we recommend the four-pixel Hydra scheme as the baseline. Future work should be done to assess the feasibility of contacting independent pixels in the outer array. The science case for the outer array requirements should also be reassessed, as a solid 10 eV requirement could shift the balance of this trade study.