Workmanship Challenges for NASA Mission Hardware

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NASA Workmanship Standards Program
June 23, 2010

Overview

(1) Failure to apply NASA Workmanship Standards to contracts
J-STD-001ES Adoption
Non-Standard Processes
The Packaging Design Dilemma

(2) Electrostatic Discharge Charge Device Model (CDM)

(3) Water Soluble Flux (WSF)

(4) High Density Interconnect PCB's

(5) Column Grid Area Array Interconnect

(6) Pb-free

Failure to apply NASA Workmanship Standards to contracts

J-STD-001ES Adoption

Non-Standard Processes

The Packaging Design Dilemma

NASA Workmanship Standards

Required for all Programs, Projects, Contracts, and Subcontracts per NPD 8730.5 NASA Quality Assurance Program Policy

NASA-STD-8739.1, Workmanship Standard for Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies.

NASA-STD-8739.2, Workmanship Standard for Surface Mount Technology.

NASA-STD-8739.3, Soldered Electrical Connections.

NASA-STD-8739.4, Crimping, Interconnecting Cables, Harnesses, and Wiring.

NASA-STD-8739.5, Fiber Optics Terminations, Cable Assemblies, and Installation.

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).

These Standards contain our best known methods for avoiding past assembly problems and defects. These best practices may not be available if suppliers are used who are not compliant with them. Compliance includes having certified operators and inspectors.

Examples of Problems from lack of Requirements Flow-down

Cleanliness testing of finished boards not performed

Demoisturizing boards prior to soldering and conformal coating not performed

Test specimens (aka “witness sample”) not produced for staking material

Crimp pull testing not performed or alternate acceptance values used

Incorrect ESD flooring measurement methods used

Requirements for Non-Standard Processes not addressed.

Finding these problems during build of mission hardware is often too late *(i)* contractually and *(ii)* in the mission life-cycle, to resolve without residual risk.

How to establish known-good suppliers for Workmanship?

When/how to develop up-and-coming suppliers who seek to serve NASA niche? *Without putting mission hardware/schedule at risk*

Adoption of J-STD-001ES

NASA Workmanship is mandated to adopt industry voluntary consensus standards where practicable.

NASA-STD-8739.2, Workmanship Standard for Surface Mount Technology.

NASA-STD-8739.3, Soldered Electrical Connections.

Will be replaced by J-STD-001ES, Space Applications Electronic Hardware Addendum to J-STD-001E Requirements for Soldered Electrical and Electronic Assemblies

Workmanship best practices may not be available if suppliers are used who are not compliant with J-STD001xS. Compliance includes having certified operators and inspectors.

J-STD-001 Class 3 is not an acceptable substitute!!!

See http://nepp.nasa.gov/index.cfm/5553

Presentation on Transition to J-STD-001DS

(scroll down to the last item on the page)

Examples of Changes/Challenges with the use of VCS's/J-STD-001xS

NASA does not "own" J-STD-001xS. NASA cannot control inclusion or exclusion of any particular requirement. Space Committee considers military and commercial space requirements as well as those of NASA.

Change-over will drive "sudden" need for retraining/certifying of personnel outside of the normal two-year cycle. This may be have a schedule/cost impact across the industry.

NASA does not drive pace of technology insertion and may not be able to provide technology knowledge fast enough to develop appropriate assurance requirements for low-risk missions.

Though DoD "adopted" J-STD-001 Class 3 in 2001 but has not required it widely on contracts. DoD suppliers free to adopt "cafeteria plan" compliance with requirements. NASA adoption will challenge this.

Non-Standard Processes

NASA-STD-8739.1, para 4.1.3
NASA-STD-8739.2, para 4.1.3
NASA-STD-8739.3, para 4.1.3
NASA-STD-8739.4, para 4.1.3
NASA-STD-8739.5, para 4.1.3

“Nonstandard Processes, Materials, or Parts. When the supplier intends to use processes, materials, or parts not covered by this standard, the supplier shall document the details of fabrication and inspection, including acceptance and rejection criteria, and provide the documentation along with appropriate test data to the procuring NASA Center for approval prior to use (*Requirement).”*

What NASA Means

What Suppliers Provide

"…processes, materials, or parts not covered by this standard…and provide the documentation…to the procuring NASA Center for approval prior to use…"

Specialty High Temp Solder
Pb-free Solder
Water Soluble Flux
Ball Grid Array, Micro BGA
Column Grid Array
Stacked Memory
Chip-on-Board
Staked stacked parts
Custom Cryogenic Cable Harnesses

Notice provided for approval during design process.

Declarations in advance are not being received.

Design not being done by Workmanship personnel.

Design and assembly may be done by two different suppliers.

(See: "The Packaging Design Dilemma" later in this presentation)

What NASA Means

What Suppliers Provide

"…the supplier shall document the details of fabrication and inspection, including acceptance and rejection criteria…"

Evidence of an engineered process designed and optimized for the technology

Repeatable and controlled methods used to monitor quality.

Accept/reject quality criteria

Swap new technology into old process

Assume old quality methods work for new technology.

Use accept/reject criteria for old technology to test/inspect new technology.

Point to NASA Workmanship Standards quality methods and criteria to show acceptability of new technology.

What NASA Means

What Suppliers Provide

"…and provide the documentation along with appropriate test data to the procuring NASA Center for approval prior to use…"

Evidence that the intended configuration (materials, geometries, quality level) is sufficiently reliable for the intended NASA mission. Preferably life test data.

- Design bounds final product performance.
- Engineered process achieves design and bounds quality variations.
- Quality methods bound quality escapes.

Raw material qualification data

Heritage statements

Successful completion of NASA Workmanship Standards tests (regardless of their applicability)

Claims that it is an in-house "standard process"

The Packaging "Design" Dilemma

- Workmanship Standards are implemented by operators and inspectors on a build-to-print basis.
- Quality organizations in NASA and NASA's supply chain presume that Workmanship is "taken care of" by the operators and inspectors. Workmanship training is not required for packaging designers and process engineers.
- NASA Workmanship Standards contain design and process engineering requirements which are not controlled by operators and inspectors.
- IPC Standards will not contain design requirements.
- Who will capture and own Workmanship design and processes requirements? Center-level documents?

Electrostatic Discharge

Charge Device Model

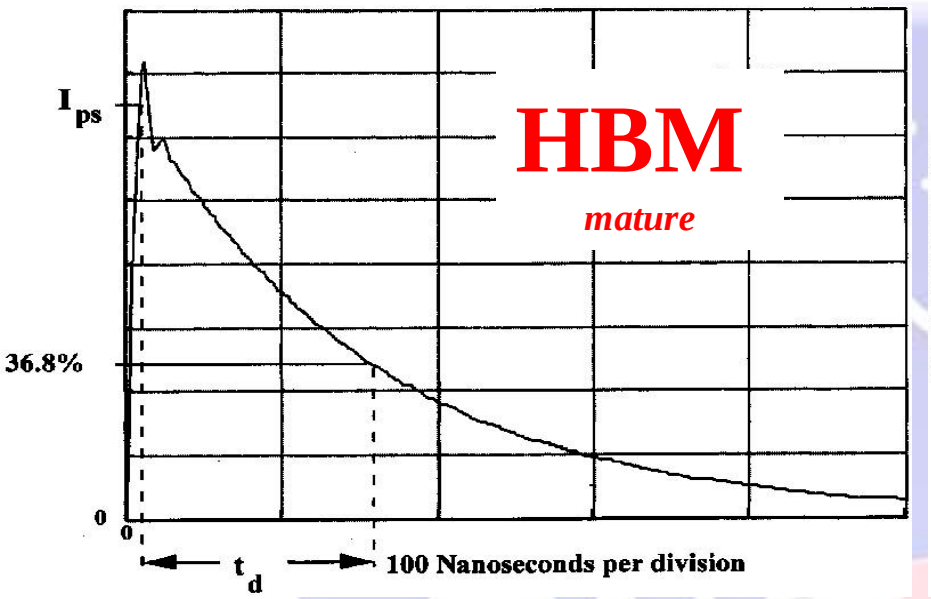
Overview

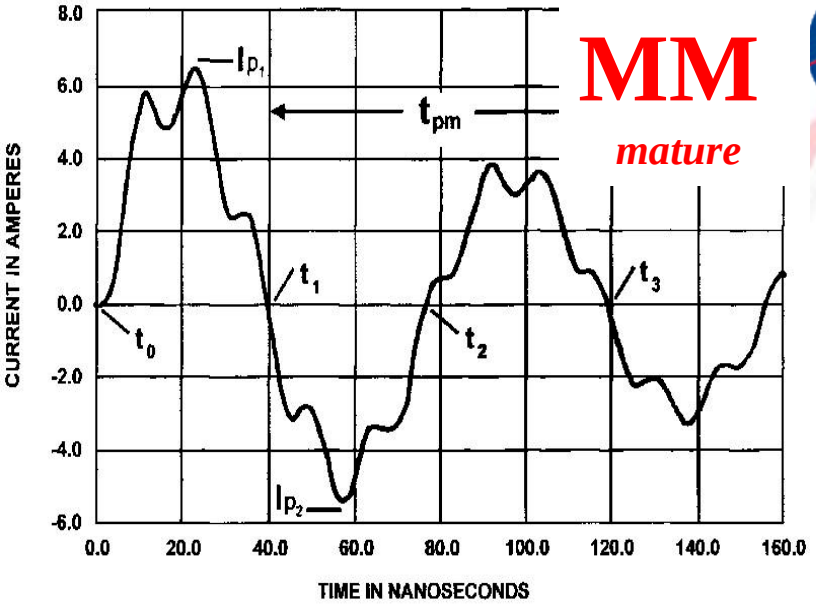
(1) ESD Models Provide a way to characterize the sensitivity of components to ESD

(2) The different ESD models simulate the different environments experienced by electronic components during the manufacturing process.

(3) Parts and assemblies may be exposed to more than one type of ESD event over the manufacturing and test life cycle.

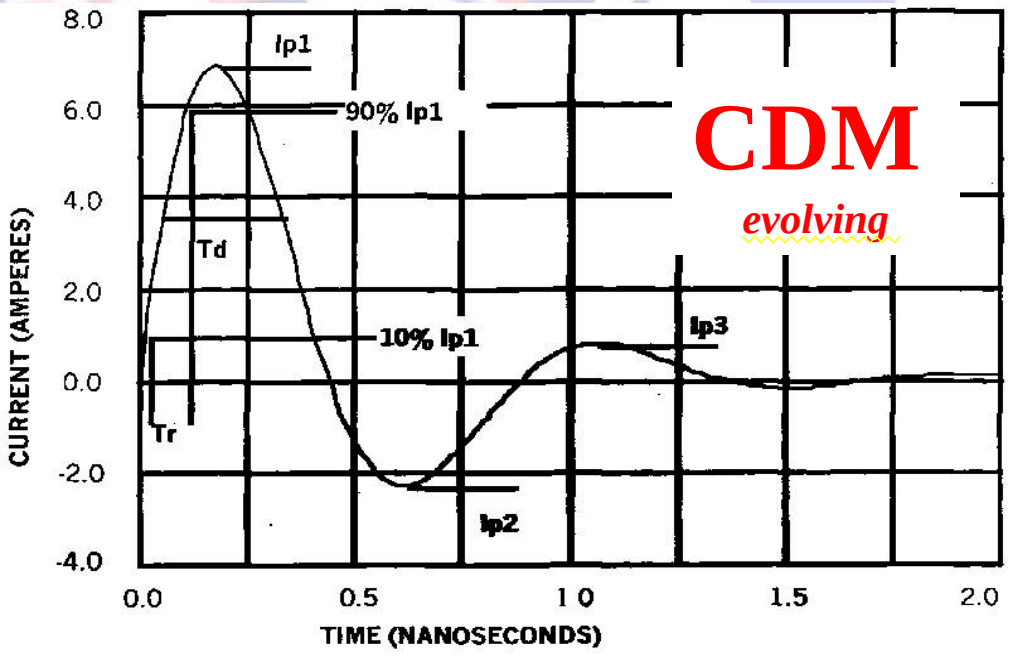
Courtesy ESP Seattle Inc.

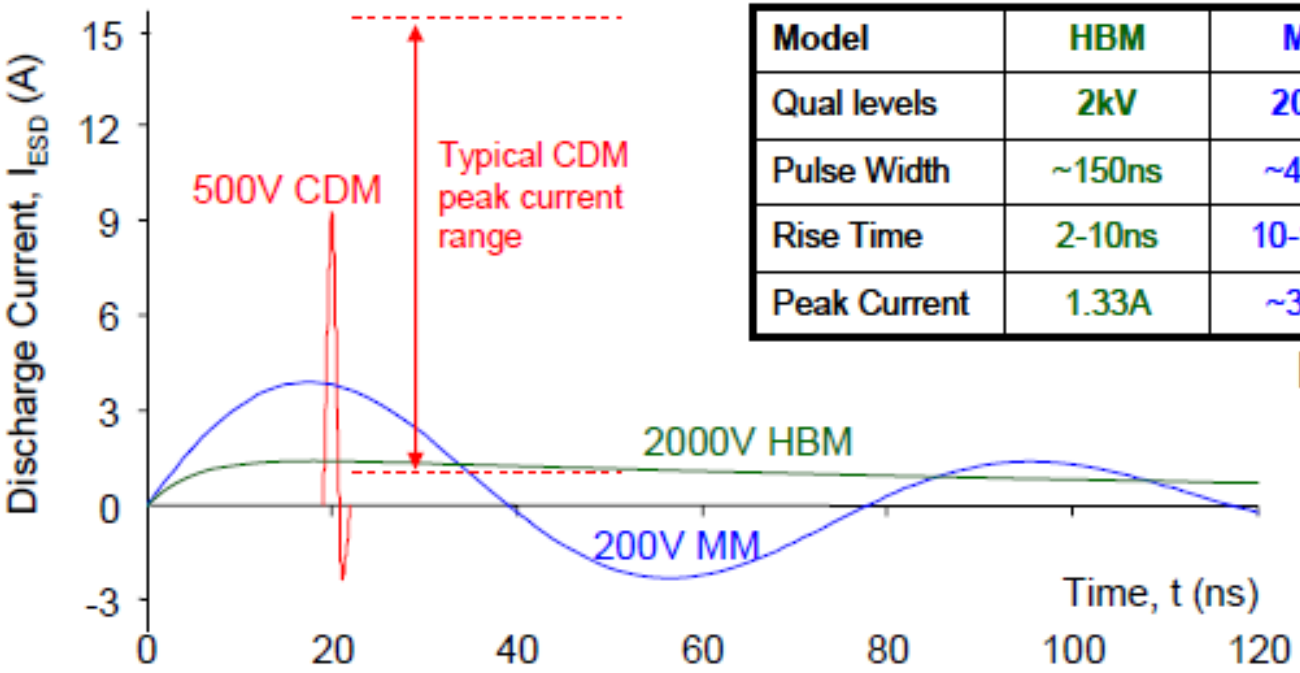




HBM = Human Body Model
MM = Machine Model
CDM = Charged Device Model

Voltage discharged through RC or RCL network creates different total energy experienced by the device.



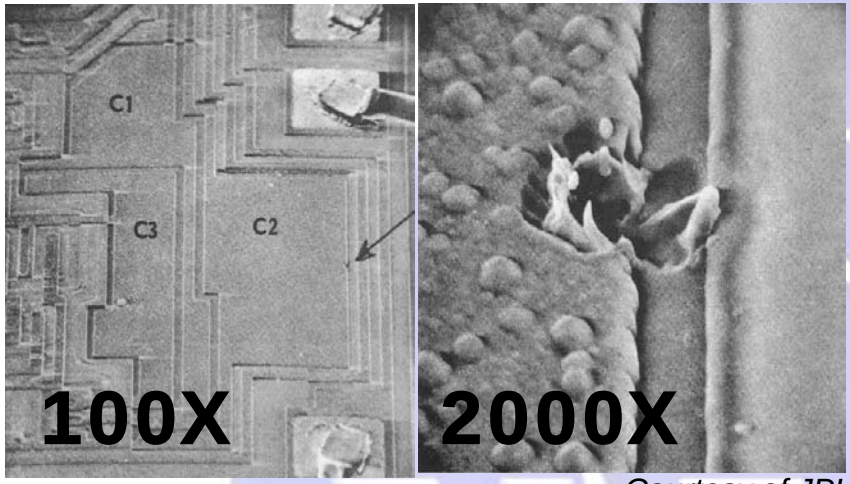


Model	HBM	MM	CDM
Qual levels	2kV	200V	500V
Pulse Width	~150ns	~40ns	~1ns
Rise Time	2-10ns	10-15ns	100-500ps
Peak Current	1.33A	~3.6A	1-16A

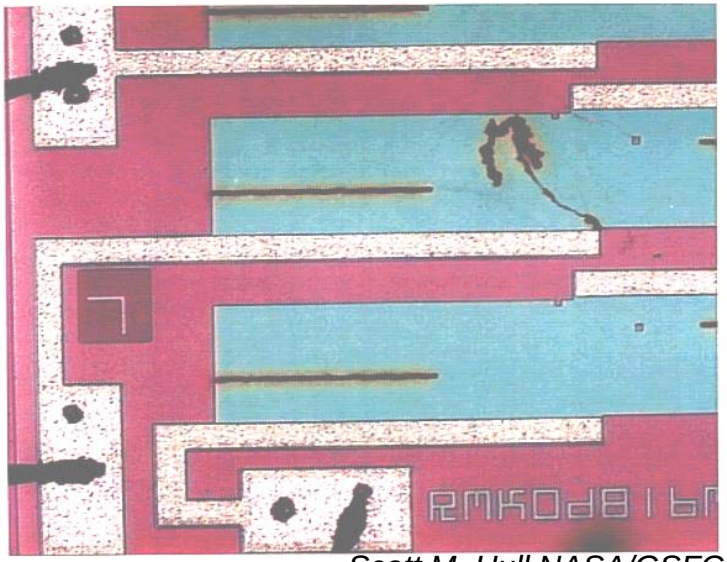
[Gieser] (modified)

Figure 4: Comparison of current waveforms for CDM, MM, and HBM ESD events.

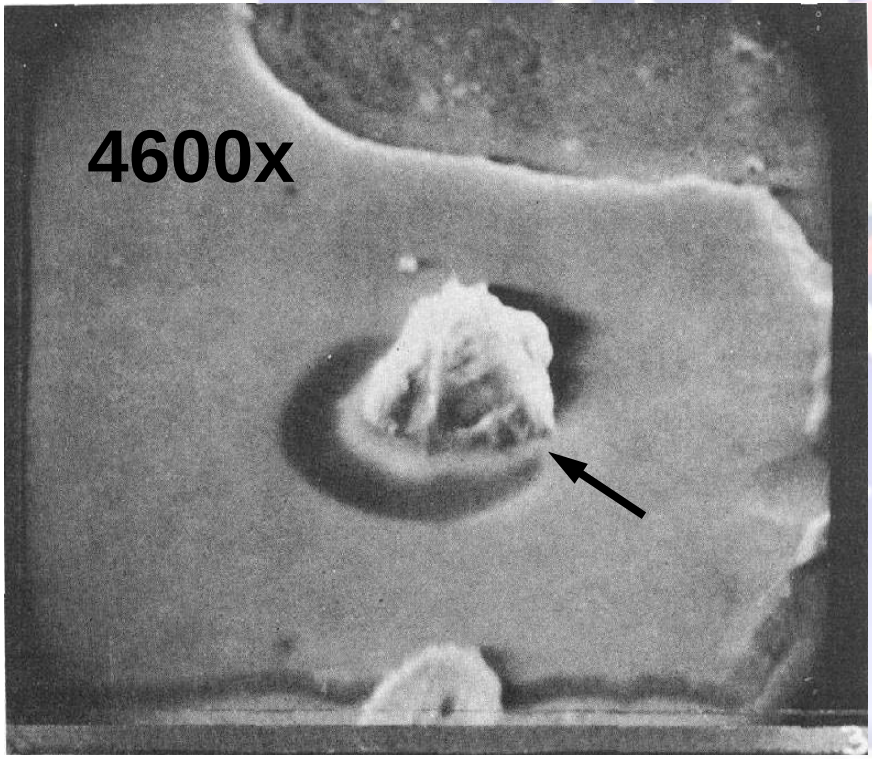
White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Industry Council on ESD Target Levels, March 2009



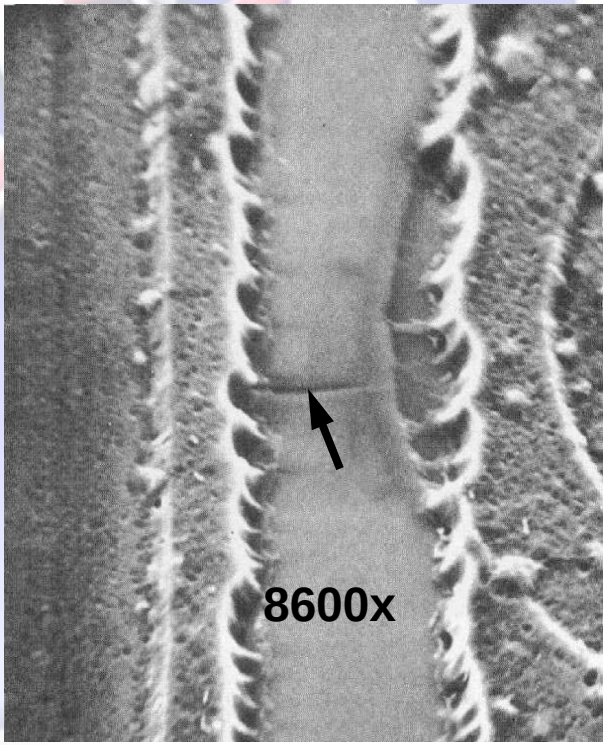
Courtesy of JPL



Scott M. Hull NASA/GSFC



Courtesy of JPL



Courtesy of JPL

HBM safety methods have brought HBM & MM failures down to ~10% of failures encountered industry-wide.

Role of CDM in failure count is now majority (~90%)

Examples of Sources of Threats (charge or discharge path)	HBM	MM	CDM
Operator	√		
Work bench	√		
Pick and Place Machine		√	
Automatic Test Equipment		√	√
Device package charging/discharging			√
Mate/De-mate of harnesses			√
RF Signals (including cell phone signals)			√

CDM Challenges

- Opportunities to use on-chip ESD protection reduced in high speed designs
- Reduction in conductor widths on-chip result in higher current densities and thermal stress
- Package capacitances in high pin-count designs increase peak current during CDM ESD event.
- Ionizers work on an HBM time scale and are not effective for mitigating rapid-pulse charging events

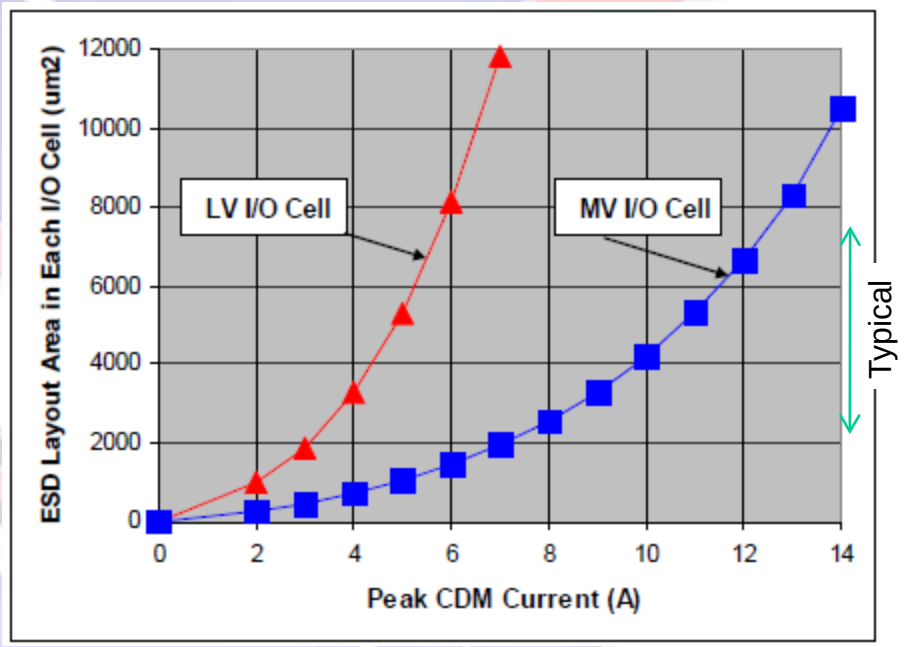
Suppliers have been working to a 500V qualification level for CDM (peak current @ 16A).

Industry position developing to reduce qualification level to 250V (peak current @ 7A). ← *increasing baseline risk*

CDM Challenges

Gate damage susceptibility is scaling with feature size.

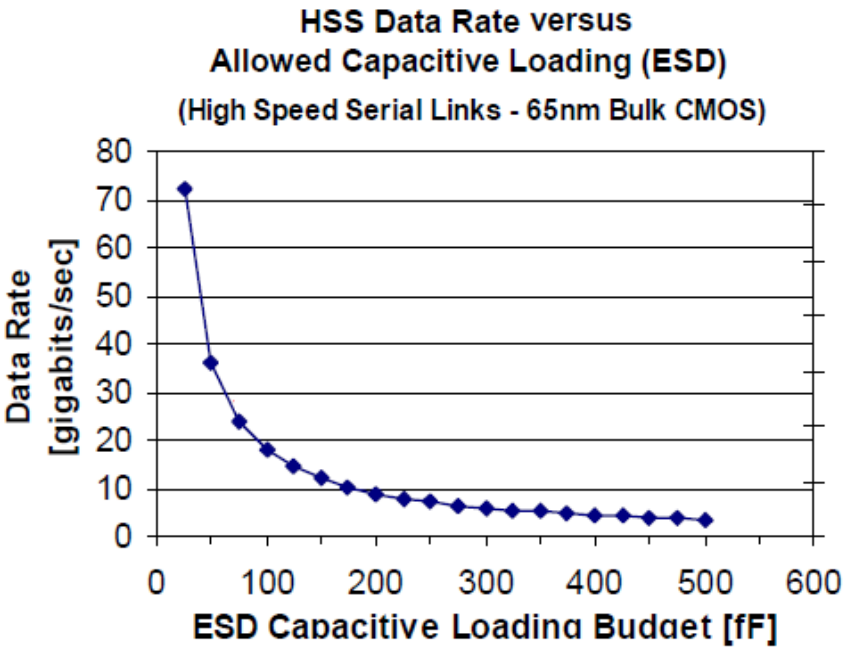
The area needed for on-chip ESD protection against CDM events @ 16A has become impractical.

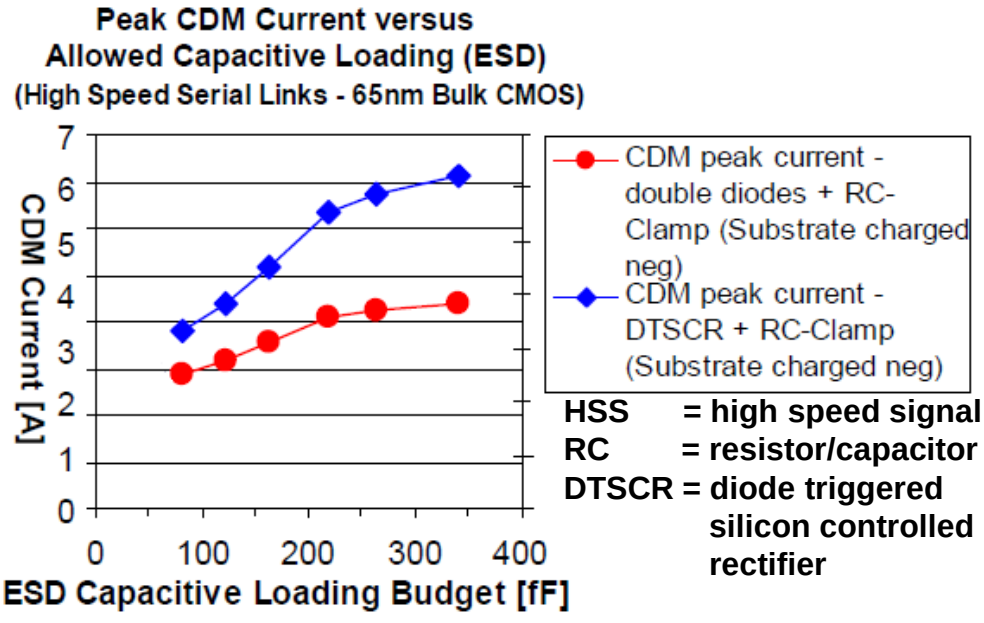


Both are 45 nm technology, LV is Vdd=1.1V, MV is Vdd=1.8V

Source: White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Industry Council on ESD Target Levels, March 2009

CDM Challenges





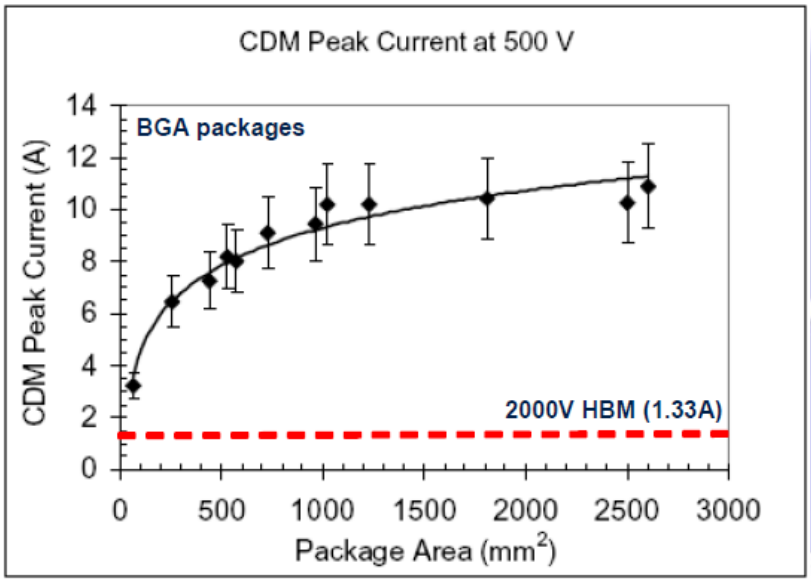
HSS = high speed signal
RC = resistor/capacitor
DTSCR = diode triggered silicon controlled rectifier

Capacitance must be reduced for high speed operation.

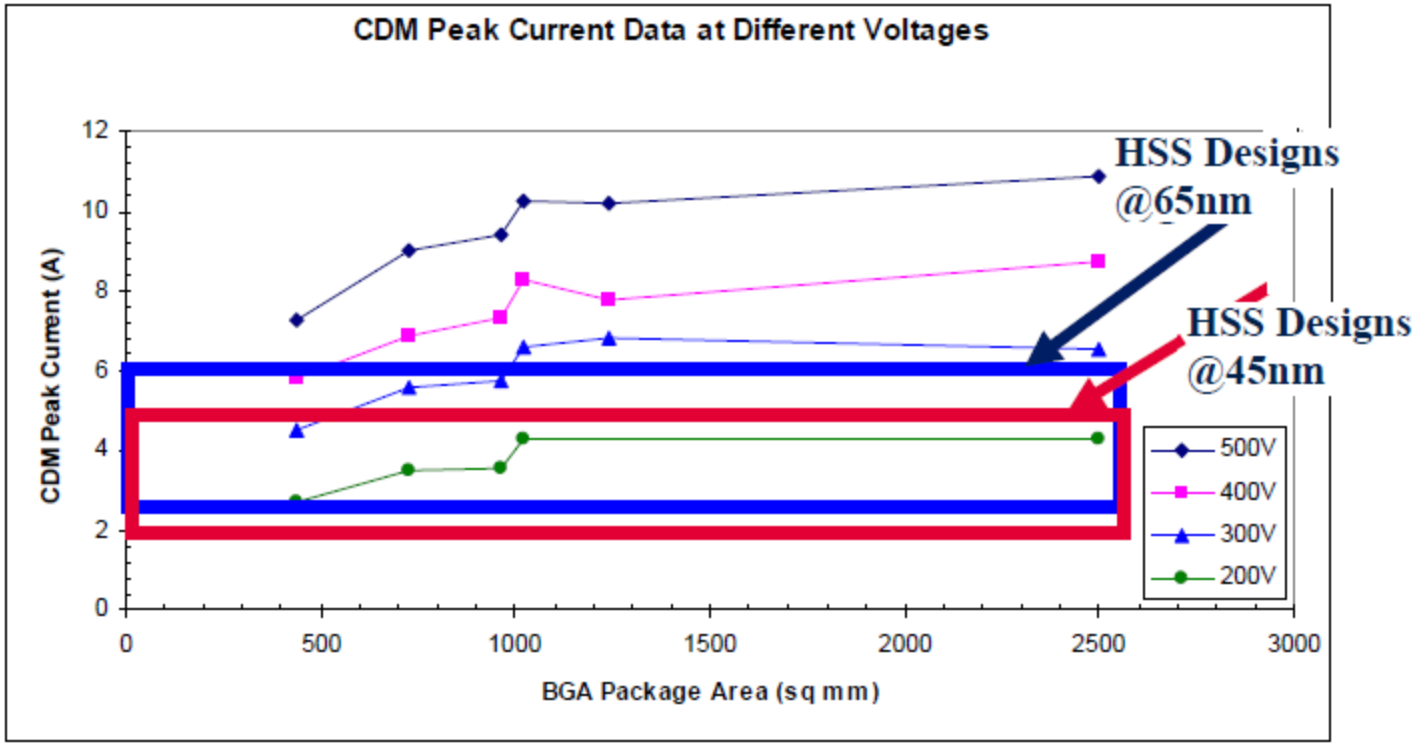
The remaining budget for ESDS circuitry scales downward providing lower levels of ESD protection.

Source: White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Industry Council on ESD Target Levels, March 2009

CDM Challenges



Package size causes an increase in CDM event current. Package capacitance charges triboelectrically or inductively and then discharges rapidly into the die during the CDM event.



CDM

- Devices will be less robust to CDM event in the future and "old" practices may not be sufficient.
- Expert help will be needed to work through CDM safety solutions. Complex and evolving event model.
- CDM safety measures may include new board materials, design rules, discharge steps during test, protection from stray RF
- Technology drivers in high-speed, high pin-count devices make them more susceptible to CDM events.
  - ✓ Suppliers will <u>not</u> "ESD harden" these devices
  - ✓ HBM methods will not protect these devices

Water Soluble Flux

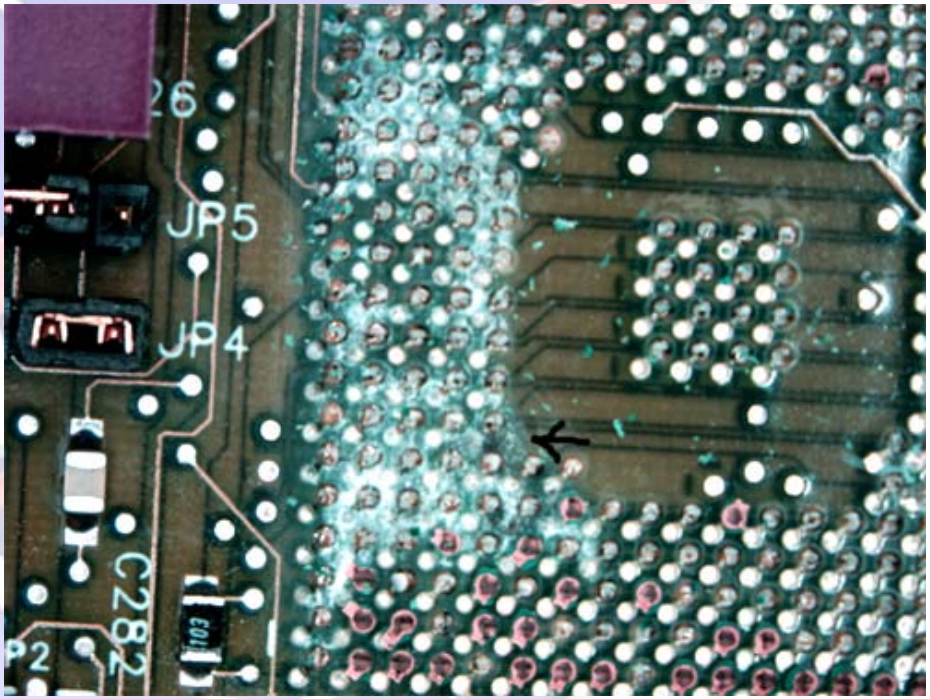
- WSF entering mission hardware due to increased use in the commercial sector ("It's our standard process.")
- Increased use in the commercial sector is to avoid problems finding and using solvents needed to clean rosin flux.
- Active ingredient in WSF is organic or inorganic acid however they are pH-neutral. Halides often added to increase activity level.
- NASA Workmanship Standards cleanliness test is not applicable to pH-neutral contaminants. Designed to find halides. *(See: "Non-standard Processes")*
- No known screening test for pH-neutral flux contaminants. Tests are QCI type, typically used by process engineers not operators; requires new equipment, knowledge. *(See: "The Packaging Design Dilemma")*

- WSF contamination (unreacted and uncleaned flux, uncleaned halides) has been root cause of failures in commercial production.

- Failures are being encountered in commercial uses indicating need to understand process factors better. Rosin flux may have provided more “forgiving” system (wider quality window).

- Cleanliness risk mitigation methods are not well understood and therefore not standardized (and not tuned for NASA missions).

- Failure modes are electrical shorts through dendrites, metallic salts, electrolyte



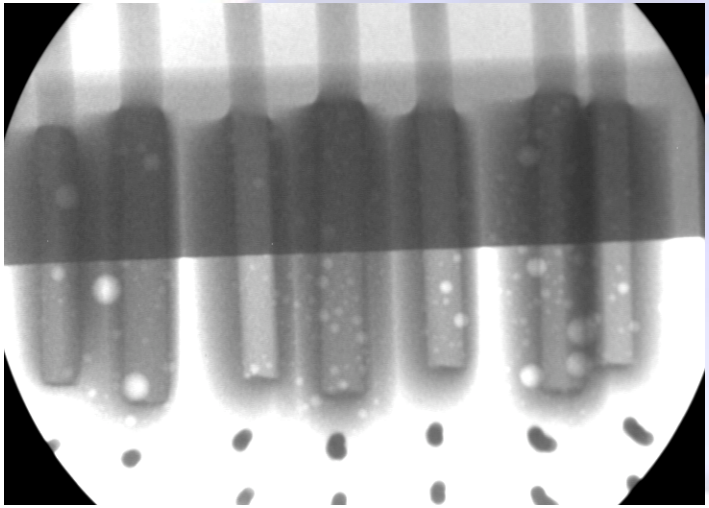
Courtesy: Foresite

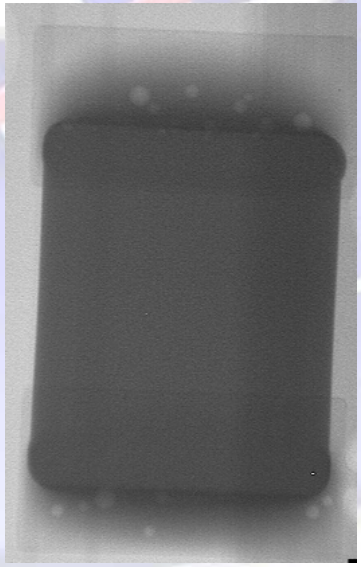
Metallic salt deposits may be permanent causing entire assemblies to be scrapped.

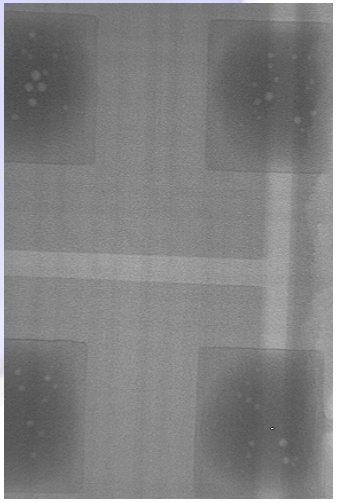
•At GSFC one project was using WSF in 2008. In 2010 there are now five. Not being used at other NASA Centers (yet?)

- Five out of five users have had solder joint voiding to level not “normal” for a rosin process.

- Workmanship does not have a clear policy on acceptable levels of voiding. Acceptability is strongly tied to thermal cycling environment. IPC points to “engineering” to referee the acceptability of voids.



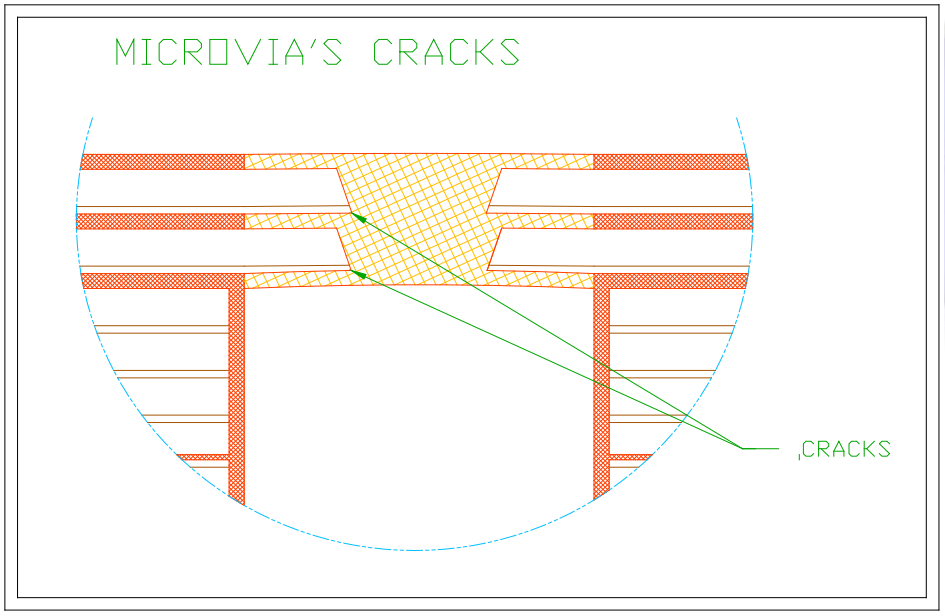




High Density Interconnect

Printed Circuit Boards

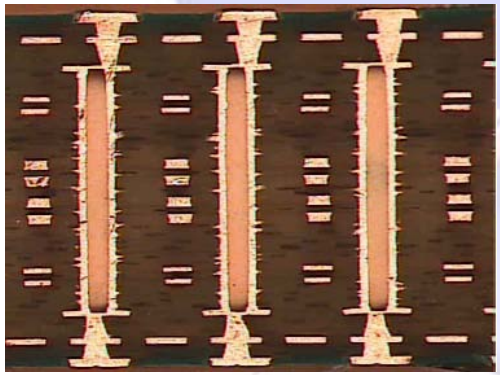
- In 2008 a GSFC project encountered a printed wiring assembly with a PCB that was failing batch-based quality inspections.
- Extensive engineering and quality attention to this board found that:
  - HDI features such as buried vias, micro-vias, and a high layer count made it very complex to manufacturer
  - The system supplier did not have a PCB supplier who could identify and control the critical processing parameters



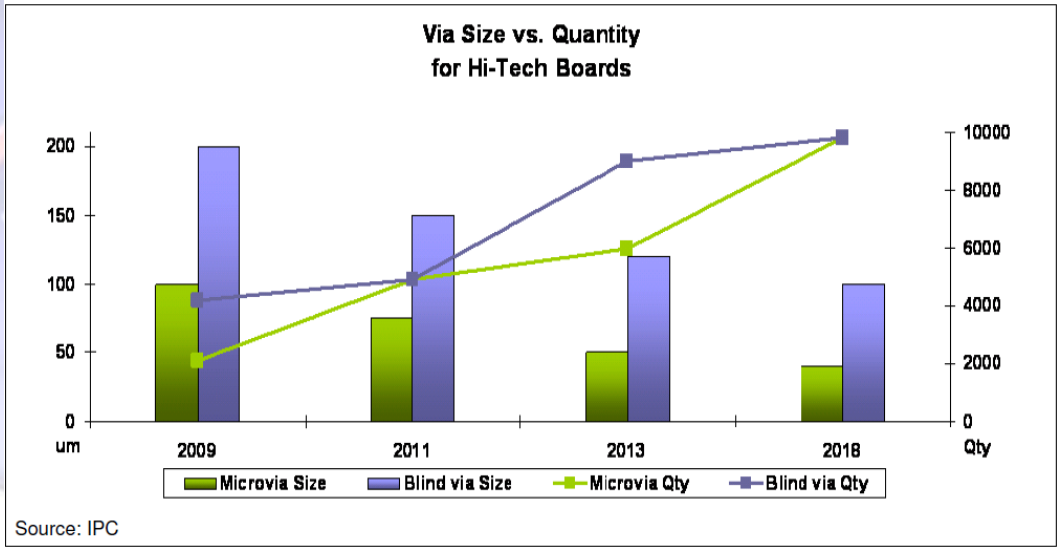
In December 2009 the IPC hosted a government-industry symposium on the concerns of the US PCB industry.

A major concern is a loss of the ability of US firms to leverage off of high-volume commercial business to fund state-of-the-art (SoA) technology knowledge (process and quality R&D) for their low-volume customers (Mil and Space).

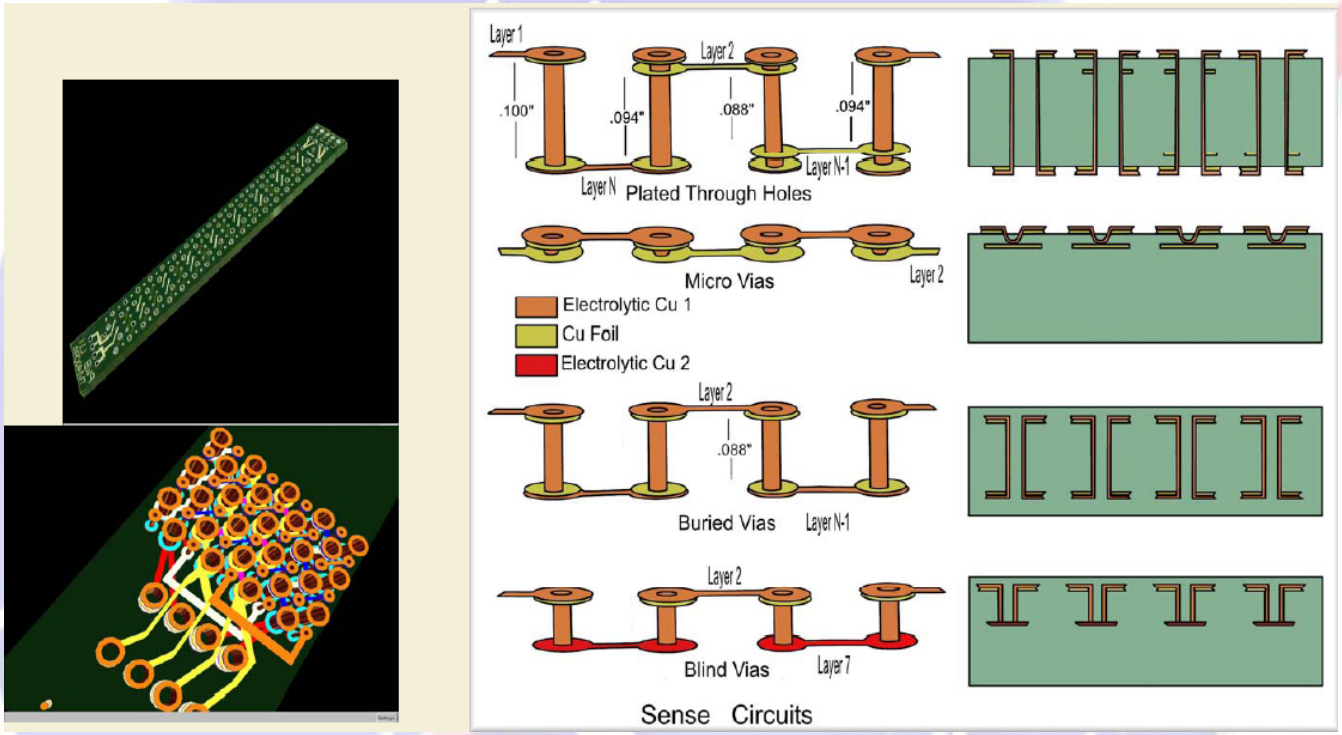
Though device suppliers require SoA features, PCB manufacturing capability is lagging and showing up as quality defects.



Courtesy: Coretec



Interconnect Stress Testing (IST) should be investigated for standard use by NASA in addition to coupon analysis.



Courtesy: PWB Interconnect Solutions Inc.

Resistive heating and sense circuits built into PCB coupons can be used to rapidly perform thermal cycling QCI testing.

Developer has demonstrated good correlation between field failures and IST test failures.

Area Array Interconnect

Column Grid Array

- Area Array Interconnect knowledge has been developed for many years by NEPP, IPC, CALCE, CAVE, others.
- Strong dependency between reliability goals and processing parameters slowed progress on standardizing quality rules.
- IPC 7095, Design and Assembly Process Implementation for BGAs, October 2004:
  - Is a guideline document
  - Does not directly address CGA's
- IPC J-STD-001ES now addresses BGAs and CGAs:
  7.5.14 Surface Mount Area Array Packages
- PCB design rules not addressed by J-STD-001ES. Pursuing PCB placement rules on mirroring, rework keep-out zone, and pad design for inclusion in IPC-2222, Sectional Design Standard for Rigid Organic Printed Circuit Boards.

Column Grid Array

IPC J-STD-001ES CGA Rules:

- No missing columns (except corners which may be intentionally missing)
- Minimum electrical clearance limits are not violated
- Full solder fillet for viewable columns. Use Xray for those which cannot be viewed.

Additional Rules used by GSFC (Center Level):

- Process capability audit required
- Lead co-planarity
- Board flatness
- Mechanical analysis of board design for thermal and mechanical robustness
- No part mirroring
- No solder-mask defined pads
- No shared vias
- Corner staking is required
- Applicable NASA Workmanship Standard requirements (8739.2)
- Verification of sufficient solder volume
- Visual verification of part placement
- Qualification testing of representative units (to show line capability)

Pb-Free

-RoHS Movement in Europe in mid 1990's

-solderable surfaces and solder itself must be Pb-free

-Worldwide suppliers offer pure tin as alternative

-Researchers and users are reminded of the tin whisker hazard

-Industry searches for new solder formulations

$SnAg_{3.0}Cu_{0.5}$
$SnAg_{3.5}Cu_{0.7}$
$SnAg_{3.5}Cu_{0.9}$
$SnAg_{3.8}Cu_{0.7}$
$SnAg_{3.9}Cu_{0.6}$

$SnAg_{3.8}Cu_{0.7}Sb_{0.25}$
$SnAg_{3.8}Cu_{0.7}Sb_{0.25}$
$Sn_{3.5}Ag_{0.74}Cu_{0.21}Zn$
$Sn_{3.5}Ag_{0.85}Cu0_{0.1}Mn$
$SnCu_{0.7}$

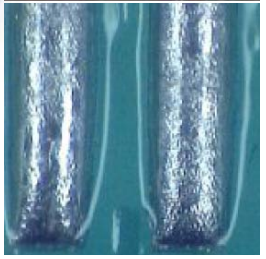
$SnZn_{9}$
$SnZn_{8}Bi_{3}$
$SnAg_{2.5}Cu_{0.8}Sb_{0.5}$
$SnIn_{8.0}Ag_{3.5}Bi_{0.5}$
$SnBi_{57}Ag_{1}$

-New formulations come with known and unknown risks

-Sensitivity to physical shock
-Some test methods do not "translate"
-Higher processing temperatures can affect boards and parts
-Assemblies may mix solders
-Logistics may not be set up to identify Pb-free materials
-Solder joints have "dull" appearance

a.

b.



a.SnPb solder, b. Pb-free solder, Source: Lead Free Surface Mount Technology, Ian Wilding, Henkel Technologies, 2005

Quality Assurance Requirements Traceability

NPD 8730.2, NASA Parts Policy

Attachment A: Criteria to Mitigate Risks Associated with Lead-Free Solder and Surface Finishes

(paraphrased)

a. Sn-Pb shall be used whenever possible. Use of Pb-free (<3% Pb) may be used by special approval on technical need and risk mitigation.

b. A GEIA-STD-0005-1 Pb-free control plan is required which addresses:

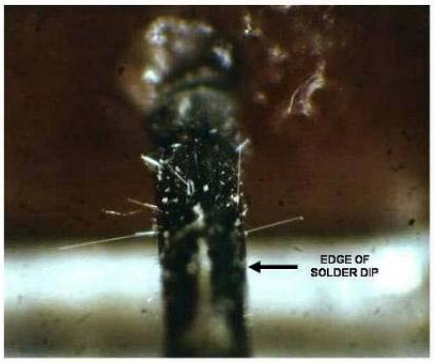
design considerations	*manufacturing process controls*
test & qualification requirements	*quality inspection & screening*
marking & identification	*maintenance & repair*
risk mitigation	*application uniqueness's*

c. GEIA-STD-0005-2 “2C” level whisker risk mitigation. “2B” level allowed in special circumstances and with PCB approval.

d. Use of Pb-free Sn-based solders and surface finishes, in applications below 13.2^{o}C, shall be assessed for the risk of the damaging effects of tin pest formation (allotropic phase transformation of tin).

Quality Assurance Requirements Traceability

J-STD-001DS.1 Joint Industry Standard, Space Applications Electronic Hardware Addendum to J-STD-001D Requirements for Soldered Electrical and Electronic Assemblies



1. Scope is surfaces to be soldered and solder used.

2. The following are specifically prohibited without meeting additional requirements:

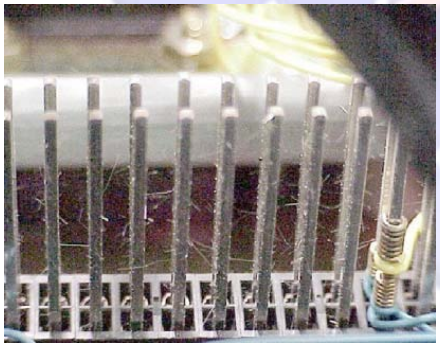
- Pb-free tin platings or metallization on external surfaces of EEE parts, mechanical parts, including on parts inside of modules (e.g. MCM, Relays)

- Pb-free solder alloy except Sn96.2Ag3.7

Quality Assurance Requirements Traceability Cont. J-STD-001DS.1

3. The cases above are allowed only with a USER approved lead-free control plan (LFCP) which accomplishes:
    a. Re-plating or hot solder dip replacement of Pb-free surfaces with SnPb -or-
    b. Minimum of 2 other risk mitigation methods employed

4. LFCP shall ensure functionality of hardware in intended application w/r/solder, platings, soldering processes
    a. Document every incidence of use
    b. Minimum of two mitigation methods
    c. Document special design requirements, processes, testing, inspections, marking, repair



LFCP Template Instructions

Template has same section numbers and headings as GEIA-STD-0005-1.

Green Shading : *short reminder of requirement statement from GEIA-STD-0005-1, removed by author*

Blue font :*fill in information on materials, reliability, configuration management, procedures, etc.*

The instructions assume that the Plan author has access to the information, either through personal knowledge, or through other knowledgeable personnel. ← can "standard" methods be provided ?

[Supplier name] :*fill in the name of the organization responsible for implementing the Lead-free Control Plan*

[LFCP] :*fill in supplier's formal name or doc number*

[Bold Italicized] :*fill in additional or custom information*

Prior to review, remove the 1st section break and all text on pgs i through iv and remainder will be the LFCP.

LFCP Template

1. Cover Page
2. Table of Contents
3. Configuration Management table
4. Forward: 2 examples given, choose one or make your own
5. Purpose and Applicability: fill in LFCP name, fill in supplier name
6. Exclusions: describe exclusions from scope of the plan
7. References: GEIA provided
8. Terms, Definitions and Acronyms: 39 IPC and GEIA terms included
9. Objectives: author is instructed to address the following:
   - Reliability: how will this be demonstrated?
   - Configuration control and product identification
   - Caveats: remaining risks and limitations of use
   - Deleterious effects of tin whiskers: how mitigated?
   - Repair, rework, maintenance, and support

How to prefer suppliers who are using this approach?

Summary (1 of 2)

(1) Failure to apply NASA Workmanship Standards to contracts
J-STD-001ES Adoption
Non-Standard Processes
The Packaging Design Dilemma

Ineffective attention to established Workmanship requirements during vendor selection, product design, and process engineering are very difficult to overcome during the build cycle. New packaging design standards are needed to capture design rules formerly in the NASA Workmanship standards.

(2) CDM

ESD safety techniques for CDM events need development. These methods may include new circuit and board design and test rules. High speed performance will continue to drive chip designs to be less CDM-robust.

(3) WSF

NASA Workmanship Standards methods are not fully effective for pH-neutral flux and do not address voiding. NASA needs to develop new assurance rules for use of WSF.

Summary (2 of 2)

(4) High Density Interconnect PCB's

Low-volume producers of this technology, who service the NASA market, are not uniformly considered a quality-mature supply chain for PCB HDI. IST testing is recommended for investigation as a quality assurance tool for mitigating this quality risk.

(5) Column Grid Area Array Interconnect

Though R&D work has progressed significantly over the last ten years in this technology area, there is still an absence of robust quality assurance rules for CGA attachments. The IPC address some critical areas but others may need to be addressed locally.

(6) Pb-free

NASA policy statements are not uniform for Pb-free solder risk mitigation. The Workmanship Standards Program is developing a Pb-free implementation plan template to facilitate compliance by NASA organizations and suppliers who are seeking to comply with the published policy statements.