ous simulated network settings.

- An actual implementation of a mesh network architecture that integrates network control and optimization functionalities. The integral approach combines communication, navigation, control, and other functions needed to perform the mission. Each network node (e.g., robot) houses modules such as robot control processor, sensor fusion processor, and image processor, which are all interconnected through a communication module. The communication module connects all the nodes in the network. The configuration can be customized for designer's needs such as reduction of power consumption or simplification of wiring. In the higher level of the R3MOON architecture, a human/machine interface is embedded for executing AGNC's 4D-GIS and for monitoring and management of the network.
- A communication module that can be configured with different routing algorithms to run the mesh network. Both proactive [e.g., OLSR (Optimized Link State Routing)] and reactive (e.g., AODV) based routing protocols can be used in the module. A mesh wireless network with optimized routing algorithms enhances system reliability and performance.

This work was done by Ching-Fang Lin of American GNC Corp. for Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18501-1.

Fiber-Scanned Microdisplays

Lyndon B. Johnson Space Center, Houston, Texas

Helmet- and head-mounted display systems, denoted fiber-scanned microdisplays, have been proposed to provide information in an "augmented reality" format (meaning that the information would be optically overlaid on the user's field of view). A system of this type would include laser diodes feeding light into the input ends of optical fibers. The output ends of the fibers would be vibrated in prescribed patterns (scanned), in synchronism with excitation of the laser diodes, to trace out the patterns to be displayed. Lenses would form virtual images of the patterns and project the images directly (or by reflection) into the viewer's eyes.

The effective object distance of the images could be set to approximate the distances of other objects in the field of view, so that the viewer need not refocus to view the display. The display units could be positioned to present the displays at the margin of the field of view, thereby minimizing distraction when the user needs to concentrate attention elsewhere. Alternatively, the display units could be mounted so that a turn of the eye or a slight turn of the head from a nominal straight-ahead orientation would be necessary for viewing the displays.

This work was done by Janet Crossman-Bosworth and Eric Seibel of the University of Washington for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809. MSC-23847-1

Reconfigurable Fault Tolerance for FPGAs

FPGAs can be reconfigured to provide higher capacity or fault-tolerant redundancy.

Lyndon B. Johnson Space Center, Houston, Texas

The invention allows a field-programmable gate array (FPGA) or similar device to be efficiently reconfigured in whole or in part to provide higher capacity, non-redundant operation. The redundant device consists of functional units such as adders or multipliers, configuration memory for the functional units, a programmable routing method, configuration memory for the routing method, and various other features such as block RAM, I/O (random access memory, input/output) capability, dedicated carry logic, etc. The redundant device has three identical sets of functional units and routing resources and majority voters that correct errors. The configuration memory may or may not be redundant, depending on need. For example, SRAM-based FPGAs will need some type of radiation-tolerant configuration memory, or they will need triple-redundant configuration memory. Flash or anti-fuse devices will generally not need redundant configuration memory. Some means of loading and verifying the configuration memory is also required. These are all components of the pre-existing redundant FPGA.

This innovation modifies the voter to accept a MODE input, which specifies whether ordinary voting is to occur, or if redundancy is to be split. Generally, additional routing resources will also be required to pass data between sections of the device created by splitting the redundancy. In redundancy mode, the voters produce an output corresponding to the two inputs that agree, in the usual fashion. In the split mode, the voters select just one input and convey this to the output, ignoring the other inputs. In a dual-redundant system (as opposed to triple-redundant), instead of a voter, there is some means to latch or gate a state update only when both inputs agree. In this case, the invention would require modification of the latch or gate so that it would operate normally in redundant mode, and would separately latch or gate the inputs in non-redundant mode.

For fault tolerance, it is assumed that only one fault will occur within a voting group within one voting cycle, and thus, the fault can be eliminated by majority voting. Three voters are often used, providing three values to the next voting group, and so on, with the