GHz, efficiencies of TWTs are still quite low. A major reason is that at higher frequencies, dimensional tolerance variations from conventional micromachining techniques become relatively large with respect to the circuit dimensions. When this is the case, conventional design-optimization procedures, which ignore dimensional variations, provide inaccurate designs for which the actual amplifier performance substantially underperforms that of the design. Thus, this new, robust TWT optimization design algorithm was created to take account of and ameliorate the deleterious effects of dimensional variations and to increase efficiency, power, and yield of high-frequency TWTs.

This design algorithm can help extend the use of TWTs into the terahertz frequency regime of 300–3000 GHz. Currently, these frequencies are underutilized because of the lack of efficient amplifiers, thus this regime is known as the "terahertz gap." The development of an efficient terahertz TWT amplifier could enable breakthrough applications in space science molecular spectroscopy, remote sensing, nondestructive testing, high-resolution "through-the-wall" imaging, biomedical imaging, and detection of explosives and toxic biochemical agents.

This work was done by Jeffrey D. Wilson of Glenn Research Center and Christine T. Chevalier of Analex Corp. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18378-1.

Optimal and Local Connectivity Between Neuron and Synapse Array in the Quantum Dot/Silicon Brain

This bio-inspired technique can enable artificial intelligence in computing technology.

NASA's Jet Propulsion Laboratory, Pasadena, California

This innovation is used to connect between synapse and neuron arrays using nanowire in quantum dot and metal in CMOS (complementary metal oxide semiconductor) technology to enable the density of a brainlike connection in hardware. The hardware implementation combines three technologies:

1. Quantum dot and nanowire-based compact synaptic cell (50×50 nm^2) with inherently low parasitic capacitance (hence, low dynamic power $\approx 10^{-11}$ watts/synapse),
2. Neuron and learning circuits implemented in 50-nm CMOS technology, to be integrated with quantum dot and nanowire synapse, and
3. 3D stacking approach to achieve the overall numbers of high density $O(10^{12})$ synapses and $O(10^{8})$ neurons in the overall system.

In a 1-cm^2 of quantum dot layer sitting on a 50-nm CMOS layer, innovators were able to pack a 10^6-neuron and 10^{10}-synapse array; however, the constraint for the connection scheme is that each neuron will receive a non-identical 10^4-synapse set, including itself, via its efficacy of the connection.

This is not a fully connected system where the 100×100 synapse array only has a 100-input data bus and 100-output data bus. Due to the data bus sharing, it poses a great challenge to have a complete connected system, and its constraint within the quantum dot and silicon wafer layer.

For an effective connection scheme, there are three conditions to be met:

1. Local connection.
2. The nanowire should be connected locally, not globally from which it helps to maximize the data flow by sharing the same wire space location.
3. Each synapse can have an alternate summation line if needed (this option is doable based on the simple mask creation).

The $10^3 \times 10^3$-neuron array was partitioned into a 10-block, $10^2 \times 10^3$-neuron array. This building block can be completely mapped within itself (10,000 synapses to a neuron).

This work was done by Tuan A. Duong, Christopher Assad, and Anilkumar P. Thakoor of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-46222

Method and Circuit for *In-Situ* Health Monitoring of Solar Cells in Space

This method has application in solar arrays for powering unmanned vehicles.

John H. Glenn Research Center, Cleveland, Ohio

This innovation represents a method and circuit realization of a system designed to make *in-situ* measurements of test solar-cell operational parameters on orbit using readily available high-temperature and high-ionizing-radiation-tolerant electronic components. This innovation enables on-orbit *in-situ* solar-array health monitoring and is in response to a need recognized by the U.S. Air Force for future solar arrays for unmanned spacecraft. This system can also be constructed out of commercial-grade electronics and can be embedded into terrestrial solar power system as a diagnostics instrument.

This innovation represents a novel approach to I-V curve measurement that is radiation and temperature hard, consumes very few system resources, is economical, and utilizes commercially available components. The circuit will also operate at temperatures as low as –55 °C and up to +225 °C, allowing it to reside close to the array in direct sunlight. It uses a swept mode transistor functioning as a resistive load while utilizing the solar cells

themselves as the biasing device, so the size of the instrument is small and there is no danger of over-driving the cells. Further, this innovation utilizes nearly universal spacecraft bus resources and therefore can be readily adapted to any spacecraft bus allowing for ease of retrofit, or designed into new systems without requiring the addition of infrastructure.

One unique characteristic of this innovation is that it effects the measurement of I-V curves without the use of large resistor arrays or active current sources normally used to characterize cells. A single transistor is used as a variable resistive load across the cell. This multi-measurement instrument was constructed using operational amplifiers, analog switches, voltage regulators, MOSFETs, resistors, and capacitors. The operational amplifiers, analog switches, and voltage regulators are silicon-on-insulator (SOI) technology known for its hardness to the effects of ionizing radiation. The SOI components used can tolerate temperatures up to 225 °C, which gives plenty of thermal headroom allowing this circuit to perhaps reside in the solar cell panel itself where temperatures can reach over 100 °C.

This work was done by Michael J. Krasowski and Norman F. Prokop of Glenn Research Center.

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18461-1.