the necessary FRF.20 negotiations messages can be generated to control the connecting router, not only to turn on IP header compression but also to adjust the compression parameters. The FRF.20 negotiation (or control) message is composed in the FRF.20 adapter by interpreting the incoming router request message. Many of the fields are simply transcribed from request to response while the control field indicating response and type are modified.
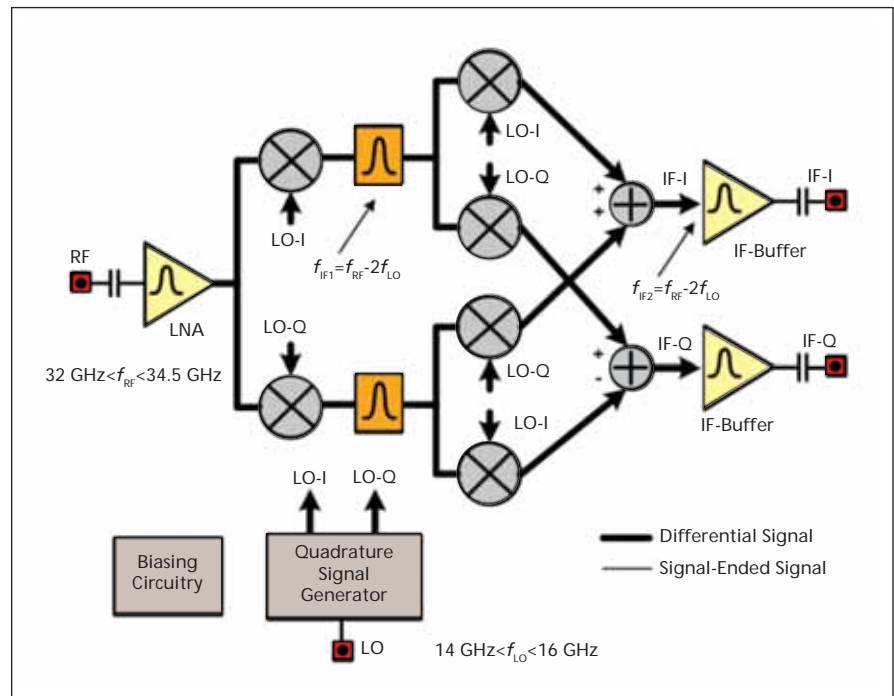
Ka-Band SiGe Receiver Front-End MMIC for Transponder Applications

New architecture improves the quality of the down-converted IF quadrature signals.

NASA's Jet Propulsion Laboratory, Pasadena, California

A fully integrated, front-end Ka-band monolithic microwave integrated circuit (MMIC) was developed that houses an LNA (low noise amplifier) stage, a down-conversion stage, and output buffer amplifiers. The MMIC design employs a two-step quadrature down-conversion architecture, illustrated in the figure, which results in improved quality of the down-converted IF quadrature signals. This is due to the improved sensitivity of this architecture to amplitude and phase mismatches in the quadrature down-conversion process. Current sharing results in reduced power consumption, while 3D-coupled inductors reduce the chip area. Improved noise figure is expected over previous SiGe-based, front-end designs.

This is the first SiGe-based receiver front-end that is capable of finding use in multiple transponder instrument programs. The design uses the latest IBM8HP SiGe process, thereby allowing for improved MMIC performance in the mm-wave regime. Improved performance is expected in terms of power consumption, quality of down-converted signals, and receiver noise figure over SiGe-based designs published by the Air

Ka-Band SiGe-Based Receiver front-end MMIC architecture.

Force Research Laboratory (AFRL) and the Army Research Lab (ARL).

Robust Optimization Design Algorithm for High-Frequency TWTs

A TWT amplifier design algorithm has applications in remote sensing, biomedical imaging, and detection of explosives and toxic biochemical agents.

John H. Glenn Research Center, Cleveland, Ohio

Traveling-wave tubes (TWTs), such as the Ka-band (26-GHz) model recently developed for the Lunar Reconnaissance Orbiter, are essential as communication amplifiers in spacecraft for virtually all near- and deep-space missions. This innovation is a computational design algorithm that, for the first time, optimizes the efficiency and output power of a TWT while taking into account the effects of dimensional tolerance variations.

Because they are primary power consumers and power generation is very expensive in space, much effort has been exerted over the last 30 years to increase the power efficiency of TWTs. However, at frequencies higher than about 60

GHz, efficiencies of TWTs are still quite low. A major reason is that at higher frequencies, dimensional tolerance variations from conventional micromachining techniques become relatively large with respect to the circuit dimensions. When this is the case, conventional design-optimization procedures, which ignore dimensional variations, provide inaccurate designs for which the actual amplifier performance substantially underperforms that of the design. Thus, this new, robust TWT optimization design algorithm was created to take account of and ameliorate the deleterious effects of dimensional variations and to increase efficiency, power, and yield of high-frequency TWTs.

This design algorithm can help extend the use of TWTs into the terahertz frequency regime of 300–3000 GHz. Currently, these frequencies are underutilized because of the lack of efficient amplifiers, thus this regime is known as the "terahertz gap." The development of an efficient terahertz TWT amplifier could enable breakthrough applications in space science molecular spectroscopy, remote sensing, nondestructive testing, high-resolution "through-the-wall" imaging, biomedical imaging, and detection of explosives and toxic biochemical agents.

Optimal and Local Connectivity Between Neuron and Synapse Array in the Quantum Dot/Silicon Brain

This bio-inspired technique can enable artificial intelligence in computing technology.

NASA's Jet Propulsion Laboratory, Pasadena, California

This innovation is used to connect between synapse and neuron arrays using nanowire in quantum dot and metal in CMOS (complementary metal oxide semiconductor) technology to enable the density of a brainlike connection in hardware. The hardware implementation combines three technologies:

1. Quantum dot and nanowire-based compact synaptic cell (50×50 nm^2) with inherently low parasitic capacitance (hence, low dynamic power $\approx 10^{-11}$ watts/synapse),
2. Neuron and learning circuits implemented in 50-nm CMOS technology, to be integrated with quantum dot and nanowire synapse, and
3. 3D stacking approach to achieve the overall numbers of high density

$O(10^{12})$ synapses and $O(10^{8})$ neurons in the overall system.

In a 1-cm^2 of quantum dot layer sitting on a 50-nm CMOS layer, innovators were able to pack a 10^6-neuron and 10^{10}-synapse array; however, the constraint for the connection scheme is that each neuron will receive a non-identical 10^4-synapse set, including itself, via its efficacy of the connection.

This is not a fully connected system where the 100×100 synapse array only has a 100-input data bus and 100-output data bus. Due to the data bus sharing, it poses a great challenge to have a complete connected system, and its constraint within the quantum dot and silicon wafer layer.

For an effective connection scheme, there are three conditions to be met:

1. Local connection.
2. The nanowire should be connected locally, not globally from which it helps to maximize the data flow by sharing the same wire space location.
3. Each synapse can have an alternate summation line if needed (this option is doable based on the simple mask creation).

The $10^3 \times 10^3$-neuron array was partitioned into a 10-block, $10^2 \times 10^3$-neuron array. This building block can be completely mapped within itself (10,000 synapses to a neuron).

Method and Circuit for *In-Situ* Health Monitoring of Solar Cells in Space

This method has application in solar arrays for powering unmanned vehicles.

John H. Glenn Research Center, Cleveland, Ohio

This innovation represents a method and circuit realization of a system designed to make *in-situ* measurements of test solar-cell operational parameters on orbit using readily available high-temperature and high-ionizing-radiation-tolerant electronic components. This innovation enables on-orbit *in-situ* solar-array health monitoring and is in response to a need recognized by the U.S. Air Force for future solar arrays for unmanned spacecraft. This system can also be constructed out of commercial-grade electronics and can be embedded into terrestrial solar power system as a diagnostics instrument.

This innovation represents a novel approach to I-V curve measurement that is radiation and temperature hard, consumes very few system resources, is economical, and utilizes commercially available components. The circuit will also operate at temperatures as low as –55 °C and up to +225 °C, allowing it to reside close to the array in direct sunlight. It uses a swept mode transistor functioning as a resistive load while utilizing the solar cells