Abstract for

Advanced Avionics and Processor Systems for a Flexible Space Exploration Architecture

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The Advanced Avionics and Processor Systems (AAPS) project, formerly known as the Radiation Hardened Electronics for Space Environments (RHESE) project, endeavors to develop advanced avionic and processor technologies anticipated to be used by NASA's currently evolving space exploration architectures. The AAPS project is a part of the Exploration Technology Development Program, which funds an entire suite of technologies that are aimed at enabling NASA's ability to explore beyond low earth orbit. NASA's Marshall Space Flight Center (MSFC) manages the AAPS project.

AAPS uses a broad-scoped approach to developing avionic and processor systems. Investment areas include advanced electronic designs and technologies capable of providing environmental hardness, reconfigurable computing techniques, software tools for radiation effects assessment, and radiation environment modeling tools. Near-term emphasis within the multiple AAPS tasks focuses on developing prototype components using semiconductor processes and materials (such as Silicon-Germanium (SiGe)) to enhance a device's tolerance to radiation events and low temperature environments. As the SiGe technology will culminate in a delivered prototype this fiscal year, the project emphasis shifts its focus to developing low-power, high efficiency total processor hardening techniques. In addition to processor development, the project endeavors to demonstrate techniques applicable to reconfigurable computing and partially reconfigurable Field Programmable Gate Arrays (FPGAs). This capability enables avionic architectures the ability to develop FPGA-based, radiation tolerant processor boards that can serve in multiple physical locations throughout the spacecraft and perform multiple functions during the course of the mission.

The individual tasks that comprise AAPS are diverse, yet united in the common endeavor to develop electronics capable of operating within the harsh environment of space. Specifically, the AAPS tasks for the Federal fiscal year of 2010 are:

- Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments,
- Modeling of Radiation Effects on Electronics,
- Radiation Hardened High Performance Processors (HPP), and
- Reconfigurable Computing.

Though these tasks are diverse in their specific key performance parameters, they collectively endeavor to accomplish these specific goals: improved total ionization dose (TID) tolerance, reduced single event upset rates, increased threshold for single event latch-up, increased sustained processor performance, increased processor efficiency, increased speed of dynamic reconfigurability, reduced operating temperature range's lower bound, increased the available levels of redundancy and reconfigurability, and increased the reliability and accuracy of radiation effects modeling.

This paper describes each AAPS technology development task, reviews the accomplishments achieved within the past fiscal year of development, and describes the support these technologies may provide the architecture options being considered by NASA.

Advanced Avionics and Processor Systems for a Flexible Space Exploration Architecture

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The Advanced Avionics and Processor Systems (AAPS) technology development project was established to foster and mature the avionic and processor technologies required to fulfill NASA's goals for future space and lunar exploration. Over the past year, multiple advancements have been made within each of the individual AAPS technology development tasks. This paper provides a brief review of the project's accomplishments over the past fiscal year, discusses the applicability of these accomplishments to the Constellation program and to future NASA exploration missions, and addresses the project's termination and re-establishment within the new Exploration Technology Development and Demonstration program.

Nomenclature

°C = Temperature (degrees Celsius)

I. Introduction

THE Advanced Avionics and Processor Systems (AAPS) project, formerly known as the Radiation Hardened Electronics for Space Environments (RHESE) project, was initially established within the Exploration Technology Development Program (ETDP) to support the advanced technology needs of the National Aeronautics and Space Administration's (NASA's) Constellation program and its constituent flight projects. The AAPS technology development project has always endeavored to mature the current state-of-the-art in environmentally hardened electronic, avionic, and processor devices that are robust enough to withstand the radiation and broad temperature extremes of the space environment. At the time of this writing, NASA is preparing for the cancellation of the Constellation program and the close-out of the Exploration Technology Development Program (ETDP) and its associated technology development projects, including AAPS. However, because of an anticipated renewed emphasis on technology development and demonstration within NASA's proposed fiscal year 2011 budget, there are ongoing formulation activities aimed at initiating a new technology development program, the Exploration Technology

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Development and Demonstration (ETDD) program and, specific to this paper, a new Autonomous Systems and Avionics (ASA) project that will continue the efforts begun by AAPS to develop robust, environmentally hardened avionics and electronics for use in extreme environments – among other activities.

II. AAPS Technology Development Tasks

The individual technology development tasks that are included within the AAPS project are broad-based and diverse, but all carry the common goal of providing advanced avionic technologies that are capable of enduring the natural environments encountered by their host spacecraft. The AAPS technologies are targeted for development because they are generally not currently available from commercial sources. For the past fiscal year of 2010, the individual AAPS technology development tasks are:

- Model of Radiation Effects on Electronics (MREE),
- Radiation Hardened High Performance Processors (HPP),
- Reconfigurable Computing (RC), and
- Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments.

Two of the technology tasks that were a part of the AAPS project last year, Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF) and Volatile and Nonvolatile Memory Technologies, were removed from the project in this fiscal year because of funding constraints and resource limitations. Because the AAPS project is an active technology development effort, advancements are continually being made to address the technology needs and avionic environmental hardness requirements of NASA's spacecraft platforms. With the potential cancellation of the Constellation program, the technologies developed within the AAPS project are being assessed for their applicability to future NASA missions that seek to explore destinations beyond low Earth orbit. It is widely accepted that the technology development accomplishments associated with the AAPS project are cross-cutting in nature, meaning that though they were developed in response to a need associated with the Constellation program, the technologies themselves are well suited to be applied to a "flexible path" architecture that focuses not only on the lunar surface as a destination, but on multiple destinations residing beyond low-Earth orbit. Regardless of the actual destination, any spacecraft platform requiring high-efficiency, reliable, low-power, avionic components and systems will benefit from the environmentally-hardened technologies developed within the AAPS project over the past five years.

This paper builds on the project information provided in three previous American Institute of Aeronautics and Astronautics (AIAA) papers[1-3] and summarizes some of the more recent accomplishments made within each AAPS technology development task during the U.S. Federal Government's 2010 fiscal year, ranging from 01 October 2009 through 30 September 2010. Each of the four current AAPS technology development tasks (plus the project management function) is addressed in the following sections. Each task summary includes a brief description of the task followed by a short summary of the past year's achievements. In addition to task summaries, there is a description of the new ASA project and its multiple technology goals in fiscal year 2011.

A. AAPS Project Management

The AAPS project management function handles the day-to-day administrative and programmatic concerns of the project including budget planning, schedule development, accomplishment monitoring, risk assessment, and project execution. The project management function serves to enable the technology development tasks and to represent the task accomplishments to the ETDP program office. As a technology reaches a technology readiness level (TRL) of 6 in maturity, it is the job of the AAPS project management function to ensure a proper infusion plan is developed and implemented. NASA's Marshall Space Flight Center (MSFC) manages the AAPS project. Details concerning the programmatic management of the AAPS project and the specifics of each technology development task within the project are captured in the baselined AAPS Project Management Plan.

As a strategy to reduce duplicative efforts between NASA and other government-sponsored developers that may also be investing in environmentally hardened electronic and avionic technology, it is the responsibility of the AAPS project management function to be cognizant of external activities and investments being made by these other U.S. Government agencies, federal laboratories, academic institutes, and commercial developers and to develop collaborative efforts where appropriate. Collaborative efforts strive to leverage the technology investments of multiple sources to deliver products that may otherwise not be realized through independent and competing efforts.

To maintain cognizance of current activities, the AAPS project manager and task leads regularly attend reviews, presentations, and conferences where multiple other non-NASA technologists are working to improve the state-of-the-art in radiation hardened electronics. Over the past year, the AAPS project was represented at many of these gatherings to discuss and coordinate technology development activities, including the AIAA SPACE 2009

conference, the Air Force Research Laboratory (AFRL)-sponsored Radiation Hardened Electronics Technology workshop, the Institute of Electrical and Electronics Engineers (IEEE) Aerospace 2010 conference, the Government Microcircuit Applications and Critical Technology (GoMACTech) 2010 conference, and the IEEE Nuclear Science and Radiation Effects Conference (NSREC) 2010. As the AAPS project transitions its technology tasks from the current project structure within ETDP to the new ETDD ASA project (see section III below), it is anticipated that the same level of cross-coordination of activities between U.S. Government agencies, federal laboratories, academic institutes and commercial developers will continue into the next fiscal year and beyond.

B. Model of Radiation Effects on Electronics (MREE)

The AAPS project's MREE task is focused on developing an updated model of radiation effects on electronics. The previously used model, Cosmic Ray Effects on Micro Electronics 96 (CREME96)[4-5], has been for years the industry standard modeling tool for estimating single event effects (SEEs) in electronics. However, over the past fourteen years since its release, the state-of-the-art in microelectronics has continued to advance toward architectures that incorporate smaller feature sizes and more complex electronic structures that often include heavy metals – all of which make today's modern electronic architectures more susceptible to SEEs and radiation induced failures. The paradigm for SEE prediction in the CREME96 model is deficient in accounting for the small features, complex geometries and heavy elements common to modern electronic architectures. The CRÈME96 model has further deficiencies in that it assumes the ionization trail left by a high energy particle is much smaller than the minimum feature size of the impended electronic structure – which is no longer true when considering modern electronic devices. Also, CREME96 assumes that the SEE sensitivity of individual microcircuits could be idealized as being due to a single sensitive junction. The cross section of this junction versus the linear energy transfer (LET) rate of the ionizing particle could then be measured and used to estimate the SEE rate.

Since CREME96 was developed the minimum feature size has shrunk by more than a factor of 100. As a result, the interaction between track microstructure and device characteristics can no longer be ignored. This assumption in CREME96 has been shown to have significant shortcomings when applied to new and emerging technologies like advanced Complementary Metal-Oxide-Semiconductor (CMOS) electronics, SiGe Heterojunction Bipolar Transistors (HBTs), photodiodes, and Infra-Red Focal Plane Arrays (IR FPAs). It is therefore the goal of the MREE task to develop a more physics-based approach to SEE prediction that will provide accurate results for modern electronics parts.

Efforts are ongoing to enable, with the new modeling tool, the ability to assess the spacecraft's surrounding structure for purpose of accurately calculating spacecraft self-shielding effects when assessing the susceptibility of a particular microelectronic circuit to the external radiation environment. By using a Computer Aided Drawing (CAD) file representation of the spacecraft's structure, the modeling tool will be designed to process the CAD file – complete with material fields within the file - to determine the exact level of shielding a sensitive electronic component may receive from the surrounding spacecraft structure. This approach also allows the detailed physical structure of the microelectronic circuit and the pattern of hole-electron creation within that circuit structure to be taken into account so that the collected charge and the resulting currents within the circuit may be estimated more accurately. This new model employs Monte Carlo simulations to predict SEE rates, allowing the updated software to be referred to as "CREME-MC." The CREME-MC codes account for a propagating particle's energy loss attributable to interactions with the spacecraft, the electronic packaging, the metallization used to build the circuit, and the metallization located within the semiconductor itself. During propagation, the effects of nuclear interactions and energy loss by ionization are taken into account as well. The calculated radiation environment at the chip will be used to not only estimate the device's accumulated total dose, but to also drive a Monte Carlo simulation that predicts the SEE rate as described above.

Most of the accomplishments achieved by the MREE task within the past fiscal year stem from the establishment and update of the features made available for use though the online CREME-MC website[6] that will be employed to host the final Monte Carlo version of the CREME software. The online site is currently being used to test a Monte Carlo based simulation of the energy deposition within multiple sensitive volumes that represent junctions within the electronic device under evaluation. The sizes, shapes and locations of these volumes will be specified by the user. The site will offer the user the ability to define a multi-layered material stack that approximates the structure of the electronic device under evaluation. During the past fiscal year, the legacy CREME96 and CRÈME86 version of the software were hosted on the site. CRÈME96 is currently available on this site. CREME86 is being prepared for release to the user community on this site. The old CREME96 site at Naval Research Lab (NRL) was deactivated in mid-July 2010 and now shows a forwarding message to the Vanderbilt site.

Other improvements to the modeling software includes updated environmental models, including an updated lunar neutron albedo environment model, an updated galactic cosmic ray model, an ongoing effort to provide a solar

proton fluence model based on solar proton spectra taken from past events, and the incorporation of the High "Z" Transport (HZETRN) model for heavier ion modeling.

This task is led by NASA's MSFC with contracted support from Vanderbilt University.

C. High Performance Processors (HPP)

Certain capabilities within the Constellation architecture, such as autonomous spacecraft operations, surface mobility, and hazard avoidance and landing, require intensive data processing capabilities. Whereas numerous systems with these capabilities have been developed and deployed, their requirements and implementations are typically constrained by data processing throughput, power resources, and susceptibilities to radiation effects. The AAPS HPP task seeks to expand the capabilities of data processing-intensive, spaceflight systems by advancing the sustained throughput and processing efficiency of high-performance radiation-hardened processors while seeking processor architectures that minimize power consumption.

The performance of processors developed from technologies appropriate for aerospace environments lags that of commercial processors by multiple performance generations. The highest performing radiation tolerant, commercially produced electronics offer increased performance at expense of reduced power efficiency. The HPP task seeks to concurrently advance the state-of-the-art of these two metrics; sustained throughput and processing efficiency.

The need for power-efficient high-performance radiation-tolerant processors and the peripheral electronics required to implement functional systems is not unique to NASA; this capability could also benefit commercial aerospace entities and other governmental agencies that require highly-capable spaceflight systems. This task will therefore leverage to the extent practical, relevant external technology- and processor-development projects sponsored by other organizations. Accordingly, important factors in defining and implementing the HPP strategy and implementation are the investment plans of these organizations and cognizance of relevant prior and ongoing NASA investments. The HPP team is addressing both of these factors through ongoing communication and collaboration with these other organizations.

Within the past fiscal year, the HPP task has fostered two promising processor development activities that are currently undergoing evaluation for their suitability for use in NASA's manned spaceflight program: the HyperX and the Maestro processors.

1. HyperX

The Coherent Logix (CLX) HyperX (Hx) was developed in a collaborative Department of Defense (DoD) program; partners included the Air Force Research Laboratory, the Office of Naval Research, Defense Advanced Research Projects Agency, Army Research Laboratory, Missile Defense Agency, the Space and Naval Warfare Systems Command, and others. A follow-on collaboration between CLX, the AAPS project and NASA's Innovative Partnership Program (IPP) entitled "Extremely High-Performance, Ultra-Low Power, Radiation-Tolerant Processor: An Enabling Technology for Autonomous and Computationally Intensive Capabilities," was selected for funding by the IPP. It to assess the performance and radiation susceptibility of the base HyperX processor, then formulate and implement radiation hardening strategies. The effort was awarded in 2008 and has accomplished a baseline radiation test of the HyperX processor. Test results formed the basis for single-event effect radiation mitigation strategies that were developed in 2009 and validated in a follow-on radiation test.

To further validate the radiation mitigation techniques, four HyperX processor boards are being flown as a part of the Materials International Space Station Experiment-7 (MISSE-7). The MISSE series of flight experiments provide an opportunity to assess the performance and functionality of various hardware components and materials during long duration exposure to the space environment. In FY09, the HPP task supported MISSE-7 integration efforts to deliver the flight version of the HyperX processor for integration in to the MISSE-7 experiment. Launch of MISSE-7 occurred in November 2009.

Two of the four Hx boards are powered and executing Fast Fourier Transform (FFT) algorithms in an infinite loop and monitoring for radiation-induced single event effects. As of May 14, 2010, the boards have executed over 140,000 iterations with no faults. Figure 1 shows two photos of the HyperX hardware flown aboard the MISSE-7 experiment.

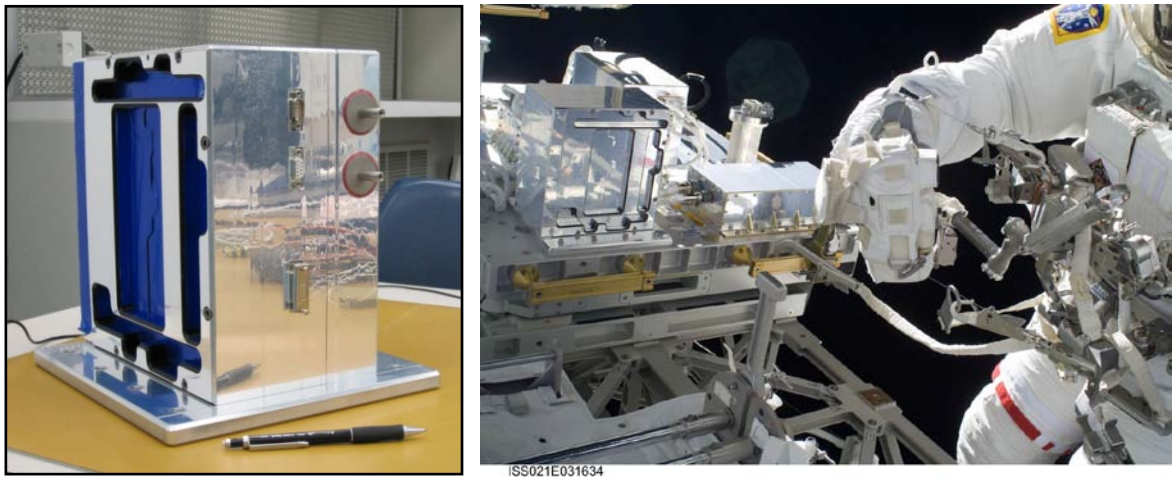

Figure 1. HyperX flight hardware (left) and HyperX experiment on-orbit during MISSE-7 installation on ISS (right).

2. Maestro

The second processor development activity being worked through the HPP task is the assessment of the Maestro Processor. This effort began as a Defense Advanced Research Projects Agency (DARPA) initiative to develop a processor that performs with a high level of efficiency across all categories of application processing ranging from bit-level stream processing to symbolic processing, and encompassing processor capabilities ranging from special purpose digital signal processors to general purpose processors. A radiation hardened version of the Tile-64, a commercial processor with heritage from this DARPA initiative, was developed in a collaborative National Reconnaissance Organization (NRO)/Defense Threat Reduction Agency (DTRA)/DARPA development project. Processor wafers were delivered March 9, 2010. Radiation test of packaged devices will commence in summer 2010.

The throughput for this device is consistent with HPP task objectives and metrics. An objective of HPP going forward will be to leverage investments in Maestro or other processor platforms to deliver a system with throughput comparable to Maestro, but at lower power dissipation.

Of particular importance to the HPP task is the continued coordination between the HPP task and the ETDP Autonomous Landing and Hazard Avoidance Technology (ALHAT) project. The HPP task is committed to coordinating the current status of processor development while the ALHAT project coordinates the current status of processing needs. During FY09, these two technology development efforts continued to work through the processing requirements as generated by ALHAT and the processor capabilities as generated by HPP, with the ultimate goal being to match each with the other.

The HPP task will transition out of AAPS and into ASA once the current AAPS project closes at the end of fiscal year 2010. This task is lead by NASA's Goddard Space Flight Center (GSFC), with support from NASA's MSFC, NASA's Langley Research Center (LaRC), and the JPL.

D. Reconfigurable Computing (RC)

The concept of Reconfigurable Computing[7] offers the promise of new capabilities within any particular plan of exploration that involves complex spacecraft. These new capabilities focus on the reduction of subsystem level flight spares inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces.

The RC task proposes a new paradigm for circuitry to respond to failures other than by redundancy voting schemes alone. The RC task strives to provide better failed circuitry detection, enablement of autonomous repair and/or replacement of defects, and support adapting circuitry to accommodate system failures. The goals of the RC task also include the concept of requiring a single configurable processor to autonomously conform to multiple configurations. Accomplishment of this goal yields a reduction in spares required to be carried on long-duration missions, since a single spare would then fit many processing functions. Such architecture adaptability will provide a great saving in spares volume and weight required by extended duration missions.

Three areas of focus have been identified for the RC task; internal modularity, external modularity, and fault detection and mitigation. The first involves ability of the core processor to emulate any form of computing resource as needed to serve all of the capacities required. The second enables the first by providing a capability to interface resources to any target system, by adapting communication standards, physical and electrical interconnections, and other parameters of the host system to hook up to the computing resource. The final allows the detection of an internal fault and autonomous isolation and recovery from the fault without required external involvement.

Cyclical and/or selective periodic testing will mitigate radiation damage and other commonly-feared failures. Reserve copies of circuitry will be generated and tested in order to bring them online in functional condition without interrupting system tasks. Then, the subsystem to be evaluated will be taken offline and tested with known inputs for known expected outputs in order to isolate possible undesirable responses. Provided the subsystem checks out as functionally correct, it can be returned to service, held in reserve for the next cycle of checks, or the reconfigurable processing units can be returned to a managed store for later redeployment. If the subsystem fails verification, the portions of circuitry causing the failure may be further isolated to mark those parts of the circuitry as defective and return the remainder to reserve, much as blocks of a computer hard disk are marked bad and ignored during future operations. Life limitations on electronics can be mitigated by these same means. Circuitry which becomes unstable and unreliable after extended active lifetime can be retired and new reserve circuitry powered up and configured into service, thus extending overall lifetime of the system.

Flexibility is also bolstered by the RC task. Interface reconfiguration can allow a single processor to make connections through different external interfaces as needed. By providing this external modularity, vehicle system integrity is enhanced by allowing processors to be transferred among busses and networks to replace lost functionality. Further, this directly supports the concept of reduced flight spaces required by long duration missions. During fiscal year 2009, the RC task has demonstrated the first of the three desired characteristics: internal modularity. A Xilinx FPGA was shown to reconfigure itself to perform three disparate tasks: motor control, Digital Signal Processing (DSP) computations (via an FFT), and as a finite state machine (via a Turing Machine simulator).

During the past fiscal year, the RC task demonstrated one solution to external modularity and several solutions to fault detection and mitigation. These demonstrations were performed in partnership with Montana State University (MSU). For the external modularity demonstration, MSU used two Xilinx boards as connected via a multiline bus. The boards use a soft-core pico blaze processor to monitor the lines of the bus and the data being transmitted. Should any one (or more) of the bus lines become inactive through a faulty connection or environmentally-related radiation event on the other board, the controlling board implements a dynamic input/output recovery routine, routing the faulty line data to an unused bus line for continued, resilient operations. For the fault detection and mitigation demonstration, MSU developed and tested a tile-based, soft processor computing system using a Xilinx FPGA. The researchers divided the FPGA into equally sized tiles which represent a quantum of resources that can implement a soft processor and can also be individually reprogrammed using partial reconfiguration (PR) of the FPGA. At any given time, three of the processors are configured in Triple Modular Redundancy (TMR) with the rest reserved as spare processor tiles. In the event that the TMR voter detects a fault, a recovery process is initiated that will attempt to reset, reinitialize, and resynchronize the faulted tile, allowing a mitigation technique for handling Single Event Upsets (SEUs) that may have occurred in the FPGA circuit fabric. If the tile reset is not successful, a spare processor is brought online from one of the unused tiles to replace the faulted circuit. Once the new TMR triplet is operational, an attempt is made to recover the previously faulted tile using partial reconfiguration. After PR, the recovered tile is reintroduced into the system as an available spare. This recovery process mitigates SEUs that may have occurred in the configuration Static Random Access Memory (SRAM) of the FPGA (i.e., Single Event Functional Interrupts (SEFIs)). If the system tries to use the recovered tile for a second time and immediately experiences a fault, the tile is marked as permanently Total Ionization Dose (TID) damaged and is no longer available for use. This allows the system to continue operation in the presence of TID failures in localized regions of the FPGA. The mitigation strategy and computer architecture in this project has the advantage of addressing the two main logical fault types experienced in SRAM-based FPGAs (fabric SEUs and SEFIs). Furthermore, the ability to continue operation despite localized TID damage can extend the useful life of flight hardware.

Also, to ensure continued leadership in the reconfigurable computing community, the RC team is providing a sponsorship of an academic membership in the Center for High Performance Reconfigurable Computing (CHReC), a consortium of academic representatives assembled to recommend Reconfigurable Computing research activities. The AAPS management has attended the CHReC workshops within the past fiscal year.

This task is managed by NASA's MSFC with support from NASA's LaRC.

E. Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments

The AAPS SiGe task has as its goal the development and demonstration of electronic components applicable to flight systems that possess distributed avionics architectures and require operation within extreme environments. The SiGe task was initially developed to support the Constellation program and its flight platforms that require environmental operations in the deep space and lunar surface environment. The extreme temperature conditions on the lunar surface (at worst case, -230°C in shadowed polar craters, and ranging from -180°C to +120°C lunar night to day) combined with the pervasive radiation environment of deep space preclude the use of conventional terrestrial electronics for applications such as sensing, actuation, and control. The SiGe task was formulated to address these environmental issues. Now, with the likely cancellation of the Constellation program, the products resulting from the SiGe development effort are being solicited for infusion on a wide variety of planned flight demonstrations, flagship-class missions, robotic precursor missions, and deep space science missions.

Fiscal year 2010 was the last year of development for the SiGe task. On 10 August 2010, the SiGe task held a final review at the Georgia Institute of Technology where the full team, including participants from Boeing, BAE Systems, IBM, JPL, Auburn University, Vanderbilt University, University of Tennessee, University of Maryland, Lynguent, and University of Arkansas, presented a summary of the SiGe development activity. Core to the SiGe effort is the use of low-cost, commercial SiGe Technology, which contains SiGe Heterojunction Bipolar Transistors (HBTs) and Complementary Metal-Oxide-Semiconductor (CMOS) devices.[8-12] Unlike other commercial off-the-shelf (COTS) integrated circuit technologies, SiGe offers unparalleled cryogenic temperature performance, built-in radiation tolerance, wide temperature range capability, and optimal mixed-signal circuit design flexibility at the monolithic level. Other benefits include the ability to fabricate power efficient, multiple breakdown voltage, high-speed SiGe HBTs on the same piece of silicon wafer as high density Si CMOS circuits and passive components.

At the final review, the SiGe team successfully delivered the following products:

- Low-power, radiation tolerant (to 100 krad), integrated SiGe BiCMOS mixed-signal (digital + analog + power) electronics for sensor/imager and actuator systems that can operate reliably across -180°C to +120°C, and under relevant radiation conditions.
- High-density packaging of these SiGe BiCMOS electronics components (with integrated passive components) which can operate reliably across -180°C to +120°C.
- Modeling and CAD tools for SiGe BiCMOS devices and packaging to accurately predict and simulate the electrical performance, reliability, and radiation tolerance of these SiGe BiCMOS mixed-signal circuits and packages across -180°C to +120°C, a range that is beyond the limits of all other existing electronics device models.
- Definition and implementation of a general purpose SiGe Remote Electronics Unit (REU) prototype capable of operation across -180°C to +120°C and simultaneous relevant radiation conditions.
- A final report that documents the entire SiGe development effort.

Over the past five years, the SiGe task has been producing increasingly complex designs that successively build toward the fabrication of the final REU prototype system. The "CRYO" moniker is used to identify the progressive stages of the development effort. Completed in 2005, the first iteration of the CRYO series, CRYO-1, was a proof-of-concept fabrication run containing SiGe-based basic circuit building blocks such as operational amplifiers, digital-to-analog converters, and standard characterization and test structures. The final REU prototype system, or CRYO-5, was fabricated during the past fiscal year and includes a SiGe-based REU Sensor Interface (RSI) Application Specific Integrated Circuit (ASIC) and a Digital Control (RDC) ASIC chip. Initially scheduled to be delivered in 2009, the final REU prototype delivery was slipped until August 2010 to accommodate a re-fabrication and test of the RDC ASIC chip. The RDC ASIC experienced some design problems during the final fabrication and therefore resulted in the inability to deliver the final packaged, environmentally hardened device. Instead, the functionality of the RDC was programmed into an Xilinx Field Programmable Gate Array (FPGA) that was used to perform and validate final radiation and cryogenic testing at Texas A&M University. Photographs of the individual RSI and RDC dies are shown in Figure 2 and a packaged version of the REU is shown in Figure 3.

The development, test, and delivery of the SiGe-based REU successfully raises the technology readiness level (TRL) of SiGe BiCMOS extreme environment electronics technology, including packaging, from TRL 2 (feasibility of low temperature operation of SiGe BiCMOS transistors) to TRL 6 (demonstrated integrated circuits, packaging, models, and design libraries, and functional protoypes), permitting seamless technology infusion into future spacecraft architectures.

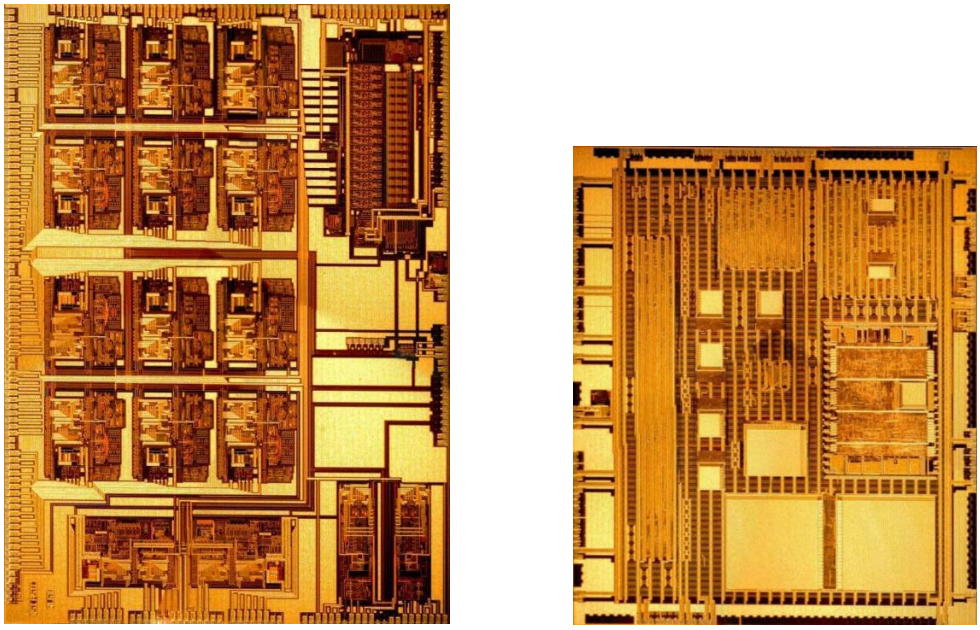

Figure 2. CRYO-5 SiGe RSI ASIC (left) and CRYO-5 SiGe RDC ASIC (right)

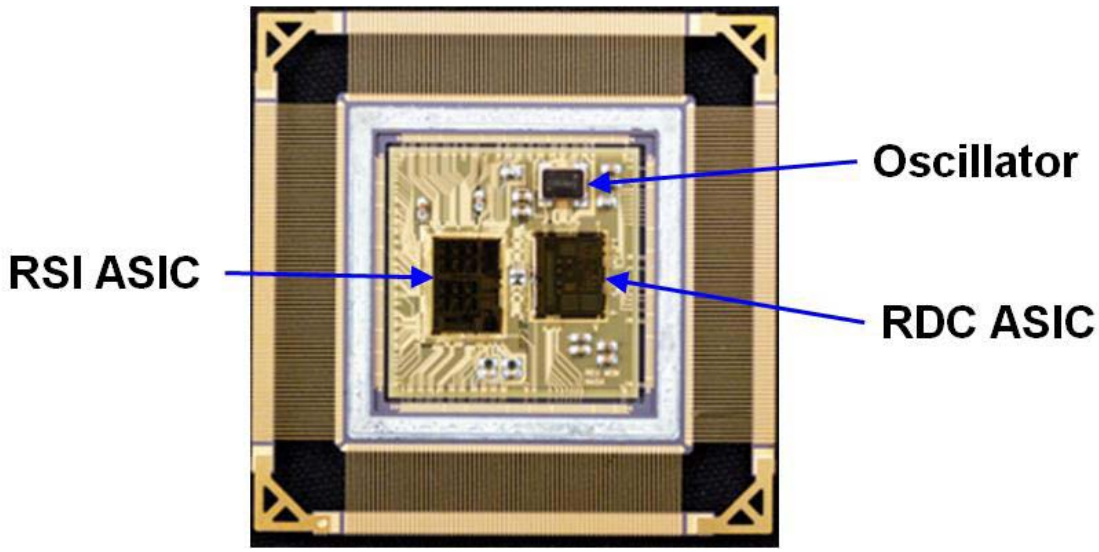

Figure 3. REU Multi-Chip Module

For purposes of testing the SiGe technology in the space environment, multiple flight experiments are underway which include SiGe-based electronic chips. Mounted on the MISSE-6 experiment are passive, unpackaged SiGe chips that function as a voltage reference. To protect the SiGe dies from atomic oxygen within the low-Earth orbit environment while allowing exposure to other environmental conditions such as radiation and temperature, the team developed a protective coating process. MISSE-6 was retrieved from the ISS during STS-128 in August of 2009. Performance tests on the SiGe die will be conducted once the full MISSE-6 payload characterization is completed by NASA Ames Research Center (ARC).

Also in cooperation with the Boeing Company, an active, packaged SiGe-based control circuit, the CRYO-3a voltage reference design, was incorporated as an integrated portion of a Boeing experiment to monitor a Thermal

Protection System material on the MISSE-7 experiment platform. MISSE-7 was launched aboard STS-129 in November of 2009 and is currently mounted on the exterior of the ISS.

The contract for this task is managed by NASA's Langley Research Center with support from the Jet Propulsion Laboratory. The Georgia Institute of Technology is the prime contractor and leads a team of multiple academic and industrial partners.

III. Transition from AAPS to ASA

At the end of fiscal year 2010, the AAPS project will be formally closed through a final project review to be conducted at MSFC on 25 August 2010. The three technology tasks that are still in development within the AAPS project, HPP, RC, and MREE, will transition from the closed project at the end of the current fiscal year into the newly formulated ASA project at the beginning of fiscal year 2011.

The ASA project is one of ten foundational technology development projects that constitute the new ETDD program. Beginning in fiscal year 2011, the new ETDD program will develop and demonstrate new technologies and prototype systems that enable new classes of human spaceflight capabilities and flagship-class mission demonstrations. Potential technology demonstrations that have been proposed include the extraction of volatiles from lunar stimulant, high-power electric propulsion, autonomous precision landing, teleoperation of surface robotics, and fission surface power systems. Flagship-class demonstration missions include (but are not limited to); long-duration, highly automated systems that feature solar electric propulsion, in-space cryogenic propellant storage and transfer, a lightweight inflatable habitation module for the International Space Station (ISS), an earth or mars-based aerocapture demonstration, and autonomous rendezvous and docking experiments. All of these potential missions will require on-board sensors, computers, flight avionics, data networks, and intelligent software to manage the mission operations and to ensure successful operation in diverse space environments.

In support of these missions, the ASA project has been formulated to comprise the technology development tasks from four different projects that were originally a part of the ETDP program. Technology tasks and investments from the AAPS project, the Integrated System Health Management (ISHM) project, Autonomy for Operations (A4O) project, and the Intelligent Software Design (ISD) project will all be combined under the single ASA project. The ASA project is being formulated to have a broader scope than the AAPS project in that it endeavors to develop cross-cutting capabilities and technologies with the following priority objectives:

- Enable crew managed autonomous operations,
- Increase reliability and capability of on-board systems, and
- Increase effectiveness and reduce costs of ground-based operations.

To accomplish these objectives, the ASA project will focus on the development of integrated avionics and software systems, increased computational power in harsh environments, automation to reduce crew workload, and increased capability to detect and respond to unexpected events and faults without dependence on ground. By implementing these technologies, functions currently handled by ground operations may be autonomously handled by onboard systems, decreasing ground operations costs and increasing the ability of the crew and flight systems to act independently.

Because of the changing nature of operations over a long period of time, as well as the need for cross-cutting technology, a related important feature of the ASA project is to develop flexible capabilities. Flexible capabilities can be swiftly configured to each mission's needs. Flexibility also provides significant benefits as the needs of missions change.

Finally, because of the need to mature technology to reduce risk, the project will adopt a strategy of migrating technology proven on the ground onto vehicles and into space-borne systems. Many technical and cultural challenges can be addressed by proving that an automation solution works on the ground. Flight controllers and ground operations personnel can ensure that a technology fits into the spacecraft operating environment, thereby paving the way for solving novel technology challenges associated with limited computational power, memory and communications infrastructures onboard vehicles. Flight controllers also work extensively with crews to train them in the use of operations technology onboard spacecraft, and so this strategy also allows the flight control and ground operations experience to pave the way for the crew autonomy experience. This path is made considerably easier by adopting the strategies of building cross-cutting and flexible technologies.

The ETDD ASA project is organized into the following seven top-level work areas:

- Automated Planning Technology – software to build and manage plans and schedules. These software systems range in capability from fully automated to decision support systems used by people.
- Discrete Control Technology – software used to track the progress of plans, automatically dispatch commands to software and systems, and gather information from other software systems to manage

plan execution. These software systems are often integrated with automated planners or Integrated System Health Management.

- Integrated System Health Management – software to determine the state and condition of a vehicle or vehicle system in the past, present and future. These software systems are informed by models of system behavior, often rooted in physics-based analysis and prognostics models that predict how and when components fail.
- Software verification algorithms – software methods to reduce the number of software defects by automating the process of finding those defects, both general and system or application specific, in source code. These software systems apply to many different classes of programming languages.
- Autocode assurance - software methods specifically designed to assist in verification and validation of automatically generated code. Autocoders principle benefits (reducing software development time) are threatened by difficulties in verifying automatically generated code; this technology development is designed to mitigate these difficulties.
- Avionics and Processing Systems – technology to develop processors, memory, data networks and packaging to survive in harsh environmental conditions, including extreme temperatures and radiation environments. These environmental conditions often preclude using terrestrial computing technology without modification; high performance computing is a critical enabler to manned exploration missions outside of Low Earth Orbit.
- Instrumentation and Sensors – technology to develop highly reliable sensors in the same environments that preclude the use of computing elements.
- Technology Integration – all of the technologies described above must work in concert in order for any space mission to be successful. Technology advances in any one area will have significant implications on the other elements of any spacecraft. In order to ensure that the ultimate capability delivered by these advances is well understood, the project will conduct ongoing efforts to ensure technologies can be successfully integrated.

Further discussion of the development activities and delivered technologies resulting from the ASA project are deferred to a future paper.

IV. Conclusion

The AAPS project has completed its final year of technology development in fiscal year 2010. The project made progress in maturing the MREE task as it provides modeling of the radiation environment and its effect on advanced, modern electronics, the HPP task as it investigates techniques that allow high efficiency, radiation hardened, potentially multi-core processors operating in extreme environments, the RC task as it develops methods of implementing a partially reconfigurable FPGA capability and input/output bus resiliency, and SiGe technology as it successfully delivered an environmentally-hardened REU prototype with supporting design tools and models, allowing further development of SiGe-based ASIC electronics. As fiscal year 2011 begins, the responsibility for developing environmentally-hardened electronics and avionics transitions to the newly formulated ASA project within the ETDD program.

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[10]Cressler, J. D., "SiGe HBT Reliability Issues Associated with Operation in Extreme Environments," *Proceedings of the 2006 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2006, pp. 3-7.

[11]Cressler, J. D., Mojarradi, M., Blalock, B., Johnson, W., Niu, G., Dai, F., Mantooth, A., Holmes, J., Alles, M., Reed, R., McCluskey, P., Berger, R., Garbos, R., Peltz, L., Joseph, A., and Eckert, C., "SiGe Integrated Electronics for Extreme Environments," *Proceedings of the 2007 GOMAC-Tech - Government Microcircuit Applications and Critical Technology Conference*, 2007, pp. 327-331.

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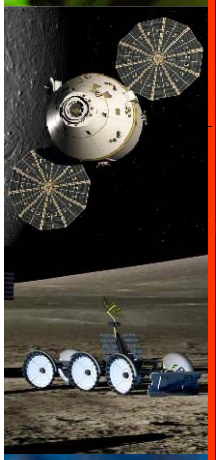


Advanced Avionics and Processor Systems for a Flexible Space Exploration Architecture

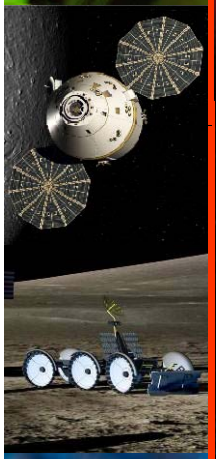
Andrew S. Keys, James H. Adams, Leigh M. Smith, *NASA Marshal Space Flight Center*

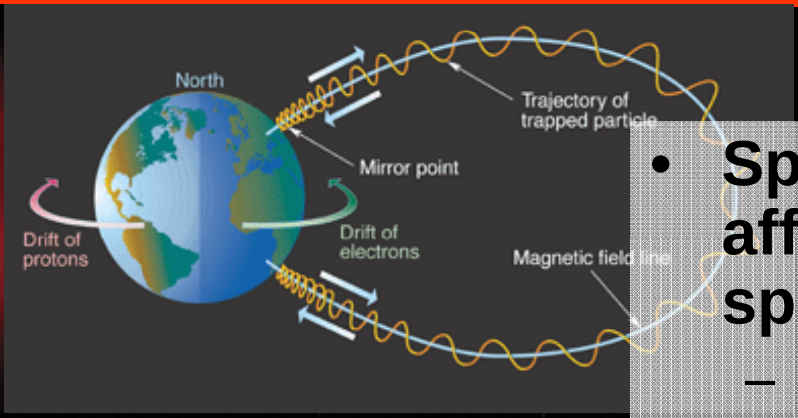
Robert E. Ray, *Jacobs Engineering Group*

Michael A. Johnson, *NASA Goddard Space Flight Center*

John D. Cressler, *Georgia Institute of Technology*

The Radiation Environment





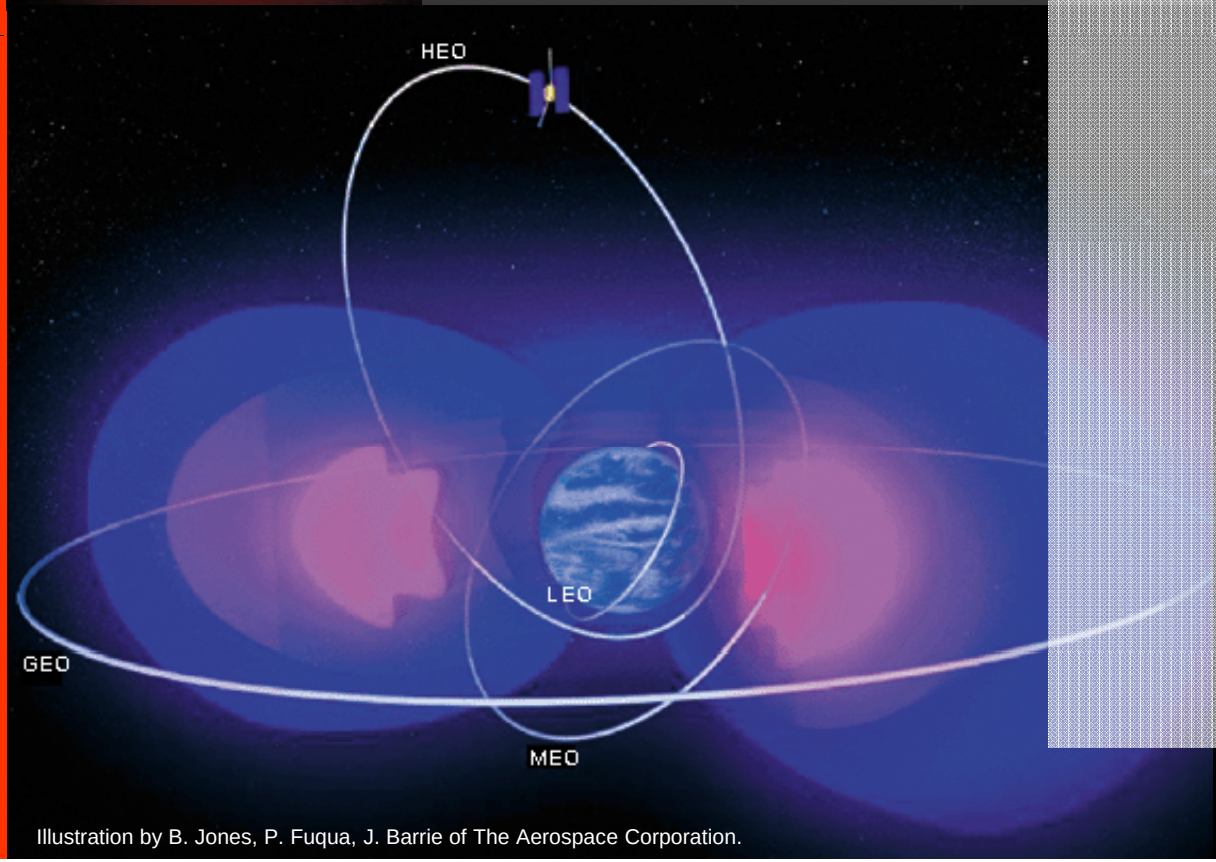
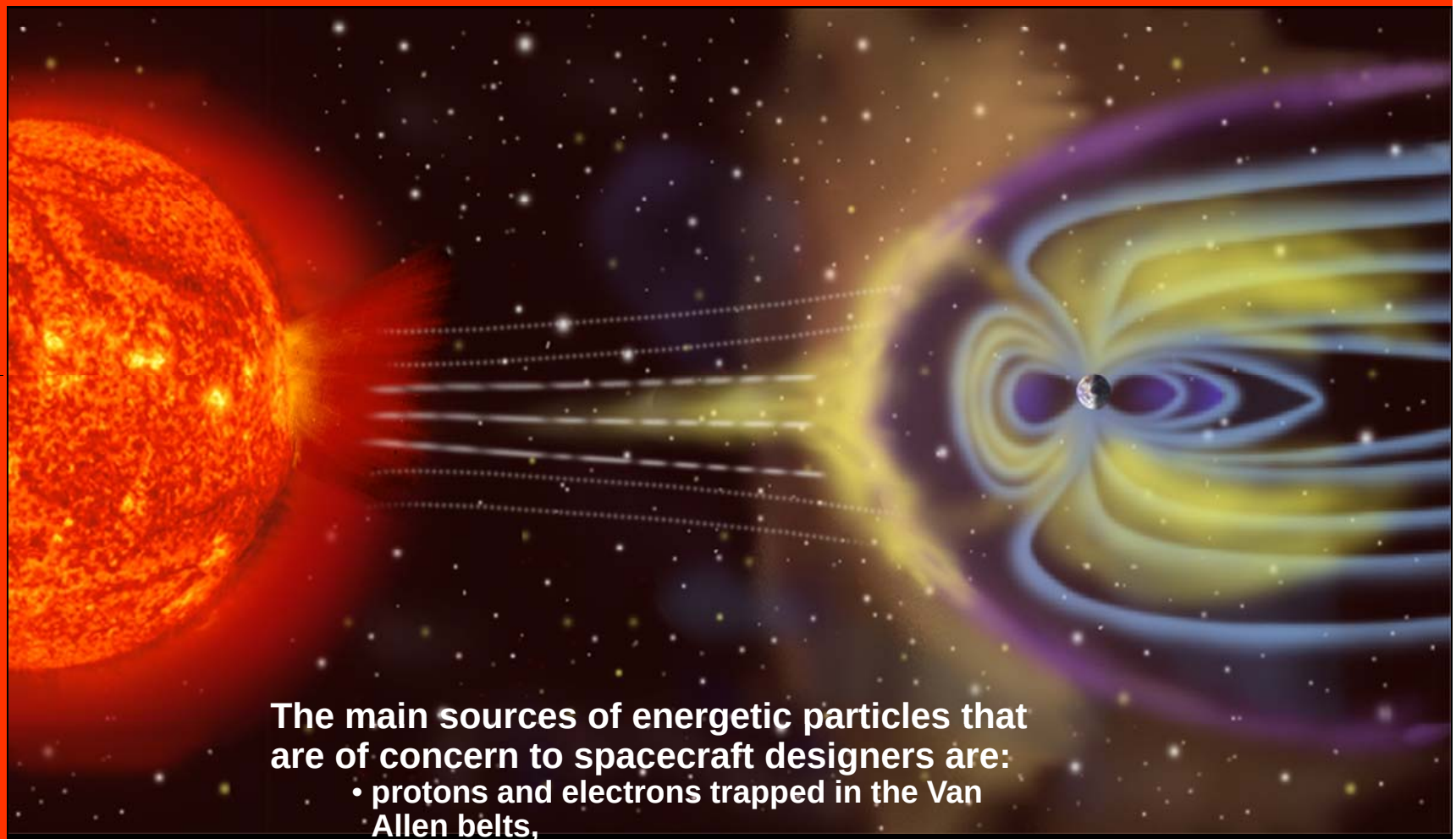


Illustration by B. Jones, P. Fuqua, J. Barrie of The Aerospace Corporation.

- **Space Radiation affects all spacecraft.**
  - Spacecraft electronics have a long history of power resets, safeing, and system failures due to:
    - Long duration exposures,
    - Unpredictable solar proton activity,
    - Ambient galactic cosmic ray

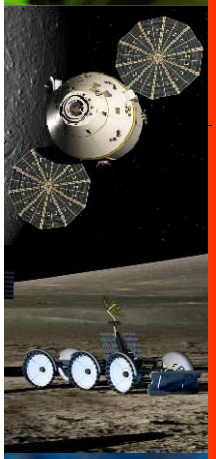
Space Environment Radiation Sources



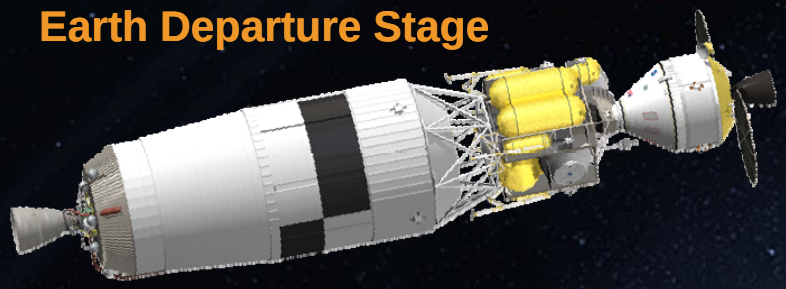
The main sources of energetic particles that are of concern to spacecraft designers are:

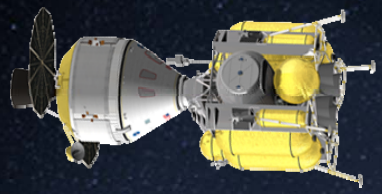
- **protons and electrons trapped in the Van Allen belts,**
- **heavy ions trapped in the Earth's magnetosphere,**
- **cosmic ray protons and heavy ions of multiple elements, and**
- **protons and heavy ions from solar flares.**

Program of Record: ConstellationSystem Elements



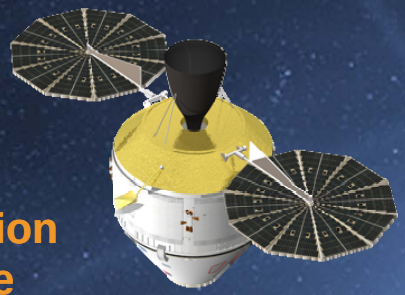
Earth Departure Stage



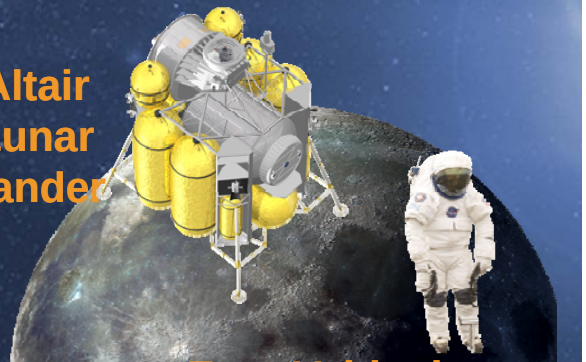


Ares V Cargo Launch Vehicle

Orion Crew Exploration Vehicle



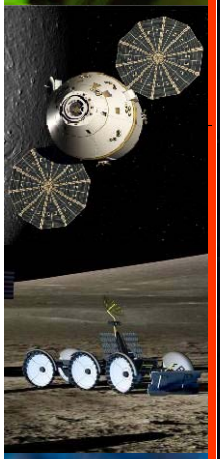
Altair Lunar Lander

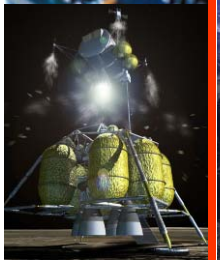


Ares I Crew Launch Vehicle

ExtraVehicular Activity Suit

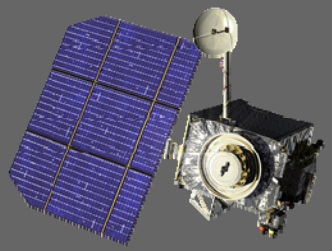
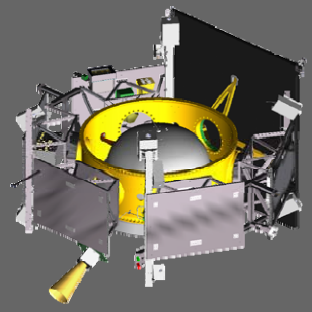
Advanced Technology for Constellation



Advanced Capabilities Division (ACD)

Lunar Precursor Robotic Program

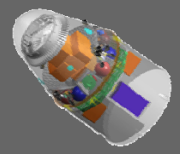



Human Research Program

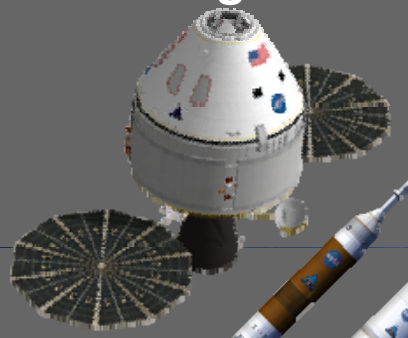

Exploration Tech. Development Program

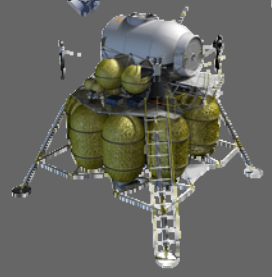


Commercial Crew Cargo Program

Constellation Program






Exploration Technology Development Program Organizational Chart

Exploration Technology Development Program
Frank Peri, Director

Diane Hope - Program Element Manager

- LaRC — Structures, Materials & Mechanisms (SMM) — Karen Whitley
- LaRC — Composite Crew Module (CCM) (Final Report FY10) — Mike Kirsch
- LaRC / GRC — Advanced Composite Technology (ACT) — Robert Draper (Acting)
- GRC — Propulsion and Cryogenic Advanced Development (PCAD) — Mark Klem
- GRC — Cryogenic Fluid Management System (CFM) — Mary Wadel
- GRC — Energy Storage and Power Systems — Carolyn Mercer
- GRC — Fission Surface Power Systems (FSPS) — Don Palac
- MSFC — Advanced Avionics & Processor Systems (AAPS) (formerly RHESE) — Andrew Keys
- KSC — In-Situ Resource Utilization (ISRU) — Bill Larson
- JSC — Human Robotic Systems (HRS) — Rob Ambrose
- JSC — Lunar Electric Rover (LER) Concept Development & Evaluation — Mike Gernhardt
- LaRC — Radiation Protection Technologies (Pre-formulation FY10) — Debi Tomek

Dana Gould - Program Element Manager

- JSC — Thermal Control for Surface (TCS) Systems — Ryan Stephan
- JSC — Autonomous Landing & Hazard Avoidance Technology (ALHAT) — Chirold Epp
- JSC — Automated Rendezvous & Docking (AR&D) Sensors (Close-out FY10) — Jennifer Mitchell
- JSC — Exploration Life Support (ELS) — Dan Barta
- JSC — Extra Vehicular Activity (EVA) Technology — David Westheimer
- ARC — Autonomy for Operations (A4O) — David Alfano
- ARC — Integrated System Health Management (ISHM) — Dave Korsmeyer
- ARC — Intelligent Software Design (ISD) — Joe Coughlan
- JPL — Advanced Environmental Monitoring & Control (AEMC) — Darrell Jan
- GRC — Dust Mitigation — Mark Hyatt
- GRC — Fire Prevention, Detection, & Suppression (FPDS) — Gary A. Ruff
- GRC — ISS Research — Fred Kohl
- LaRC — Entry Descent & Landing (EDL) Study — Paul Krasa

AAPS Project Goals & Objectives




Advanced Avionics & Processor Systems
To expand technology development efforts in radiation-hardened electronics

1.0 Project Mgmt.
To assure proper integration between the technology applications and the technology maturation.

2.0 Modeling Tools
Model of Radiation Effects on Electronics (MREE)To develop an updated model of radiation effects on electronics

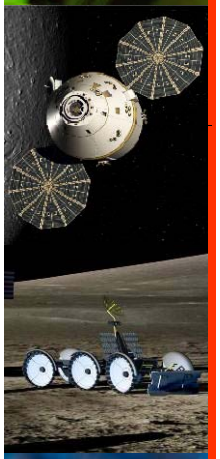
3.0 Radiation Hardened Data Sys
High Performance Processors (HPP), Memory, and SIRF. To expand the capabilities of data processing-intensive spaceflight systems

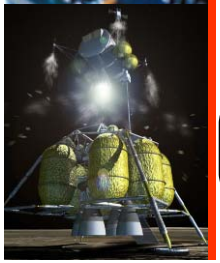
4.0 Temperature Hardened Electronics
Low-Temp Electronics (SiGe)
To develop and demonstrate extreme environment electronics components

5.0 End Item Avionics
Was reserved for future work such as, Innovative Sensors, Display Technologies, Illumination Technologies, Focal Plane Arrays, etc.

6.0 Modular & Fault Tolerant Sys
Reconfigurable Computing (RC)
Developing computing capabilities that respond to failures using new techniques

AAPS Project Management Structure



FY10 AAPS Project Prior to Technology Transition

PM = Project Manager
TechM = Technical Manager
TL = Task Lead

MSFC

AAPS Project Management

Andrew Keys (PM)
Leigh Smith (TechM)
Kathryn Vernor/Jacobs
Jay (Scott) Jones/SAIC

James Adams (TL)
Nasser Barghouty

Modeling of Radiation Effects on Electronics

Vanderbilt U.
Robert Reed
Bob Weller
(Plus Others)

GSFC

SEE-Immune Reconfigurable FPGA

Michael Johnson (TL)

Creigh Gordon
(Plus Others)

AFRL/Kirtland

LaRC

High Performance Processor

Tak Ng

Michael Johnson (TL)

JPL

Rafi Some
Carlos Villalpondo

Ga. Tech.

SiGe Electronics for Extreme Environments

Marvin Beaty (COTR)
Denise Scearce

Mohammad Mojarradi

John Cressler (TL)
(Plus Others)

Mike Watson (Acting TL)
Robert Ray/Jacobs

Tak Ng
Denise Scearse

Reconfigurable Computing

Brock LaMeres
(Plus Others)

Montana St. U.

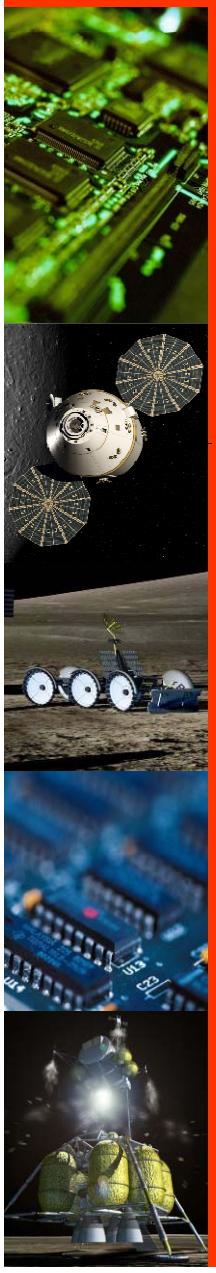
Rad-Hard Volatile and Nonvolatile Memory

Todd Macleod (TL)

Qamar Shams

Other Partners:
NRO, BAE Systems, Boeing, Xilinx

AAPS Objective and Project Goals



The **Advanced Avionics and Processor Systems (AAPS)** project expands the current state-of-the-art in spacecraft avionics components and processor systems to develop high performance devices for long duration exposure to the space and lunar environments.

- **The specific project goals of the AAPS project are to foster technology development efforts in radiation-hardened electronics possessing these associated capabilities:**
  - improved Total Ionization Dose (TID) tolerance,
  - reduced Single Event Upset (SEU) rates,
  - increased threshold for Single Event Latch-up (SEL),
  - increased sustained processor performance,
  - increased processor efficiency,
  - increased speed of dynamic reconfigurability,
  - reduced operating temperature range's lower bound,
  - increased the available levels of redundancy and reconfigurability, and
  - increased the reliability and accuracy of radiation effects modeling.

Memory Accomplishments

Objective:

Develop the Memory Test Experiment for the Fast and Affordable Science and Technology Satellite.

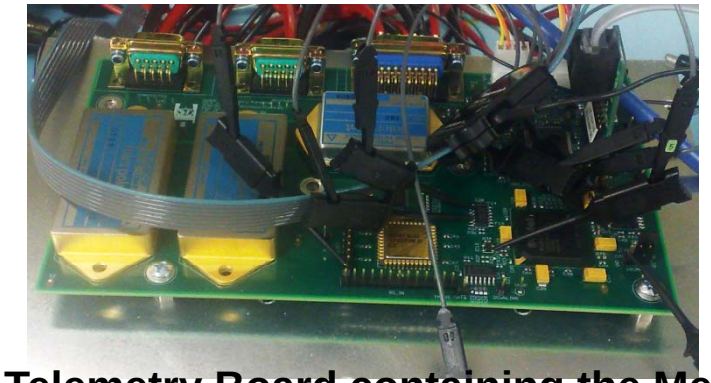
Key Accomplishment:

- June 2009

Significance:

- The Memory Test Experiment (MTE) design and development was completed. The experiment was designed and developed by MSFC civil servants developing the FASTSAT avionics. This experiment contains a Ferroelectric based memory circuit that will be tested during the year long flight of the Fast and Affordable Science and Technology Satellite (FASTSAT). Launch is scheduled for February 2010. The test consists of writing and reading test patterns into the memory device and reporting and errors detected. The MTE is incorporated into the telemetry board for the satellite.

FASTSAT Satellite



Telemetry Board containing the Memory test Experiment

Memory Accomplishments

Objective:

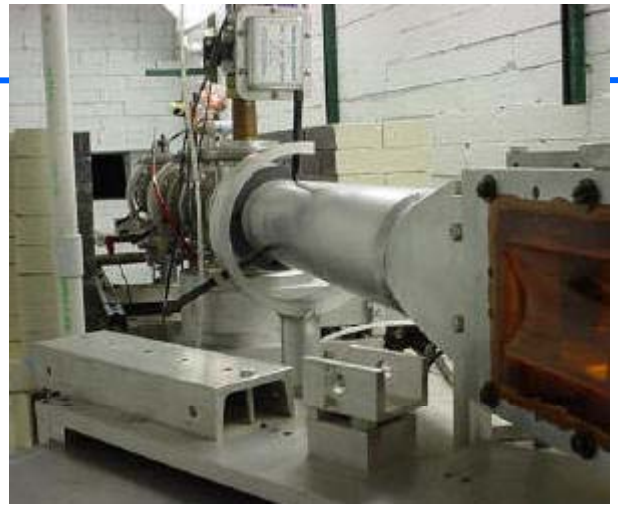
Radiation Testing the Memory Test Experiment for the Fast and Affordable Science and Technology Satellite at Indiana University.

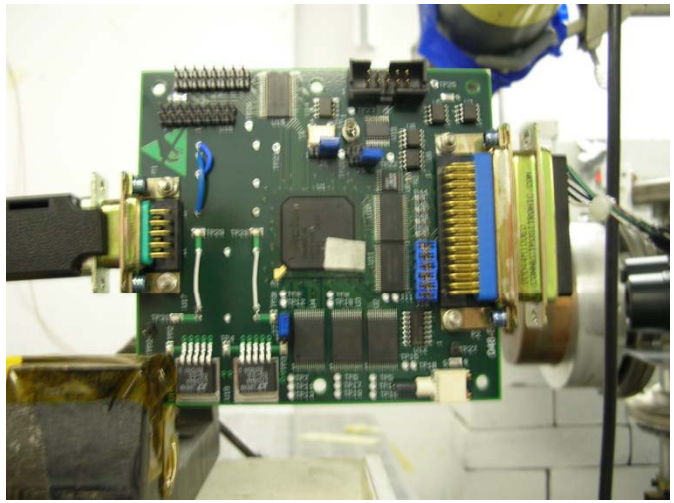
Key Accomplishment/:

- July 2009

Significance:

- The Memory Test Experiment (MTE) was tested under proton radiation at Indiana University. The test was conducted to verify the FASTSAT avionics. The MET is incorporated into the telemetry board of the FASTSAT avionics. The test consisted of putting the avionics boards into the proton beam and testing them with power on and off. Energy levels were up to 200 KeV with the dose of 115 rads. The telemetry board passed the radiation testing and no errors were recorded in the ferroelectric memory devices.





Telemetry Board

URTM Informal PDR Completed

Objective:

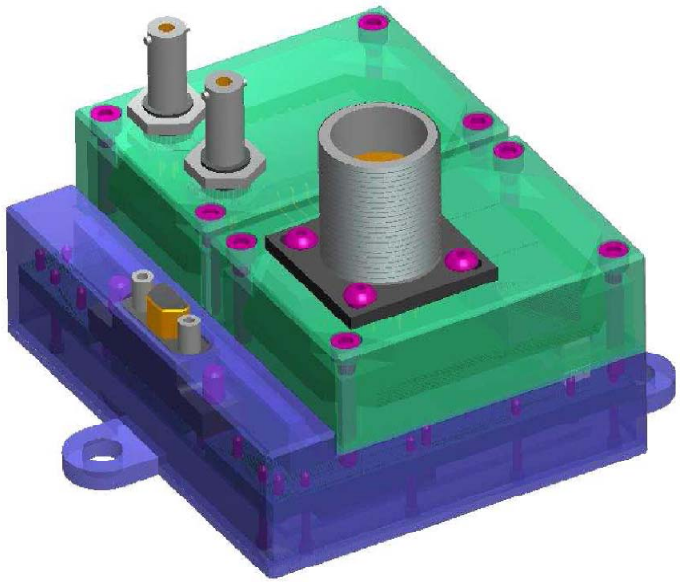
Development of External Modularity for the Radiation-Hardened Electronics for Space Environments (RHESE) Reconfigurable Computing (RC) subproject

Key Accomplishment/Deliverable/Milestone:

Universal Reconfigurable Translator Module (URTM) hel Preliminary Design Review (PDR) on 11/13/2007

Significance:

This review is a step necessary prior to beginning progress in hardware and system development, and eventual demonstration of URTM technology, as one of the three major objectives of the RHESE Reconfigurable Computing task.



Shown: Proposed URTM Unit, with Two of Three Physical Interface Modules (PIMs) Installed

Low Temperature Electronics (SiGe) Flight Experiment on MISSE-6

Objective:

To perform test and verification of SiGe radiation-hardened materials in the extreme space environment.

Key Accomplishment / Deliverable / Milestone:

Two passive SiGe-based microelectronic voltage reference dies were part of the Materials International Space Station Experiment – Flight 6 (MISSE-6) which was installed on the exterior of the ISS by the astronauts of Endeavor STS-123 during their March 2008 flight. It will remain in orbit for 6-9 months.

Significance:

These were installed as a passive experiment to test the effects of the extreme environment on the SiGe material. The SiGe dies will be tested for performance after the MISSE-6 experiment is retrieved during a later shuttle mission.

A MISSE experiment is attached to Columbus Module, during Spacewalk
(ref: NASA)

Recent NASA photograph of MISSE-6 after deployment, taken by the Space Shuttle Crew.

SiGe CRYO-5 Design Complete

Objective:

To develop and demonstrate extreme environment electronic components required for distributed architecture for Lunar, Martian, robotic, and vehicular systems using SiGe technology.

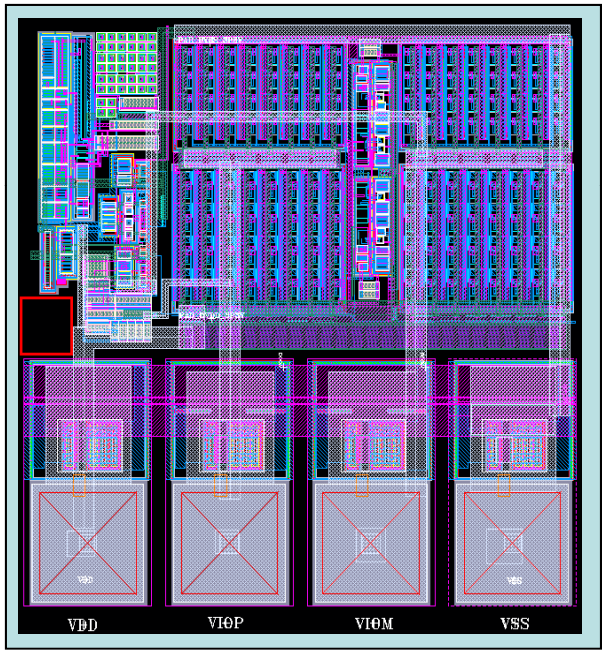
Key Accomplishment/Deliverable/Milestone:

• Date: December 5, 2008

• Description: The SiGe task has been producing increasingly complex designs that successively build toward the fabrication of a final REU prototype system. The final REU prototype system, the CRYO 5 design, will be fabricated, tested and delivered in 2009. It will include a SiGe-based REU Sensor Interface (RSI) ASIC chip and a REU Digital Control (RDC) ASIC chip.

Significance:

SiGe Remote Electronics Unit (REU) technology is ideal for use in the ORION and ARES programs by providing radiation tolerance for extended space flight.



Shown: CRYO-5 Design

SiGe CRYO-5 Release to Fabrication

SiGe CRYO-5 Release to Fabrication

Objective:

CRYO-5 is now complete and the three tiles (RSI, RDC, and test tile) are now on their way to fabrication at IBM.

Key Accomplishment / Deliverable / Milestone:

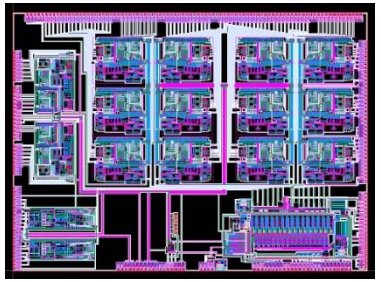
Date of Accomplishment: 13 March 2009

We have completed the CRYO-5 tape-in, consisting of all of the needed components of the final SiGe REU: the REU (Remote Electronics Unit) Sensor Interface (RSI) ASIC (Application Specific Integrated Circuit); the REU Digital Control (RDC) ASIC and a supporting test tile of various circuits. All three die are now on their way to fabrication.

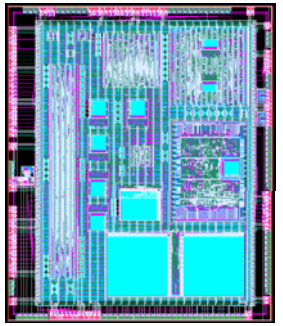
Significance:

The CRYO-5 run represents the final fabrication cycle for the SiGe task. The three tiles fabricated during this cycle will constitute the final delivered SiGe prototype package.

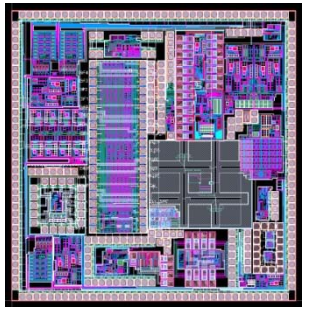
The SiGe task will demonstrate that commercially-available SiGe BiCMOS (Bipolar Complementary Metal Oxide Semiconductor) technology can be successfully used in extreme environments.



Screen capture of the final 10x14 mm^2 RSI ASIC chip from CRYO-5



Screen capture of the final 10x12 mm^2 RDC ASIC chip from CRYO-5



Screen capture of the final 5x5 mm^2 test circuit chip from CRYO-5

Reconfigurable Computing (RC) Demonstration #1

Objective:

Radiation-Hardened Electronics for Space Environments (RHESE) Reconfigurable Computing (RC) task Demonstration #1 was to show basic manual reconfiguration of the test hardware into three substantially different computing resources.

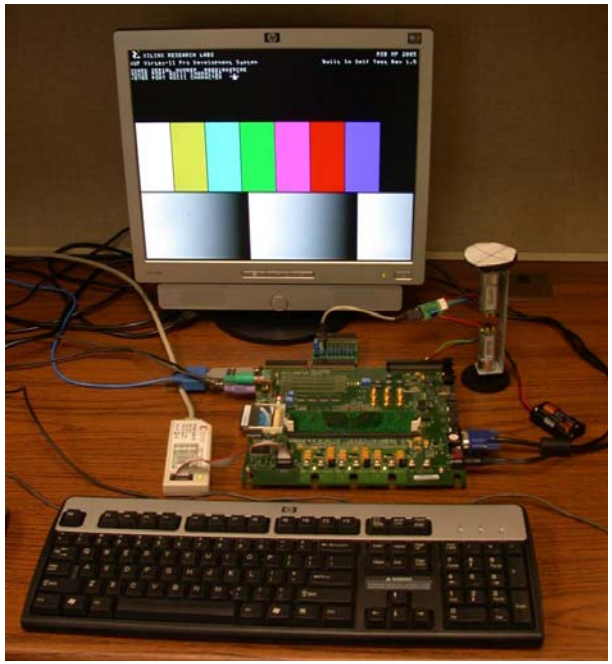
Key Accomplishment/Deliverable/Milestone:

- 13 January 2009

- Basic concepts of RC were showcased at MSFC. Coupled with the demo was an informative slideshow with background information, a description of goals and activities of the demonstration itself, and plans for future research and demonstrations of progressively more complex RC concepts and capabilities. This demo concentrated on very basic manual reconfiguration of the test hardware into three substantially different computing resources. These were: microprocessor, digital signal processor and motor control/feedback setups.

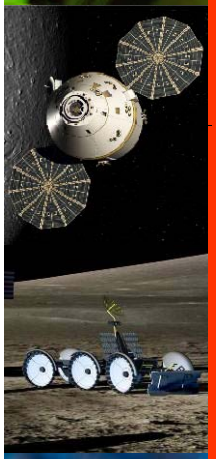
Significance:

- Establishes a foundation for RC upon which further demonstrations of internal reconfiguration, external reconfiguration, and fault recognition functions will build.
- Provides crucial publicity of RC efforts within NASA and the technical community at large; weighs heavily in efforts to garner significant technical and fiscal support for RC.



Shown: Hardware for RC Demo #1

RC Demonstrations # 2 and # 3



Objective:

The RC task is developing advanced and innovative capabilities to respond to hardware failures through the exploitation of the unique abilities of reconfigurable computing fabrics**.**

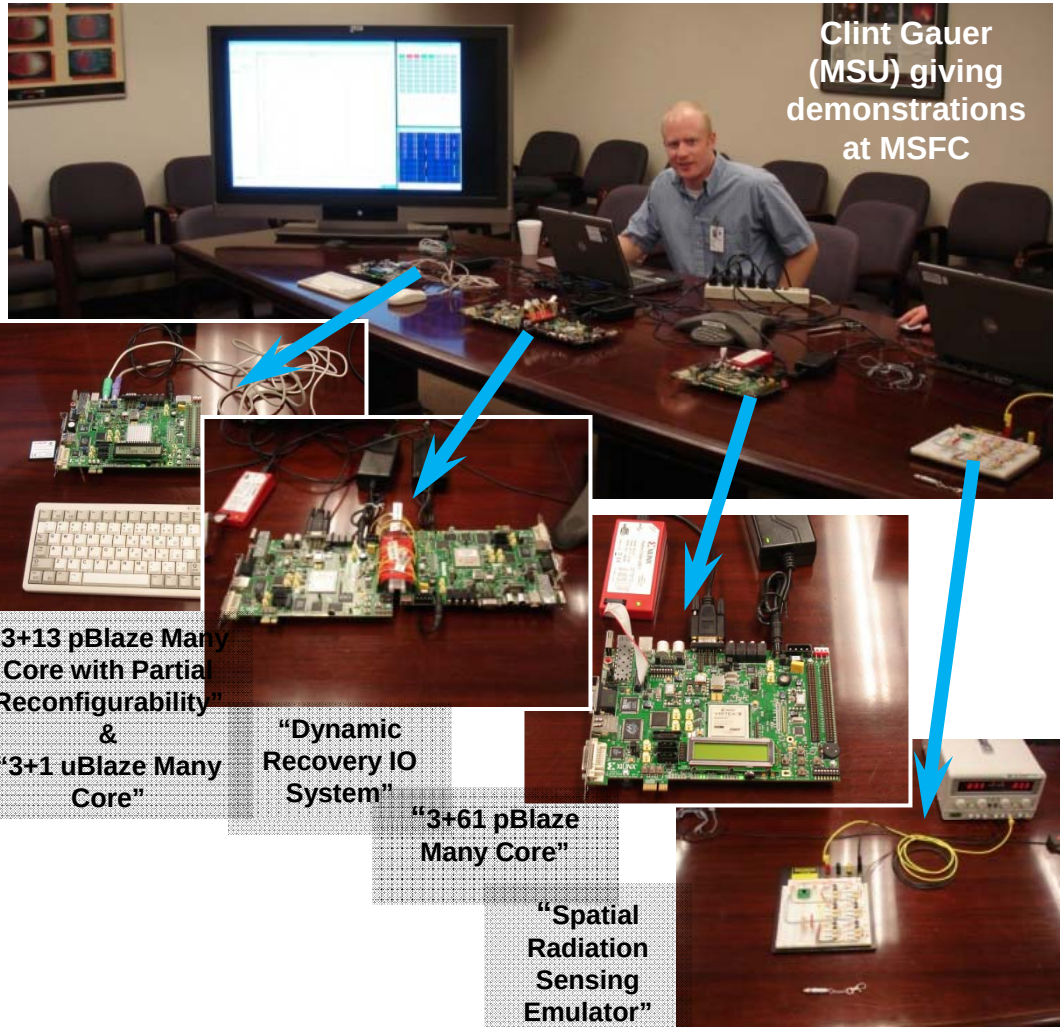
Key Accomplishment / Milestone:

- Montana State University (MSU) has worked with MSFC to ensure research in reconfigurable computing (RC) aligns with RC task objectives.

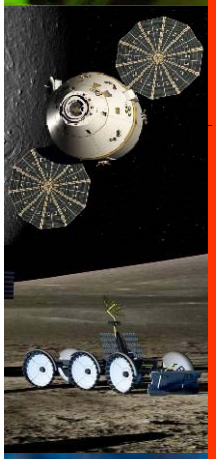
- On 07 January 2010, MSU visited MSFC to demonstrate key capabilities that serve to satisfy the RC needs:
  - Resilient and dynamic recovery from unreliable input/output (RC Demo #2)
  - Partial reconfigurability on a Field Programmable Gate Array (FPGA) using picoBlaze and microBlaze soft processor cores (RC Demo #3)

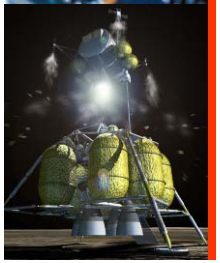
Significance:

These new capabilities demonstrate flexible, reconfigurable resources that enable the reduction of flight spare inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces.



High Performance Processor (HPP) Flight HW Delivered for MISSE-7 Integration





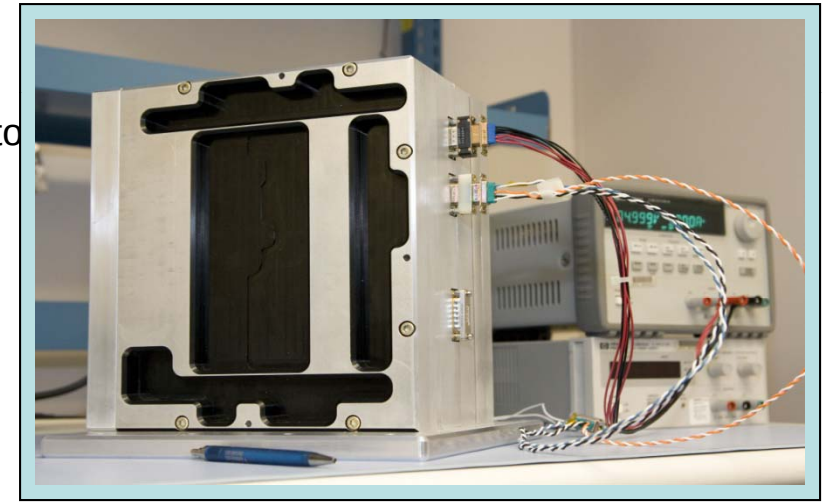
Objective:

Delivery of Materials for International Space Station Experiment-7 (MISSE-7) / HyperX experiment to the Naval Research Laboratory (NRL) and successful integration into the MISSE-7 payload.

Key Accomplishment / Deliverable / Milestone:

Date of Accomplishment: 3 March 2009

The MISSE7/ HyperX experiment was delivered to the Naval Research Laboratory and successfully integrated into the MISSE-7 payload. The experiment passed mechanical and electrical interface tests, and functional performance tests. It incorporates four HyperX flight boards, an Aeroflex LEON3-FT radiation-hardened controller board (delivered via Space Act) and flight software.



Shown: MISSE-7 flight hardware containing four HyperX processor boards and an Aeroflex LEON3-FT controller board

Significance:

The HyperX processor by Coherent Logix, Inc., is one of the processors being evaluated and tested by the HPP task for its potential use on Constellation project platforms, in particular for use on the Altair Lunar Lander.

HyperX Experiment Launched on MISSE-7

Objective:

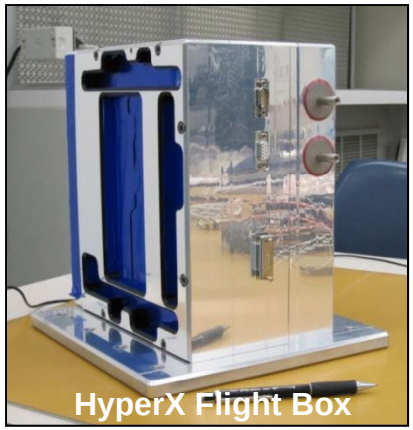
This effort seeks to assess the performance and radiation susceptibility of the base HyperX processor, then formulate, implement, validate, and verify software-based radiation hardening strategies.

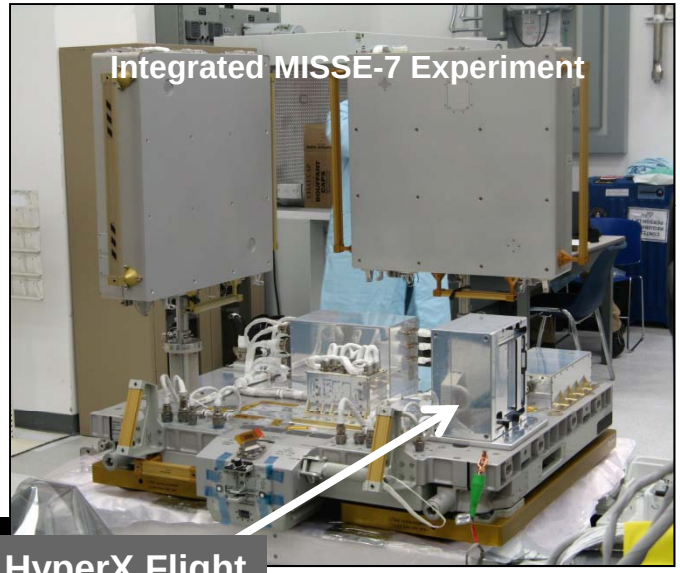
Key Accomplishment / Milestone:

- **STS-129 Launch: November 16, 2009**
- **The HyperX is one of many MISSE-7 experiments.**
- **MISSE-7 is mounted on the exterior of ISS for exposure to the low-earth orbit environment.**
- **Experiment turn-on: November 21.**
- **All systems verified: December 4.**

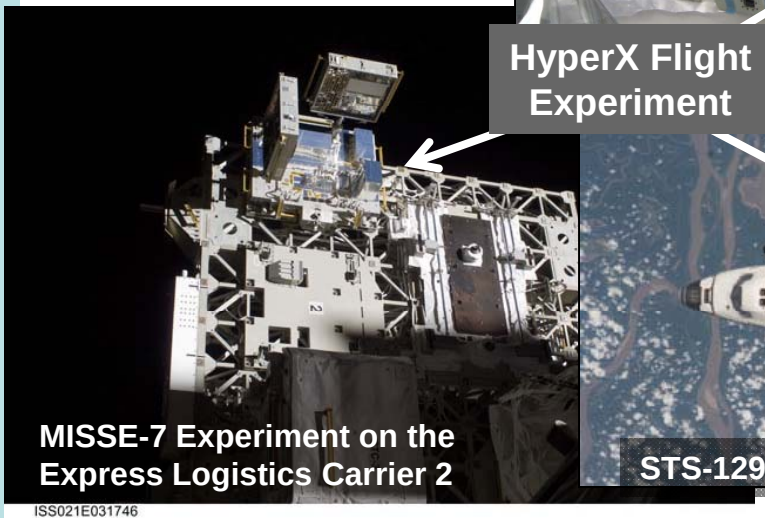
Significance:

- **The Materials International Space Station Experiment-7 (MISSE-7)/HyperX investigation intends to validate and verify ground-based tests that have examined radiation susceptibilities of this processor when executing computationally-intensive spaceflight applications, and the effectiveness of strategies that have been derived to mitigate these susceptibilities.**

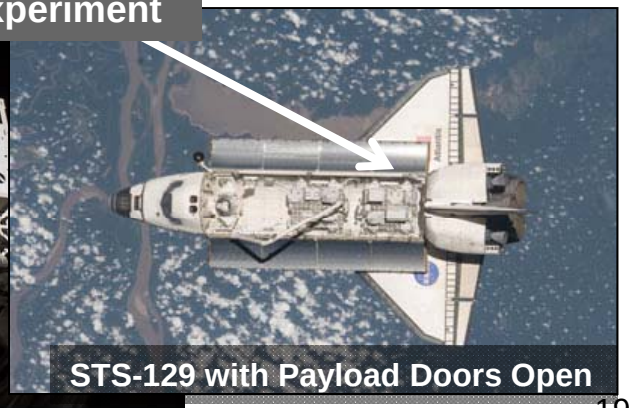

HyperX Flight Box


Integrated MISSE-7 Experiment

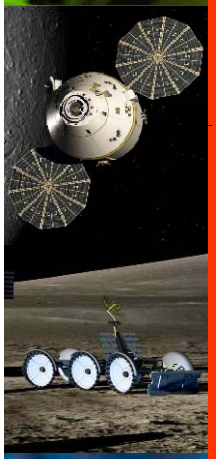
HyperX Flight Experiment


MISSE-7 Experiment on the Express Logistics Carrier 2

ISS021E031746


STS-129 with Payload Doors Open

HPP Down-Select



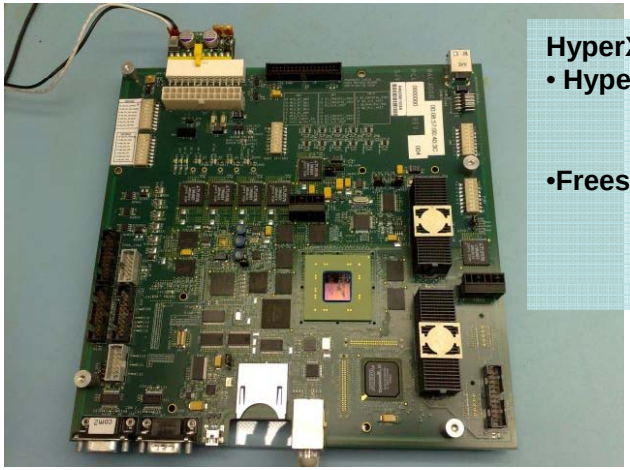
Objective: Select viable rad-hard, high performance processor for Constellation flight avionic systems

Key Accomplishment / Milestone:

- High Performance Processor (HPP) task performed study on commercial, multi-core processors using performance, power, and radiation susceptibility metrics.
- Processors benchmarked:
  - o Coherent Logix's HyperX platform, and
  - o Tilera's Tile64 platform.
- Autonomous Landing and Hazard Avoidance (ALHAT) algorithm used for benchmarking.
- Considering multiple metrics, downselect made to continue Tilera-based processor development.

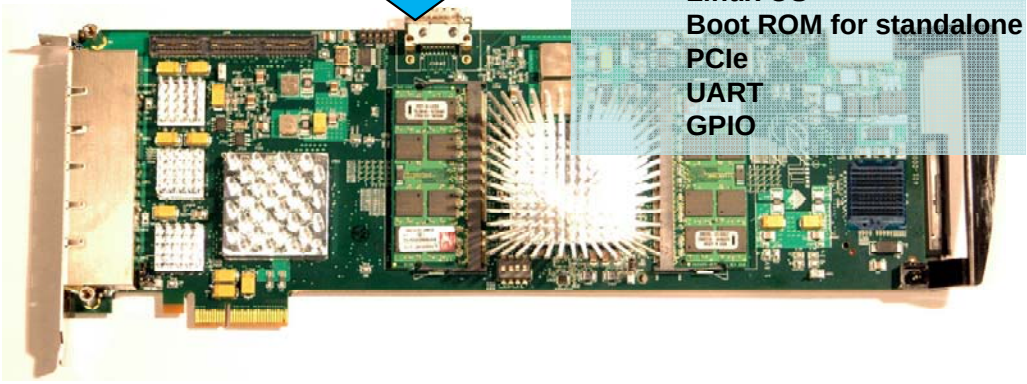
Significance:

- AAPS supports the development of design techniques and tools that allow the development of radiation hardened microprocessors capable throughput, power efficiency, and power consumption consistent with computationally-intensive capabilities.
- By leveraging the NRO-funded work to create a 49-core, rad-hard, Tilera-based processor (OPERA), HPP plans to develop a smaller, power efficient version of OPERA by FY13.



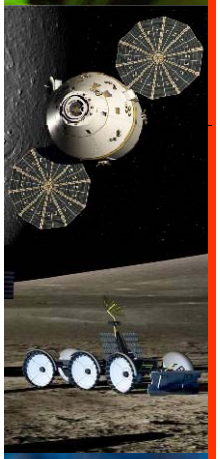
HyperX HADS1 Evaluation board
- **HyperX Processor**
  - **384 MB DDR2**
  - **GPIO**
- **Freescale ARM with:**
  - **128MB memory, SD Flash, USB, Ethernet, 2X UARTS**

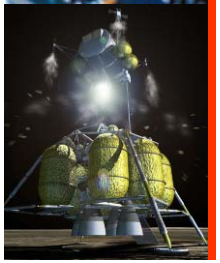
HPP Downselect to Tilera Architecture



Tile64 Evaluation Board
- **Tile64 Processor**
  - **12 port GigE switch**
  - **XAUI**
  - **128MB memory**
  - **Linux OS**
  - **Boot ROM for standalone**
  - **PCIe**
  - **UART**
  - **GPIO**

CREME-MC Alpha Version Released





Objective: ***Model of Radiation Effects on Electronics***

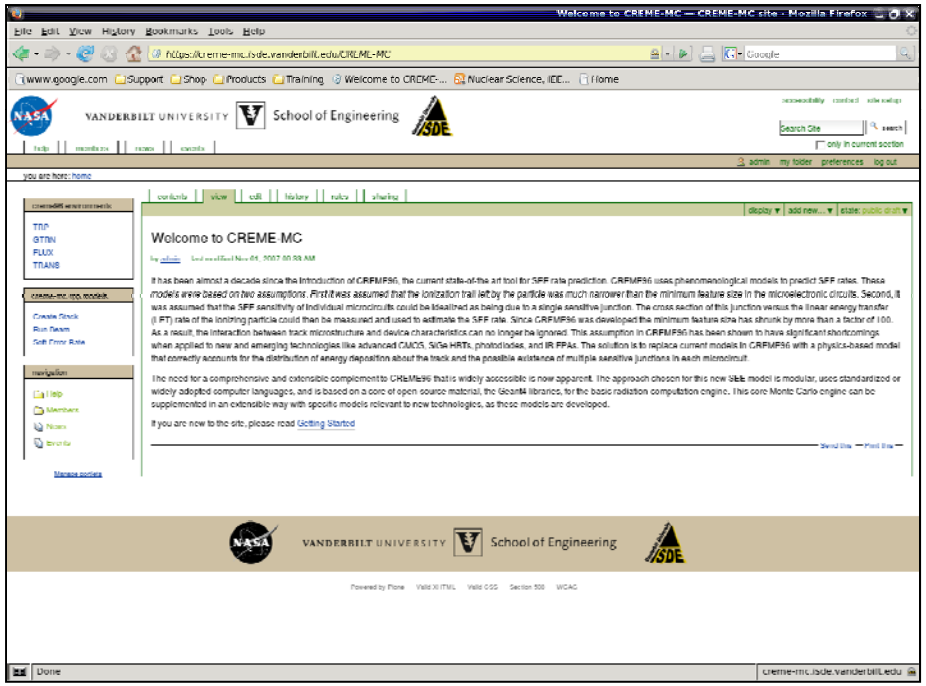
This subproject is to develop an on-line tool to replace CREME96. It will used primarily to select parts that are sufficiently radiation hard for their intended applications are spacecraft electronics. The code will provide estimates of total dose and single event effect rates.

Key Accomplishment/Milestone:

The alpha version of the CREME-MC was online and available to NASA and Vanderbilt University personnel on 11/1/07.

Significance:

Represents a highly functional release of the system with significant documentation. The site contains all of the low level functions allowing concentration on advancing the state of the art in soft error rate predictions for space.



Shown: CREME-MC website available at http://creme-mc.isde.vanderbilt.edu

Completion of Legacy CRÈME86 & CRÈME96 Codes Available On-line

Objective:

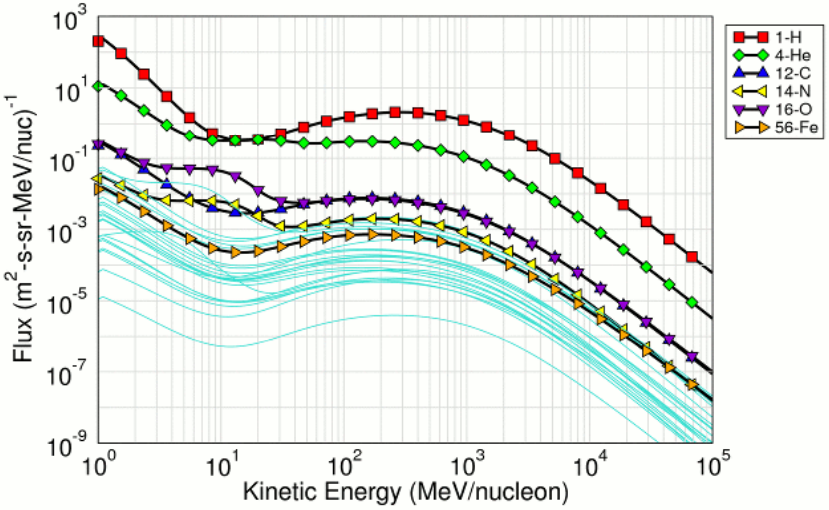
To preserve access to the legacy codes of CREME86 and CREME96 on the new modeling website.

Key Accomplishment / Milestone:

- **Completion of Legacy CREME86 and CREME96 codes Available On-line (Dates: 12/09 and 3/09, respectively)**
- **Make CREME86 available on-line from a US server by hosting it at Vanderbilt University.**
- **Host CREME96 at Vanderbilt University in order to preserve access to it after the Naval Research Lab host is deactivated.**

Significance:

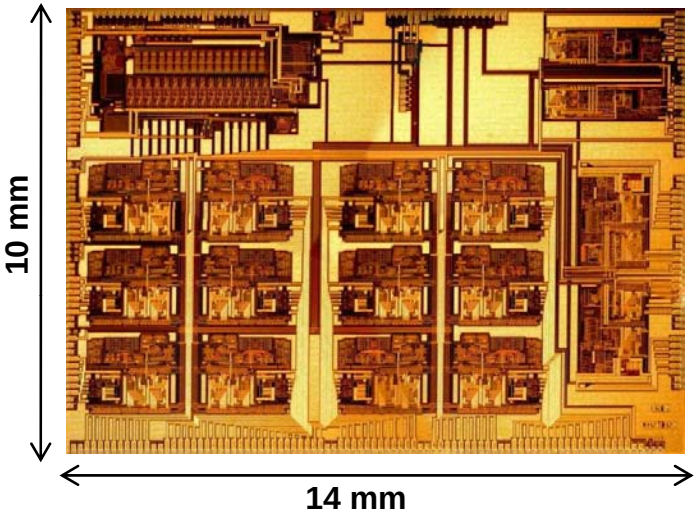
- **All the heritage CREME tools for radiation effect prediction are now available on a single WWW site that will also host the newer software version, CRÈME-MC, which is being developed by the Modeling of Radiation Effect on Electronics (MREE) task.**
- **This permits linkage between heritage and new models plus allows easy interchange of model and environmental information between the tools.**



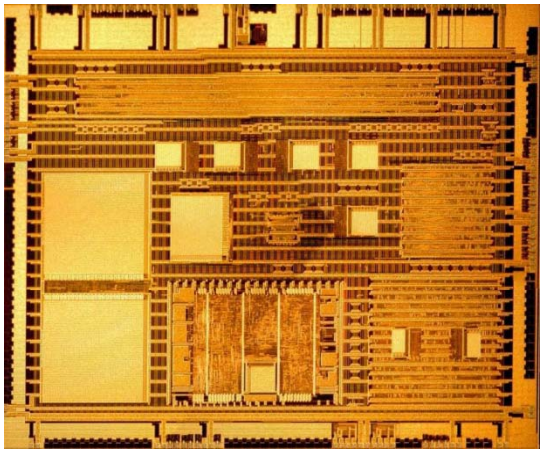
The plot above features elemental differential energy spectra during a solar-quiet period near solar minimum for many elements. The spectra includes galactic cosmic rays, anomalous cosmic rays, and solar energetic particles from solar outbursts. CRÈME codes use these spectra to define the environment appropriate for modeling spacecraft electronics.

SiGe FY09 Accomplishments

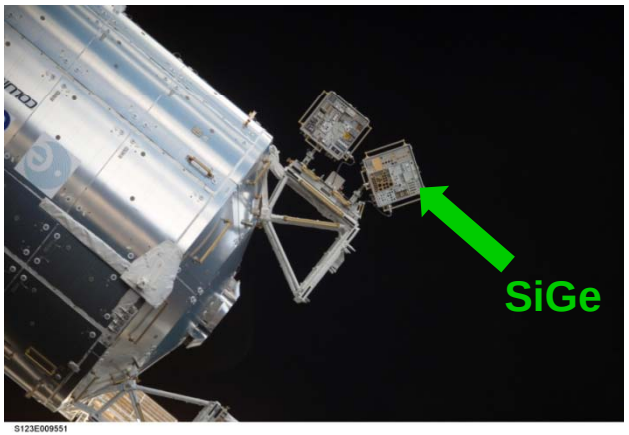
CRYO-5 SiGe Analog ASIC



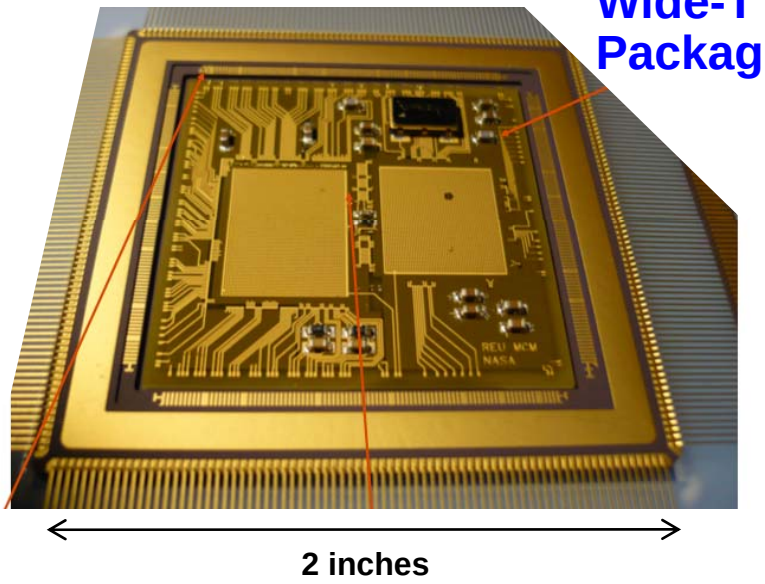
CRYO-5 SiGe Digital ASIC



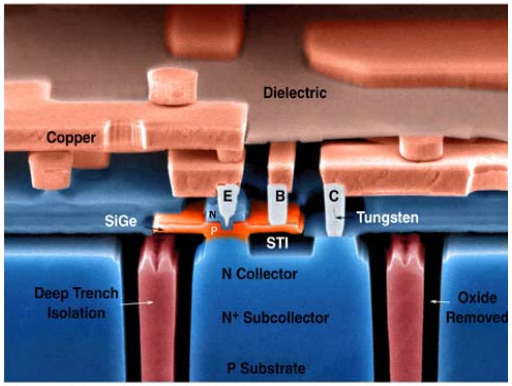
ISS Experiments (MISSE-6,7)

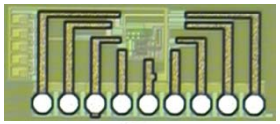


Wide-T Packaging



SiGe Infrastructure Development



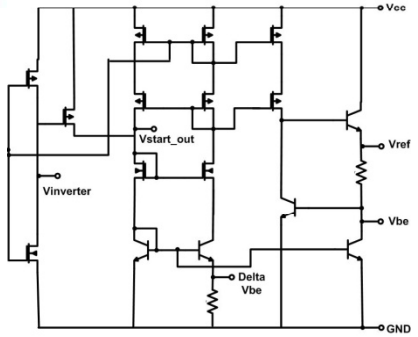


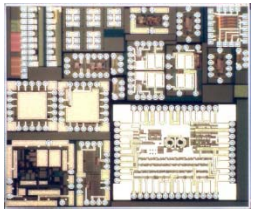
Extreme Environment Toolkit

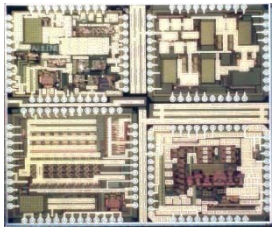
ModLyng IME

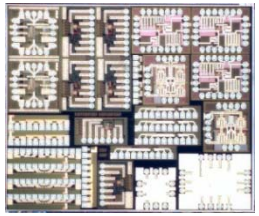
Compact Model Toolkits

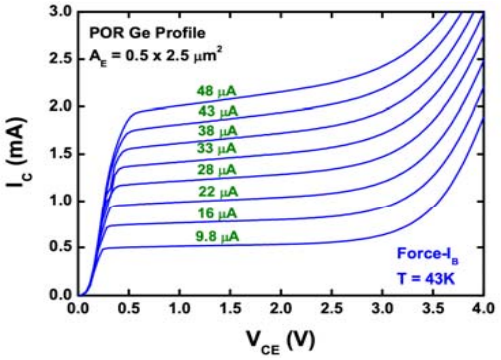
- Mission Profile
- System Level Specification
- Sensors/Actuators/ Loads/Package
- SoC Architecture
- SoC Definition
- Channel Definition
- Circuit Design
- SiGe Process Design Kit
- SiGe Device Characterization
- SiGe Device Modeling
- Temperature Sensitivity
- Radiation Sensitivity
- Physics of Failure

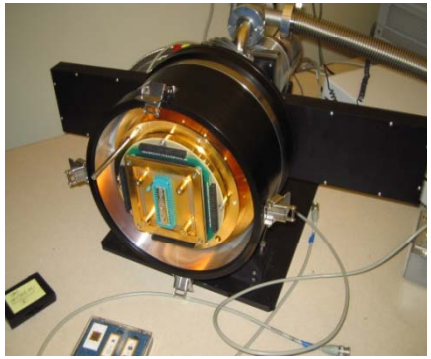


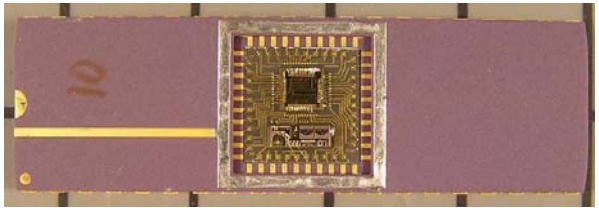


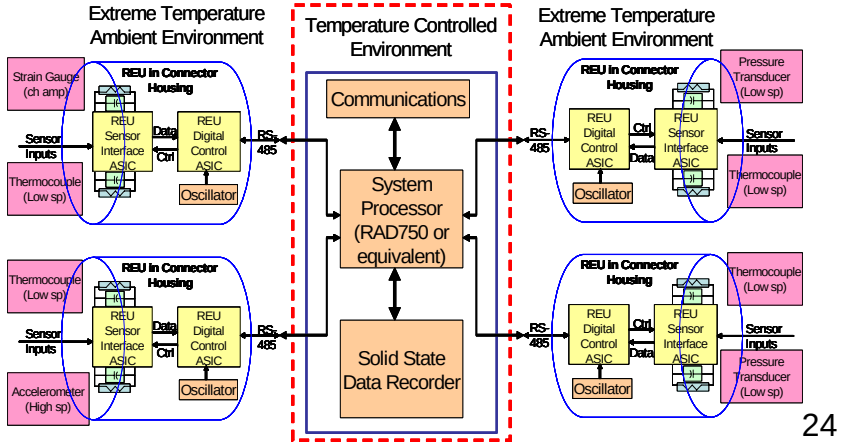




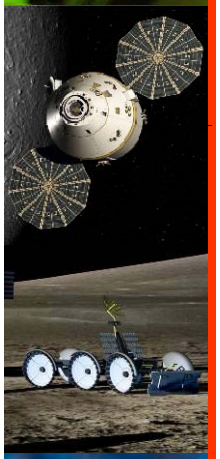




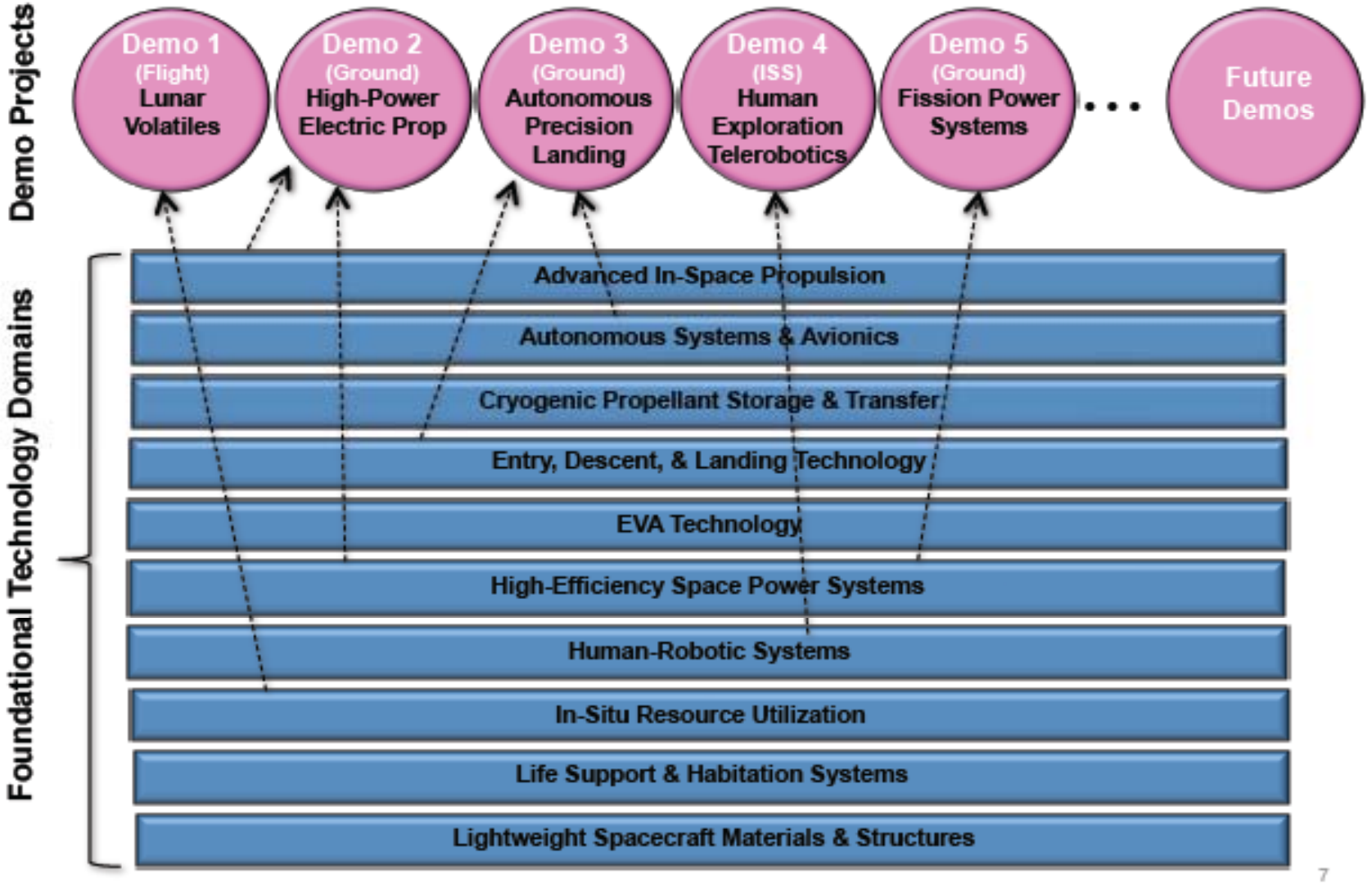




What Happens Next?



ETDD Program Structure



Summary

- **All spacecraft are affected by the radiation environment**
  - Spacecraft traveling beyond low-earth orbit must deal with a potentially extreme radiation environment.
- **The AAPS project has been a successful force in developing and delivering advanced avionics for the Constellation Program.**
- **Three tasks started under AAPS,**
  - HPP
  - MREE
  - RC

  …will continue into FY11 under the new Exploration Technology Development and Demonstration program within the Autonomous Software and Avionics (ASA) project.