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NASA Goddard Space Flight Center

EVALUATION OF 3D PLUS PACKAGING TEST STRUCTURES FOR NASA GODDARD SPACE FLIGHT CENTER

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Abstract:
Environmental tests were performed on packaging test structures designed and manufactured for ESA and CNES by 3D Plus Electronics. The design provided circuit elements that acted as thermal, mechanical and moisture sensors. Other design features showed the compatibility of the packaging with chip passives, bare electronic dice and plastic encapsulated microcircuits packaged together in an innovative, stacked multichip module. The NASA GSFC testing augmented long duration testing on the same units carried out by ESA and CNES. The NASA portion demonstrated packaging stability over temperature, in moisture, with voltage stress, in shock and in vibration environments.

1. Background:

Electronics packaging in the commercial world has seen innovations that have revolutionized the industry. NASA GSFC is constantly exploring advanced electronic packaging techniques so that they too can achieve a higher degree of miniaturization, thereby contributing volume and weight reduction to advanced spacecraft systems. In this vein, test vehicles were chosen for evaluation of stacked Multi-Chip-Modules (MCMs) developed by the company 3D Plus Electronics. NASA GSFC was able to leverage off of an evaluation funded and managed by CNES and ESA by obtaining pieces of a production run of packaging test vehicles. ESA and CNES were planning to perform long duration ruggedness testing. To enhance ESA and CNES' results, NASA performed analyses and environmental tests not included in their test program. The test vehicles were named CESAR by 3D Plus.

2. Design Concept:

3D Plus' product is a packaging technology based on plastic encapsulation of stacked up layers of electronic devices mounted to metallized polyimide film substrates (*Fig. 1*). The key elements in the manufacturing process are: film design, population of the film, stack up and encapsulation, sawing, plating and scribing. Various types of pin-outs are offered from Pin-Grid-Array (PGA) to Ball-Grid-Array (BGA). The test vehicles evaluated here were lead frame, flat-pack type, on a 25 mil pitch.

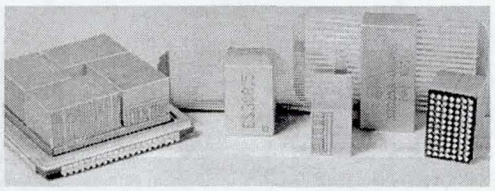


Figure 1. 3D Plus Stacked Multichip Modules
(Photo Courtesy 3D Plus Electronics)

3D Plus' primary products are memory modules. Custom modules have also been produced including test vehicles (daisy chain cubes for JPL, thermal cubes for JPL and the CESAR cube for ESA). Other custom cube designs have included a Temic microcontroller, an optical iris, an FPGA and a DC/DC converter. The electronic parts inside the cube can be bare electronic dice, packaged parts (plastic or ceramic) or chip passives (capacitors and resistors). They have several package designs, which enable the use of high-speed components, very small plastic encapsulated microcircuits (PEMs), and heavier and hotter ceramic packaged parts. 3D Plus' miniaturization technique can provide an 80% reduction in footprint.

2.1 Film Design:

Metallized flexible films are used for the layer substrates. They can be polyimide or FR4 BT material. The metallization is Cu+Ni+Au and is a minimum of 0.127 mm in trace width and pitch. 3D Plus subcontracts the production of the films. The metallization pattern on the films allows interface between the internal part and the final, external surface of the cube. This is the tertiary interface counting from the board into the part (the bond wire being the fourth level of interconnect in the case of the use of bare dice). The film metallization must provide a multi-bond surface: wire bondable, epoxy bondable and solderable. This allows mixing of dice, packaged parts and chip passives. Mechanical

features in the film allow proper stack-up of the module and alignment at the secondary interface. traces to be 0.8 mΩ/square.

2.2 Population of the Films:

The films are populated with packaged parts, dice and/or chip passives. The wire bonds are glob topped. Population and glob topping is done at the 3D Plus facility. The populated films are then electrically tested and screened in accordance with customers' requirements. This step allows the use of known-good-die in the finished multichip module which is a great assurance enabler.

2.3 Stack Up, Encapsulation and Sawing

Stack up and encapsulation is done at the 3D Plus facility. The standard products are 4 and 8 layers high. The evaluation cube discussed here is 10 layers high. The lead frame is installed during this step and can be PGA or flat pack. BGA is also available. The encapsulation with Hysol FP4450 followed by sawing, brings the layers together and exposes the secondary interconnects at the external faces of the module. The sawing process cuts through the encapsulation and through the metallization tracks on the flex substrates making the secondary interconnects flush with the external layers of the cube.

2.4 Plating and Scribing

The final manufacturing step is plating and scribing. Plating is also a subcontracted process. Gold is plated over nickel. The plating process effectively connects all of the secondary interconnects which are exposed on each of the vertical external faces of the cube. Following plating, tracks are scribed down the side faces to arrange connection between the secondary interconnects and the pins on the lead frame, or BGA, and to isolate secondary interconnects from each other (some of the secondary interconnects may not be separated from each other with a scribe line when bussing is desired). The scribing process is done at the 3D Plus facility using a computer-controlled laser. The scribe design makes use of real estate made available by "no connect" pins on the lead frame to provide individual control to each of the layers. 3D Plus reports the limit to the scribing process as a minimum width of 0.380 mm.

3. CESAR Test Vehicles

The testing and the design of the evaluation structures was intended to explore the ability of the process to produce rugged, stacked, electronic devices which survive typical conditions of space Measurement of films, which were delivered as part of the CESAR project, found the resistance of the flight use. The layers of the stack include special devices that are used to detect:

1. moisture ingress
2. torsional stress during temperature changes
3. the effect of the stacking on chip resistors and capacitors mounted on the same layer as silicon devices
4. the effect of the stack design on typical memory chips in the packaged form
5. the ability of the cube to dissipate heat with and without an internal heat sink.

Table 1 describes the composition of the layers. Figure 2 shows the arrangement of the components in the cube. ESA and CNES used 22 units for their portion of the evaluation and NASA GSFC used 9. Two sets of unencapsulated, populated, layers were provided to NASA GSFC to facilitate testing and final analyses.

Table 1. Composition of the 10 Layer Test Structure

Layer	Devices
10	Corrosion chip and contact continuity pattern
9	Strain gauge and 5kΩ chip resistors
8	DRAM TSOP with all leads terminated inside of the cube
7	DRAM TSOP with half of the leads terminated inside of the cube and half terminated at the cube side face, 22nF ceramic chip capacitor and two 10 nF ceramic chip capacitors
6	Thermal chip with no heat sink
5	Strain gauge, 100 kΩ chip resistors, 200 daisy chained wire bonds
4	Thermal chip with heat sink
3	DRAM TSOP with half of the leads terminated inside of the cube and half terminated at the cube side face, two 100 nF ceramic chip capacitors and two 10 uF tantalum capacitors
2	DRAM TSOP with all leads terminated inside of the cube
1	Corrosion chip and contact resistance pattern

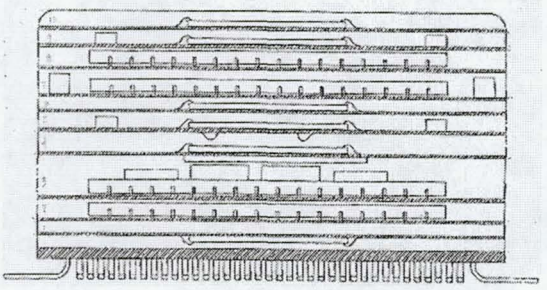


Figure 2. CESAR Component Arrangement

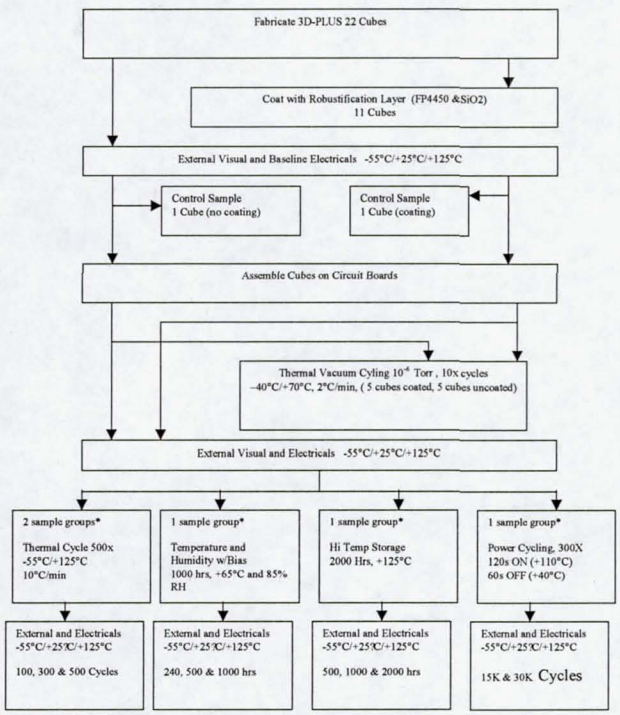
The DRAM devices in layers 2, 3, 7 and 8 were Samsung 16M x 4 bit KM44V16104A (4k refresh). The tantalum capacitors are 10 uF/10V and 2.2 uF/10V. The ceramic capacitors are 100 nF/50V, 22nF/50V and 10 nF/50V. The resistors are 5kΩ/125mW, 100 kΩ/125mW, 5kΩ/250mW and 100kΩ/250mW. The corrosion chip and the thermal chip were custom made for this evaluation. The strain gauge was identified by 3D Plus as made by ACM. Part characteristics, detailed pin assignments and internal connection drawings were provided to NASA GSFC by 3D Plus.

4. Testing:

4.1 Test Plans

ESA and CNES managed the portion of the test plan that included the following tests and shown in Figure 3:

a. preconditioning thermal cycling in vacuum
b. 500x thermal cycling (-55°C to +125°C)
c. temperature humidity bias (+85°C/85%RH/1000 hrs)
d. high temperature bake (+125°C, 2000 hrs)
e. power cycling (30k x on/off, 120 sec on +110°C, 60 sec off +40°C)



* *1 sample group = 1 coated TV conditioned, 1 uncoated TV conditioned, 1 coated, no conditioning, 1 uncoated, no conditioning*

Figure 3. ESA and CNES Test Plan

NASA/GSFC provided the testing that is detailed in Figure 4 and consists of:

a. CSAM
b. thermal conditioning (+125°C, 48 hrs)
c. voltage conditioning (+125°C, 320 hrs)
d. thermal characterization
e. vibration (sine & random)
f. mechanical shock
g. 85% humidity / 85°C
h. finite element modeling

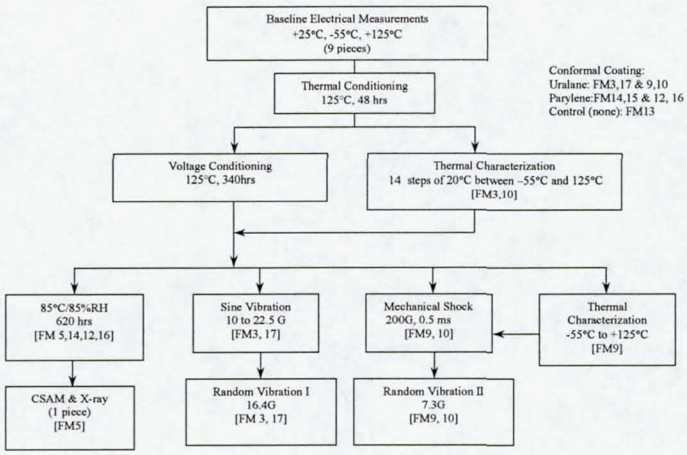


Figure 4. NASA GSFC Test Plan

4.2 Test Unit Serialization and Sample Preparation

Each test unit was serialized as follows: FM13 (control), FM3, FM5, FM9, FM10, FM12, FM14, FM16, and FM17. FM13 occupied a board by itself and it was not conformally coated (Assembly 1). FM 14 and 15 were mounted to a test board and then conformally coated with Parylene C (Assembly 2). FM12 and FM16 were mounted to a test board and also conformally coated with Parylene C (Assembly 3). FM3 and FM17 were mounted to a test board and then conformally coated with Uralane (Assembly 4). FM9 and FM10 were mounted to a test board and also conformally coated with Uralane (Assembly 5). Standard practices used for flight hardware assembly were applied.

4.3 Electrical and Environmental Test Conditions.

4.3.1 Baseline Electricals:

Electrical tests were done to establish a baseline of performance after every evaluation step, using the bias conditions and circuits recommended by 3D Plus and CNES. Three temperature electricals were only taken at the beginning of the evaluation (this does not include the thermal characterization test). Direct Current (DC) parameters were measured for each of the components on the layers. Testing was automated using LabView allowing each

measurement to be made on each layer at each electrical test step. A data review performed during the evaluation confirmed that our test circuits were achieving the same range of measurements with the same approximate accuracy as was being achieved in the CNES/ESA testing being done in France. The pass/fail criteria are shown in Table 3.

Table 3. Pass/Fail Criteria for Electrical Tests

Test No.	Test Name	Number of Elements Measured Per Pass	Passing Range	Units
1	Corrosion Module Resistance	6	712 - 788	Ohms
2	Corrosion Trace Isolation	2	<1	mAmps
3	Film Contact Resistance	4	< 1	Ohms
4	Daisy Chain Continuity	1	< 1	Ohms
5	Strain Gauges	8	2565 - 2835	Ohms
6	Thermal Monitor			
a	Control	4	300	Ohms
b	Forward voltage (loaded and unloaded)	12	0.5 to 1	Volts
c	Reverse Current (loaded and unloaded)	12	< 100	nAmps
7	Test number not used			
8	Capacitor Blocks			
a	Layer 3	1	40 - 55	nFarads
b	Layer 7	1	3 - 4	uFarads
9	Resistance Blocks			
a	Large valued layer	1	22500 - 27500	Ohms
b	Small valued layer	1	1125 - 1375	Ohms
10	DRAM Quiescent Currents			
a	Standby current	2	< 2	mAmps
b	Enabled current	2	< 480	mAmps

4.3.2 Thermal Characterization:

Electrical characterization of the cubes was done to perform real time monitoring of the various test layers during increasing and decreasing thermal stress. The parts were exposed to the temperatures of 20°C intervals between -55°C and +125°C. The transition rate between each temperature was 5°C/minute. Electrical measurements were taken following a 10 minute dwell at each temperature.

4.3.3 Voltage Conditioning: A circuit was set up to bias as many of the internal components as possible. The biased parts were baked at 125°C for 340 hours.

4.3.4. 85°C/85% RH. Samples was exposed to the heat and humidity test specified in MIL-STD-202, Method 103 to quantify the ability of Parylene C to protect the parts from moisture damage. The duration was 640 hours.

4.3.5 Sine Vibration.
Sine vibration was done in accordance with MIL-STD-202, Method 201, Condition A. Figure 6 shows the sine vibration profile used.

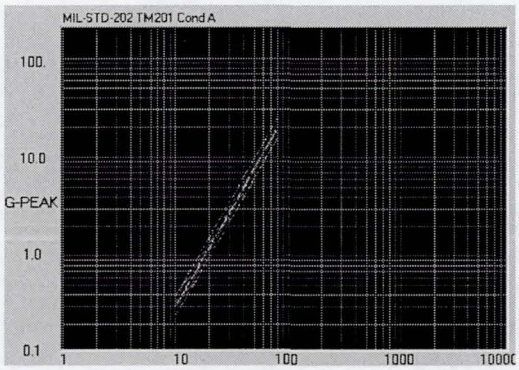


Figure 5. Sine Vibration Spectrum – test setting and achieved profile

4.3.6 Mechanical Shock
Mechanical shock was performed in accordance with MIL-STD-883, Method 2002, with a peak level of 200g and a pulse duration of 0.5 ms. Figure 6 shows that shock profile was applied both in the upward and downward direction. The parts were fixtured and tested in the X,Y and Z axis as well. All layers were electrically tested after the test.

4.3.7. Random Vibration
Random vibration testing was performed in accordance with MIL-STD-883, Method 2026 in the X,Y and Z-axes. The 4.5" x 4.5" test board was rigidly mounted at the corners and at the center to limit board effects. Random Vibration I uses Condition E (16.4 G) and Random Vibration II used Condition B (7.3 G). Figures 7a and 7b show the test conditions and the resulting profiles.

4.3.8. CSAM and DPA
Scanning acoustic microscopy was employed to understand if the tool was at all useful with this type of layered, PEMs-like device. A DPA was performed by CNES on units FM3 and FM17 in which anomalies were found.

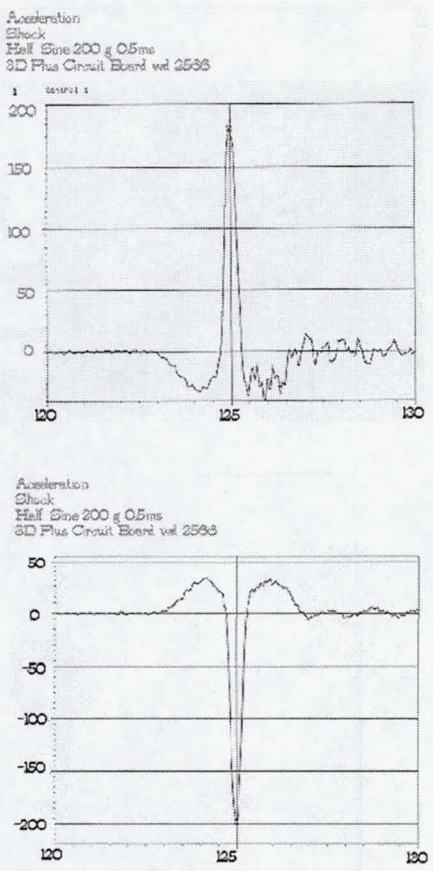


Figure 6. Shock Profile

5.0 Finite Element Analysis:

Finite element modeling was used to show theoretical stress caused to the part due to static and dynamic vibration and thermal stress and thermal cycling. This analysis was performed for the evaluation stack design prior to testing. The results of this analysis gave cause for changing some of the test conditions planned resulting in the tests described above. Staking at the corners of the cubes was used to give the parts a better chance of passing the Vibration I test.

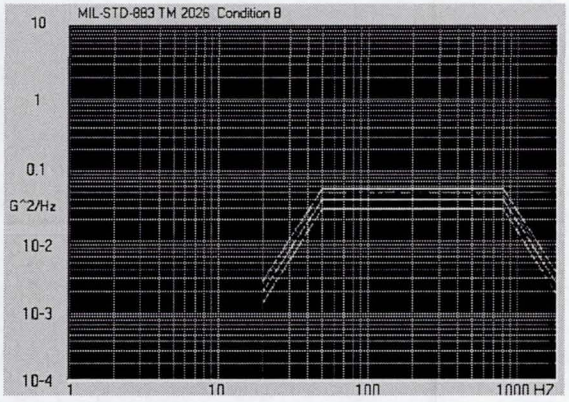


Figure 7a. Random Vibration I – test and resulting profile

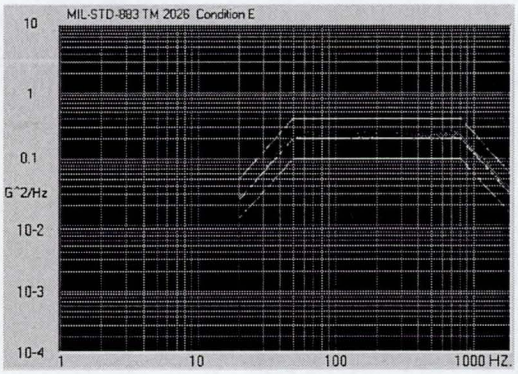
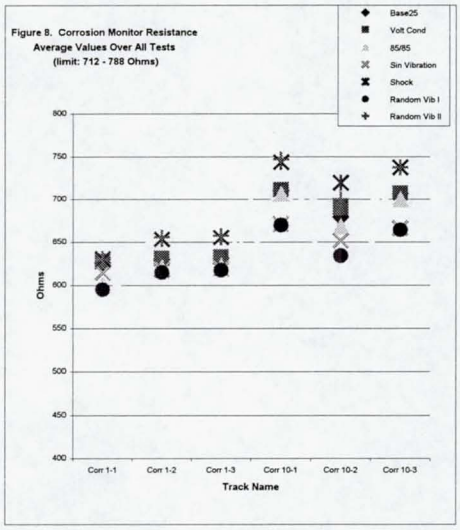


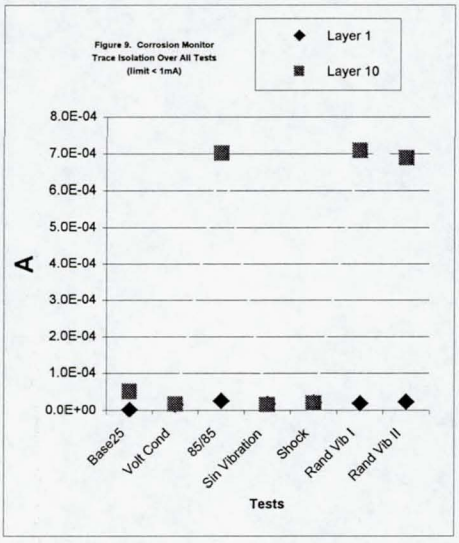
Figure 7b. Random Vibration II – test and resulting profile

6.0 Results

6.1 Electrical Data Graphed

The data was collected by test unit (FM#), by device (layer) and by test. Figures 8 through 17 show 10 out of the 111 graphs generated for the final NASA report.





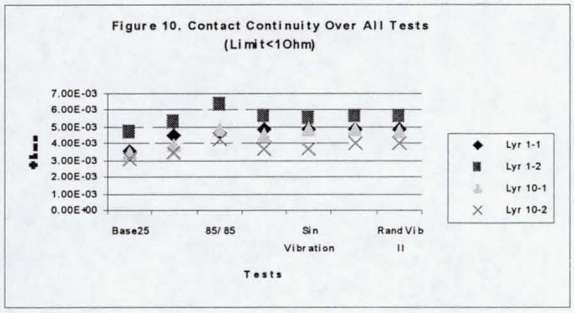


Figure 10. Contact Continuity Over All Tests
(Limit<1Ohm)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Base25
85/ 85
Sin Vibration
Rand Vib II
Tests
Lyr 1-1
Lyr 1-2
Lyr 10-1
Lyr 10-2

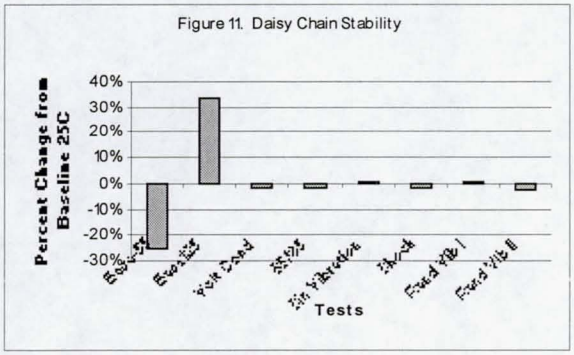


Figure 11. Daisy Chain Stability
Percent Change from Baseline 25C
40%
30%
20%
10%
0%
-10%
-20%
-30%
Tests

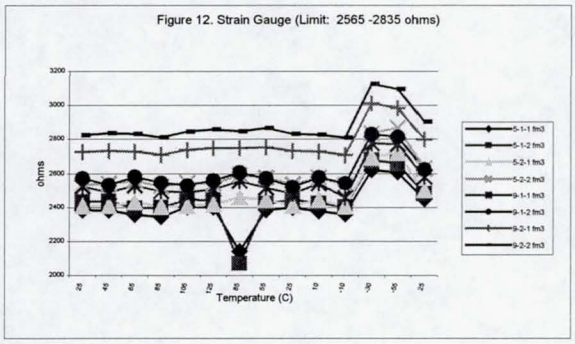


Figure 12. Strain Gauge (Limit: 2565 -2835 ohms)
ohms
Temperature (C)

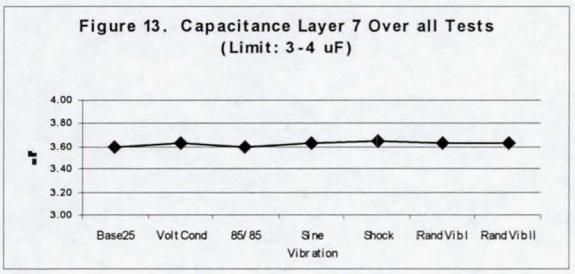


Figure 13. Capacitance Layer 7 Over all Tests
(Limit: 3-4 uF)
4.00
3.80
3.60
3.40
3.20
3.00
Base25
Volt Cond
85/ 85
Sine Vibration
Shock
Rand Vib I
Rand Vib II

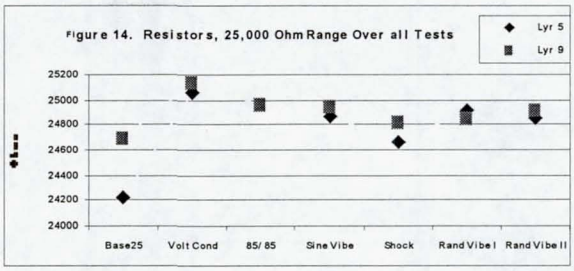


Figure 14. Resistors, 25,000 Ohm Range Over all Tests
Lyr 5
Lyr 9
25200
25000
24800
24600
24400
24200
24000
Base25
Volt Cond
85/ 85
Sine Vibe
Shock
Rand Vibe I
Rand Vibe II

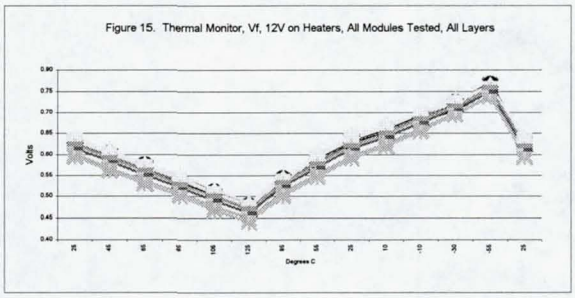


Figure 15. Thermal Monitor, Vf, 12V on Heaters, All Modules Tested, All Layers
Volts
Degrees C

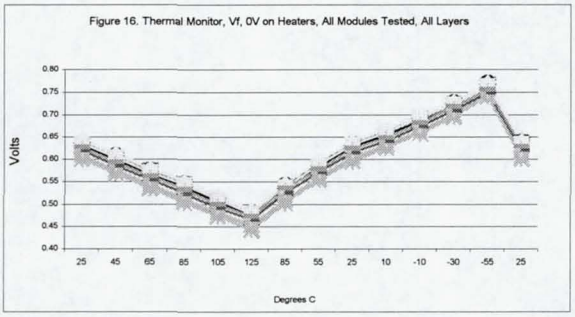


Figure 16. Thermal Monitor, Vf, 0V on Heaters, All Modules Tested, All Layers
Volts
0.80
0.75
0.70
0.65
0.60
0.55
0.50
0.45
0.40
25 45 65 85 105 125 85 55 25 10 -10 -30 -55 25
Degrees C

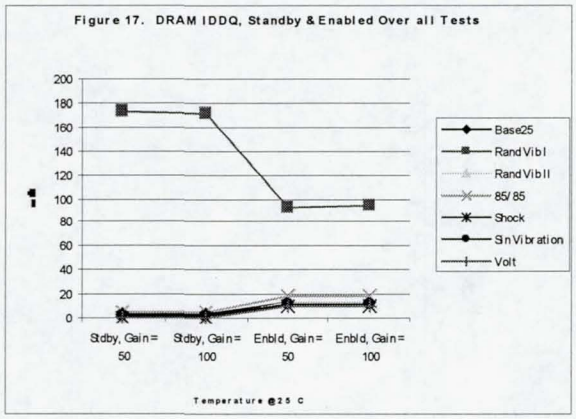


Figure 17. DRAM IDDQ, Standby & Enabled Over all Tests
200
180
160
140
120
100
80
60
40
20
0
Stdby, Gain= 50
Stdby, Gain= 100
Enbld, Gain= 50
Enbld, Gain= 100
Temperature @25 C
Base25
Rand Vib I
Rand Vib II
85/ 85
Shock
Sin Vibration
Volt

6.2 Analysis of the Electrical Measurement Results

All of the data, except three points, was within family and agreed with that collected by ESA. The three out-of-family data points were as follows:

1. The measured reverse current on diode 3, layer 6 of device FM17, indicated that it was shorted. This was an "as received failure". The cause the failure was not pursued.

2. DRAM Iddq, in device FM3 and FM17: This measurement combined Iddq for all four devices in the cube so it was unclear which one or more failed.

The data showed that the failure(s) in the DRAM(s) in FM3 started to occur intermittently from the end of the thermal characterization test though the middle of the vibration testing. The failure became severe and permanent at the final measurement following the sine vibration test. The DPA showed signs of electrical overstress at an input diode in all four of the DRAM in the FM17 device. It is hard to understand how this could have occurred as the setup was not touched or changed between temperatures. In any case, the failure does not have a signature normally associated with a failure of the packaging and is certainly an artifact of a localized, heating event. This same type of failure was encountered during the CNES/ESA testing.[1/]

The data for the DRAM in FM17 showed abrupt change in Iddq following the sine vibration test. The appearance of the failed site on level 7 was noted by CNES as "Fusion of the resin with the silicon and aluminum". This defect was not noted on any of the three other DRAM layers. Again localized heating due to electrical overstress may have been the cause though the artifact is not clearly understood.[2/]

3. Strain Gauge element 1 and 2 on layer 9, device FM5: This same device failed in some of the ESA samples. A DPA was performed which found metallization defects on the die, believed to be unrelated to the packaging [1/].

The following was observed in the data:

1. Corrosion monitor resistance: The data was consistent over the testing, though some of the tracks on layer 10 baselined higher than those on layer 1. Layer 10 was also slightly more sensitive to moisture.

2. Corrosion monitor isolation: The data was all within specification though layer 10 seemed to be more sensitive to moisture (85/85 test). The sensitivity to the vibration tests may have also been moisture related as those tests were conducted during the most humid time of the year.

3. Contact Continuity: All measurements showed continuous circuits with no significant sensitivity to moisture.

4. Daisy Chain Wire Bonds: All measurements showed continuous circuits with no permanent sensitivity to moisture or other environment changes.

5. Strain Gauge: The dice in FM3 showed sensitivity to temperature while the dice in FM9 and FM10 did not. No failure trends were encountered over the mechanical and moisture testing. FM5 had a failure during baseline electricals and voltage conditioning (see above) which is considered to be related to an as-received die-level defect.

6. Thermal Monitor
a. Forward Voltage (Vf), with 0V and 12V on Heaters: No out of family data was encountered. No difference could be detected between the layer with and without a heat sink.
b. Reverse Current ($I_{R)}$, with 0V and 12V on Heaters: One device was received in a failed condition (see above). For the remaining data, no out-of-family data was encountered. No difference could be detected between the layer with and without a heat sink.

7. Capacitors: No significant change occurred over all of the tests.

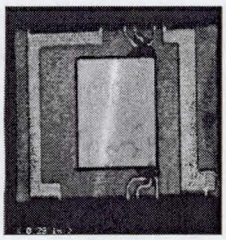
8. Resistors: All measurements were within specification.

9. DRAM: A failure was apparent following Thermal Characterization and Sine vibration which continued through the subsequent Random Vibration I test (noted above). All other measurements were within specification.

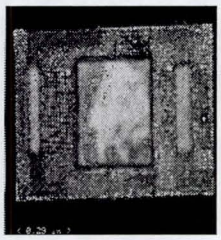
6.3 CSAM

It was fairly difficult to apply CSAM because the part was very thick with so much area of interest through the z-axis. Once a proper location could be identified, good images of the polyimide film, the metallization, glob top and the die could be discerned. We were not able to interpret the presence or absence of voids under the die. CSAM may be useful prior to a planned FA or DPA but was not found to be conclusive for a non-destructive evaluation tool in this case. Figures 8a through 8d show examples of CSAM images produced at NASA GSFC of the CESAR device.

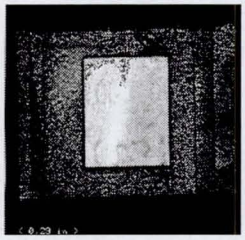
7.0 Finite Element Analysis
For brevity, the details of the Finite Element Analysis (FEA) are not given here, but only a summary and the results. The total power dissipation for the cube



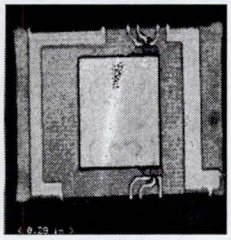
8a. CSAM Overall 1



8b. CSAM Below Die



8c. CSAM Die Surface



8d. CSAM Overall 2

was calculated from the characteristics reported by 3D Plus as 2.968W. The printed circuit board was considered the heat sink or reference temperature. The maximum temperature rise at steady-state was determined to be 50.1°C, requiring the maximum circuit card temperature to be 65°C (all internal devices on simultaneously).

The analysis of the dynamic vibration case was performed assuming a printed circuit board with the same dimensions used in the testing (4.5" x 4.5" x 0.062", mounting points on corners and in center). Tin-Lead solder (63:37) was assumed. Only one module was assumed to be on the board (due to RAM limitations in the FEA computer). The higher Vibration I level was used (16.4 Gs). The analysis resulted in four resonant frequencies for the z-plane (perpendicular to the mounting plane):

F1 = 1052 Hz F3 = 1685 Hz
F2 = 1520 Hz F4 = 1874 Hz

With these resonances, the highest stress occurs at F1, at the corner of the device, with a value of 10.6 Mpa. The 3σ RMS von Mises stress is 34.68 MPa, which is 2.15 times the yield strength of the solder joint. This analysis indicated that:

1. A second vibration test should be done, at with a lower overall RMS force to demonstrate the cube's ability to pass a less rugged test, but one still very much used by NASA projects.
2. It would be more useful to see if a staked cube (using normal flight hardware materials and processes) could pass the Vibration II test rather than to risk damaging the test units in a test that analysis indicated they could not pass without staking.

8.0 Conclusions

The 3D Plus packaging technology provides very high density and stable performance in rugged environments. The parts are suitably rugged and stable with respect to high and low temperature, humidity, shock and vibration. Care must be given to properly stake the parts when they are as high as these evaluation cubes. The data did not indicate that there was a need for special moisture protection beyond normal conformal coating (parylene or Uralane) though these being non-hermetic, care should still be given to keep the parts as dry as possible to ensure long life. No significant performance difference was noted between the layer with the heat sink and the one without the heat sink [The results for the temperature cycling and long term temperature tests, performed by CNES and not presented here, were similarly stable for all of the layers]. The test vehicles were exposed to severe environmental stresses and thousands of passing data points were collected indicating that it is highly suited for use in extreme environments where normal derating and protection practices, for temperature and moisture, are used.

References:

1/ Analyse de Defaillance sur les Cubes CESAR FM4 et FM36, A. Wislez, Laboratoire Central des Industries Electriques, 2001
2/ Analysis Report, CESAR Cube 3D FM17 and FM3, RAAE-04.03, F. Courtade, CNES, 2002

Recognition:

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