NASA-DoD LEAD-FREE ELECTRONICS PROJECT: OVERVIEW

Kurt Kessel
ITB, Inc.
NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center
Kennedy Space Center, FL, USA
kurt.r.kessel@nasa.gov
{On behalf of the NASA-DoD Lead-Free Electronics Project Consortium}

ABSTRACT
Original Equipment Manufacturers (OEMs), depots, and support contractors have to be prepared to deal with an electronics supply chain that increasingly provides parts with lead-free finishes, some labeled no differently and intermingled with their SnPb counterparts. Allowance of lead-free components presents one of the greatest risks to the reliability of military and aerospace electronics. The introduction of components with lead-free terminations, termination finishes, or circuit boards presents a host of concerns to customers, suppliers, and maintainers of aerospace and military electronic systems such as:

1. Electrical shorting due to tin whiskers
2. Incompatibility of lead-free processes and parameters (including higher melting points of lead-free alloys) with other materials in the system
3. Unknown material properties and incompatibilities that could reduce solder joint reliability

As the transition to lead-free becomes a certain reality for military and aerospace applications, it will be critical to fully understand the implications of reworking lead-free assemblies.

Key words: lead-free, reliability, harsh environments testing, aerospace

BACKGROUND
The NASA-DoD Lead-Free Electronics Project builds on the results from the Joint Council on Aging Aircraft/Joint Group on Pollution Prevention (JCAA/JG-PP) Lead-Free Solder Project, the first group to test the reliability of lead-free solder joints against the requirements of the aerospace and military community, while focusing on the rework of SnPb and lead-free solder alloys and includes the mixing of SnPb and lead-free solder alloys. The majority of testing being conducted for this effort will mirror the testing completed for JCAA/JGPP LFS Project. Some changes were made in order to optimize the usefulness of the data.

OBJECTIVE
In response to concerns about risks from lead-free induced faults to high reliability products, the NASA-DoD Lead-Free Electronics Project Consortium outlined a multi-year project to provide manufacturers and users with data to clarify the risks of lead-free materials in their products. The project also provides useful data to component manufacturers supplying to high reliability markets. The project was launched in November 2006. The primary technical objective of the project is to undertake comprehensive testing to generate data on failure modes / criteria to better understand the reliability of packages (e.g., thin small outline package, ball grid array, plastic (dual inline package), chip scale package, quad flat pack (no leads) assembled and reworked with lead-free alloys and with mixed (lead/lead-free) alloys).

The intended goal of this project is to:

1. Determine the reliability of reworked solder joints in high-reliably military and aerospace electronics assemblies.
2. Assess the process parameters for reworking high-reliability lead-free military and aerospace electronics assemblies.

Develop baseline recommendations for process guidelines and a risk assessment for assembling high-reliability lead-free military and aerospace electronics assemblies.

PROCEDURES
Test Vehicle
The test vehicle is a printed wiring assembly (PWA), designed to evaluate solder joint reliability. Test vehicle raw boards comply with IPC-6012 (Qualification and Performance Specification for Rigid Printed Boards), Class 3, Type 3. Test vehicle size is 14.5 X 9 X 0.09 inches with six 0.5-ounce copper layers. The design incorporates components representative of the parts used for military and aerospace systems and is designed to reveal relative differences in solder alloy performance. A variety of plated through-hole (PTH) and surface mount technology (SMT) components are included. All components are "dummy" devices with pins internally daisy-chained and contain simulated die. The circuit board was designed with daisy-chained pads that are complementary to the components. Therefore, the solder joints on each component will be part of a continuous electrical pathway that can be monitored during testing by an event detector (Anatech or equivalent). Failure of a solder joint on a component will break the continuous pathway and be recorded as an event. Each

component has its own distinct pathway (channel). Figure 1 illustrates the test vehicle design.

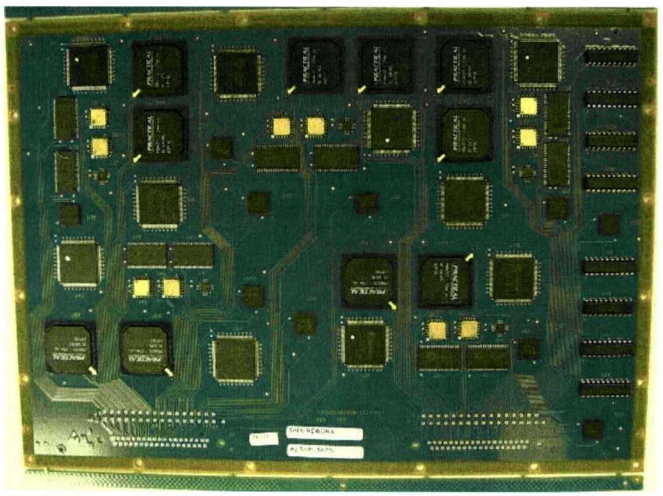


Figure 1 Test Vehicle Design

All test vehicles were assembled using immersion silver (Ag) and a limited number of electroless nickel / immersion gold (ENIG) finished glass fiber (GF) laminate (IPC-4101/26) printed circuit boards with a glass transition temperature, T_g, of 170°C minimum and categorized as either "Manufactured" or "Rework". "Manufactured" test vehicles represent printed wiring assemblies newly manufactured for use in new product. Test vehicles being subjected to thermal cycle and combined environments testing will include forward and backward compatibility. Test vehicles assembled for vibration and mechanical shock will not include forward and backward compatibility. "Rework" test vehicles represent printed wiring assemblies manufactured and reworked prior to being tested. Solder mixing will be comprised of forward and backward compatibility:

1. Forward compatibility is a SnPb component attached to a printed wiring assembly using lead-free solder with a lead-free profile.
2. Backward compatibility is a lead-free component attached to a printed wiring assembly using SnPb solder with a SnPb solder profile.

In addition to the NASA-DoD Lead-Free Electronics Project test vehicles, Crane Division, Naval Surface Warfare Center, a NASA-DoD Consortium member, added 30 test vehicles to the NASA-DoD project in support of their Naval Supply Command (NAVSUP) sponsored "Logistics Impact of Lead-Free Circuits/Components" project. The primary purpose of the 30 test vehicle add-on was to perform multiple pass SnPb rework 1 and 2 times on random Pb-free DIP, TQFP-144, TSOP-50, LCC and QFN components from SAC305 and SN100C soldered assemblies.

The reworked test vehicles will be integrated into the NASA-DoD Lead-Free Electronics Project -55°C to +125°C thermal cycling testing (Rockwell Collins; Cedar Rapids, Iowa). Drop testing (Celestica; Toronto, Ontario, Canada) was run as an identical parallel test to minimize variation between the NASA-DoD and Crane test data. Celestica (Toronto, Ontario, Canada) also performed the vibration testing for the Crane test vehicles.

The goal of the Crane test vehicle effort is to generate initial data supporting the qualification of existing SnPb rework procedures for all military hardware built with lead-free processes through analysis of thermal cycling, vibration, and drop test data, with subsequent microsection analysis. Questions to be answered by the Crane testing effort include:

1. What effect does X1 and X2 rework have on assembly reliability as tested by thermal cycle, vibration, and drop testing?
2. Are lead-free assemblies reworked with SnPb as reliable as as-built lead-free hardware?
3. How do residual Pb-free solder contamination levels in SnPb joints after X1 and X2 rework correlate to reliability?
4. What effect does X1 and X2 SnPb rework have on surface mount land thickness (copper erosion) by cross section?
5. Observed visual evidence of X1 and X2 rework damage to 170Tg laminate?

All test results from the NASA-DoD Lead-Free Electronics Project and Crane Division, Naval Surface Warfare Center effort will be made publicly available on the NASA TEERM website [1].

Test Components

A variety of component types and component finishes were included on the test vehicle. The CLCC and TSOP component types were selected due to industry acknowledged solder joint integrity issues in Class III High Performance electronic products. The DIP components were selected to represent plated through-hole technology. The PLCC, TQFPs BGAs, CSPs and QFNs (MLF) were selected to represent surface mount technology. Table 1 lists the various component types with their associated surface finishes.

20LCC-1.27mm-8.90mm-DC-L-Au = **Tinning-SAC305**
20LCC-1.27mm-8.90mm-DC-L-Au = **Tinning-SnPb**
A-MLF20-5mm-.65mm-DC(30467)
A-MLF20-5mm-.65mm-DC-Sn(30801)
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643)
A-TQFP144-20mm-.5mm-2.0-DC-NiPdAu
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643) = **Tinning-SAC305**
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643) = **Tinning-SnPb**
PBGA225-1.5mm-27mm-DC(10565)
PBGA225-1.5mm-27mm-DC-LF(16074)
A-PDIP20T-7.6mm-DC-Sn (30737)
PDIP20T-DC (12006)
PDIP-20 - NiPdAu
A-CABGA100-.8mm-10mm-DC(30102)
A-CABGA100-.8mm-10mm-DC-LF(30695)
A-CABGA100-.8mm-10mm-DC-105
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-TR
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-SnBi-TR
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-Sn-TR

Table 1 Component Types and Finishes

Destructive Physical Analysis (DPA) is being performed on samples from each of the component types being placed onto the test vehicles. The DPA process is being used to ensure that the components being used for testing meet the consortia required standards and to evaluate the quality of construction.

Test Vehicle Assembly

The test vehicles (193 in total) were assembled at the BAE Systems Irving, Texas facility. A detailed description of the specific tin/lead and lead-free soldering processes was detailed in the NASA-DoD Lead-Free Electronics Project Plan [2].

The lead-free solder alloys selected for this project were:

1. SAC305 – Sn3.0Ag0.5Cu – reflow soldering {Tin (Sn); Silver (Ag); Copper (Cu)}
2. SN100C – Sn-0.7Cu-0.05Ni + Ge – reflow and wave soldering {Tin (Sn); Copper (Cu); Nickel (Ni); Germanium (Ge)}

Sn37Pb was used as the baseline for reflow and wave soldering.

Table 2 lists the solder alloys used for each type of solder process during the assembly of the NASA-DoD Lead-Free Electronics Project test vehicles.

Selection criteria of prime importance included commercial availability, industry trends, and past reliability testing performance.

Solder Alloy	Solder Process		
	Reflow	Wave	Manual
SAC305	X	N/A	X
SN100C	X	X	X
SnPb baseline	X	X	X

Table 2 Solder Alloys and Processes

{N/A = Due to limitations on board numbers and components, these solder alloys were not used during the noted assembly processes}

Test vehicles were assembled using these solders and a variety of component types. The following harsh environment testing was then conducted:

1. Vibration (Boeing; Seattle, Washington and Celestica; Toronto, Ontario, Canada)
2. Thermal Cycle -20 to +80°C (Boeing; Seattle, Washington) and -55 to +125°C (Rockwell Collins; Cedar Rapids, Iowa)
3. Combined Environments Testing (Raytheon; McKinney, Texas)
4. Mechanical Shock (Boeing; Seattle, Washington)
5. Drop (Celestica; Toronto, Ontario, Canada)
6. Interconnect Stress Test (PWB Interconnect Solutions Inc.; Nepean, Ontario, Canada)
7. Copper Dissolution (Celestica; Toronto, Ontario, Canada and Rockwell Collins; Cedar Rapids, Iowa)

Table 3 lists the various categories of test vehicles that were assembled for this effort.

Test Vehicle Type	Reflow Solder	Wave Solder	Number of Boards
Lead-Free Rework All Test Vehicles	SAC305	SN100C	33
SnPb Rework* All Test Vehicles	SnPb*	SnPb*	40
SnPb Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SnPb	SnPb	17
SnPb Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SnPb	SnPb	17
Lead-Free Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SAC305	SN100C	20
Lead-Free Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SAC305	SN100C	43
Lead-Free Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SN100C	SN100C	11
Lead-Free Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SN100C	SN100C	6
Lead-Free Manufactured Test Vehicles Crane Rework Effort	SN100C	SN100C	6

Table 3 Test Vehicle Assembly Details

{* NOTE: Lead-Free profiles will be used for reflow and wave soldering}

The solder joint quality and placement accuracy of all test vehicles were x-ray and visually inspected in accordance with the IPC-JSTD-001 and IPC-A-610 specifications.

Test Vehicle Rework

There was a large volume of rework for this project. In order to get the rework procedures completed in a timely manner, multiple facilities performed the rework activities (BAE Systems; Irving, Texas, Lockheed Martin; Ocala, Florida, and Rockwell Collins; Cedar Rapids, Iowa).

Components reworked were grouped by rework solder alloy / material (SnPb, Flux only, SAC305 and SN100C). The location performing the rework chose what order to rework the solder alloy / material groups, but had to use the numbered order below for specific component locations within the solder alloy / material group. When reworking a component, the component was to be removed and replaced before moving to the next component. All details regarding the rework procedure, including temperature profiles, are contained in the NASA-DoD Lead-Free Electronics Project Plan.

Thermal Aging

The project consortia members desired to have the test vehicles begin the various testing procedures with a common starting state point in an effort to eliminate potential assembly differences which could possibly inadvertently/unintentionally influence the testing results. The project consortia members reviewed intermetallic calculations generated by Rockwell Collins and compared the calculations to data sets from the Center for Advanced Vehicle Electronics (CAVE) at Auburn University, the National Physics Laboratory (NPL), the National Institute of Standards and Technology (NIST), and the Center for

Advanced Life Cycle Engineering (CALCE) at University of Maryland.

The thermal aging procedure was selected to establish a common, standard starting point such that all test vehicles were relatively equal in terms of solder joint microstructure, printed wiring board stress state, surface finish oxidation condition, and intermetallic phase formation/thickness. The thermal aging procedure is not necessarily, nor intended to be, representative of the various burn-in, bake-out, or other environmental stress screening (ESS) procedures that are used to evaluate electronics hardware quality/functionality. Additionally, it should be noted that the thermal aging procedure being used by the NASA-DoD LFE Project consortia is not meant to be representative of operational field life.

Assembly Irregularities

With all of the complexities built into the NASA-DoD Lead-Free Electronics Project design of experiment, test vehicle irregularities were bound to occur.

When reviewing the CSP data, please note that the CSP components on all test vehicles only have continuity in the outside solder balls. The wrong component configuration was used during test vehicle drafting. Traces interconnecting internal rows of balls to the outside row of balls do not exist on the test vehicles, Figure 2

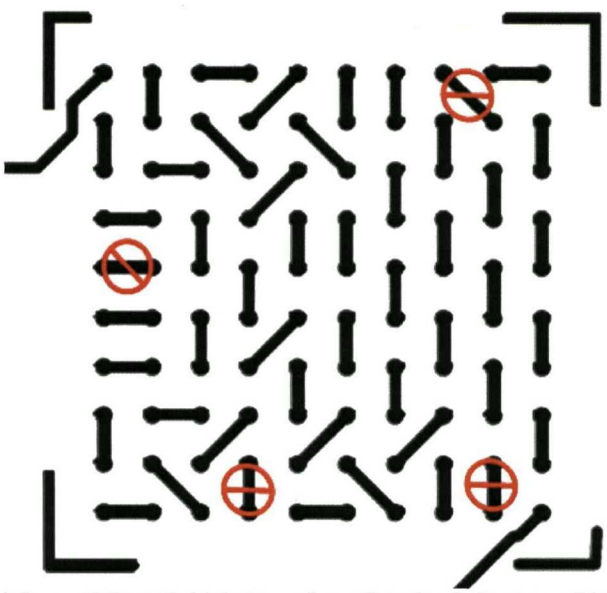


Figure 2 Test Vehicle Drawing, Chip Scale Package (CSP)

In order for a CSP component failure to be recorded, breaks in both sides of the continuity box must occur, Figure 3.

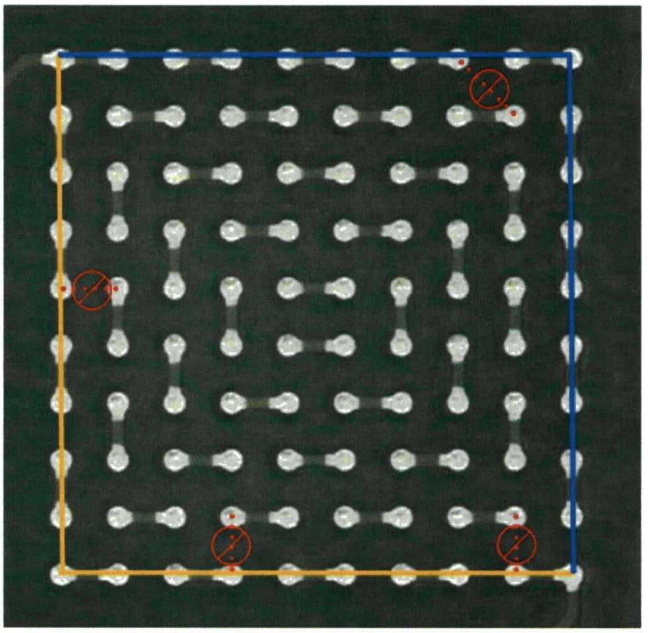


Figure 3 Chip Scale Package (CSP) Continuity Loop

The assembled boards were then subjected to harsh environments testing (e.g., thermal cycle, vibration, drop, mechanical shock) to better define solder joint reliability. Results from the project have been made available during the duration of the project allowing advanced information to assist organizations in their implementation or mitigation strategies.

TESTING PARAMETERS AND METHODOLOGY

In developing the test plan, there was a review of the performance requirements called out in applicable military and industry standards. The next step was to select test methods recognized and agreed upon by the technical team members. A key factor was selecting test parameters that would subject enough environmental stress to cause solder joints to fail, thus permitting differentiation between lead vs. lead-free performance. Military document MIL-STD-810F [3] and industry documents IPC-SM-785 [4] and IPC-TM-650 [5] were primary references used for writing the test plan. One test—the Combined Environments test—followed a procedure developed and used by Raytheon.

Vibration (Boeing; Seattle, Washington and Celestica; Toronto, Ontario, Canada)

The vibration test was conducted at two separate locations. The NASA-DoD Lead-Free Electronics Project test vehicles were tested at Boeing while the Crane Division test vehicles were tested at Celestica.

The vibration test determines solder joint failures during exposure to vibration conditions. The stakeholders agreed that MIL-STD-810F, Method 514.5 (Vibration), would be the starting point for developing a vibration test that would determine the reliability of the various solder alloys under severe vibration. Specific details on the vibration test can be found in the Joint Test Protocol [6].

The stakeholders agreed that a stress step test representing increasingly severe vibration environments was appropriate for this test, see Figure 4. A step stress test is required since a test conducted at a constant 8.0 g_{rms} level (Step 1) would take thousands of hours to fail the same number of components as a step stress test. This is because some locations on a circuit assembly experience very low stresses and severe vibration is required in order to fail components at these locations. The shape of the PSD (Power Spectral Density) curve for each step stress level was designed so that all of the major resonances of the test vehicles would be excited by the random vibration input. The PSD curves presented in MIL-STD-810F were used as guides for the creation of this step stress test but were not directly duplicated.

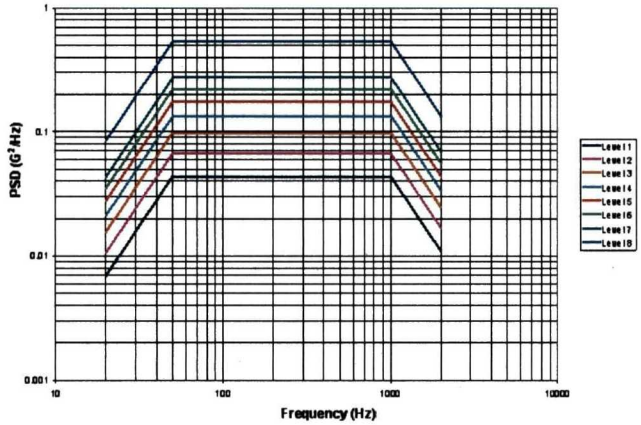


Figure 4 Vibration Spectrum

Thermal Cycle -20 to +80°C (Boeing; Seattle, Washington) and -55 to +125°C (Rockwell Collins; Cedar Rapids, Iowa)

The thermal cycle testing determines the capability of a solder to withstand extreme thermal cycling. This test will be performed in accordance with IPC-SM-785. Figure 5 illustrates the test vehicles loaded into the -55 to +125°C test chamber.

Thermal cycling will be conducted at two different conditions, -20 to +80°C and -55 to +125°C, technical representatives from the U.S. Army Aviation and Missile Command (AMCOM) suggested two temperature ranges to allow for acceleration factors to be determined, which will permit extrapolation of the data to actual use conditions of their systems. The thermal cycle tests were run until a significant number (greater than 63 percent) of component failures were achieved in order to provide statistically meaningful data. Specific details on the thermal cycle test can be found in the Joint Test Protocol.

After examining the available data on dwell time effect, the lead-free solder project participants agreed that the high-temperature dwell time would be 30 minutes. Solder alloy creep during the high temperature dwell of the thermal cycle is largely responsible for damage within the solder joints. In order to maximize the effects of solder alloy creep, a 30-minute high temperature dwell will be used for this project.

Figure 5 Test Vehicles in the Thermal Cycle Chamber

Combined Environments Testing (Raytheon; McKinney, Texas)

The Combined Environments Test (CET) determines the reliability of solders under combined thermal cycle and vibration. The CET for the NASA-DoD Lead-Free Electronics Project is based on a modified Highly Accelerated Life Test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process. The project stakeholders felt that the CET would provide a quick method to identify comparative potential reliability differences in the test alloys vs. the SnPb baseline. The primary accelerated environments are temperature extremes (both limits and rate of change) and vibration (pseudo-random six degrees of freedom used in combination). Specific details on the combined environments test can be found in the Joint Test Protocol.

This test utilized a temperature range of –55 to 125°C with 20°C/minute ramps. The dwell times at each temperature extreme are the times required to stabilize the test sample plus a 15-minute soak. 10 g_{rms} pseudo-random vibration was applied for the duration of the thermal cycle. Testing continued until sufficient data was generated to obtain statistically significant Weibull plots indicating relative solder joint endurance (cycles to failure) rates. If significant failure rates were not evidenced after 50 cycles, the vibration levels were increased in increments of 5 g_{rms} and cycling continued for an additional 50 cycles. This process was repeated until all parts failed or 55 g_{rms} was reached. Figure 6 illustrates the test vehicles loaded into the HALT/HASS Chamber.

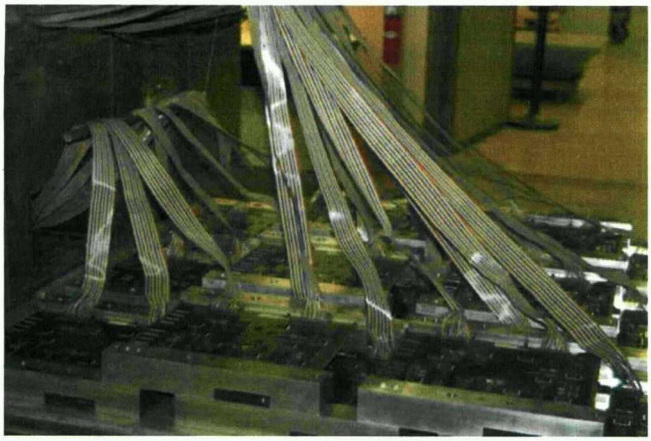


Figure 6 Test Vehicles in the HALT/HASS Chamber

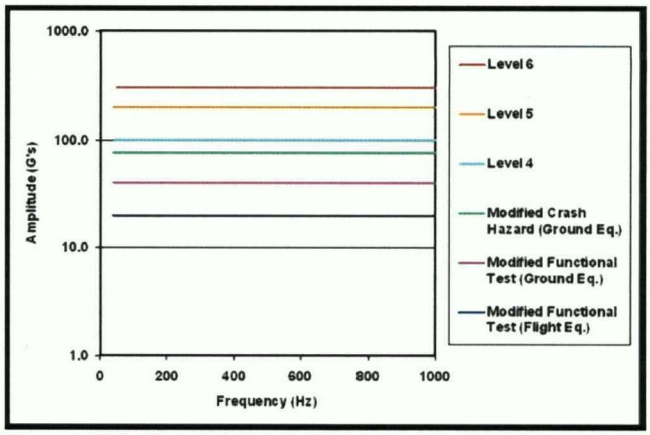


Figure 7 Mechanical Shock SRS Test Levels

Mechanical Shock (Boeing; Seattle, Washington)
The purpose of the mechanical shock test is to determine the resistance of the solder to the stresses associated with high-intensity shocks induced by rough handling, transportation, or field operation. The mechanical shock test procedure was changed from the procedure used for the JCAA/JGPP Lead-Free Solder Project. The consortia members felt that the procedure change was necessary since it is very difficult to meet both the SRS shape and the pulse duration for this test as outlined in MIL-STD-810F. Pulse duration is approximately equal to the inverse of lowest SRS frequency, 10 Hz. SRS requirement means pulse duration >100 msec while MIL-STD-810F outlines pulse durations $\leq$ 23 msec. Specific details on the mechanical shock test can be found in the Joint Test Protocol.

Testing followed MIL-STD-810F, Method 516.5 with the following modifications: (1)100 shocks were applied per test level (rather than 3) and all of the shocks were applied in the Z-axis, and (2) the shock transients applied at the levels specified in MIL-STD-810F, Method 516.5 for the Functional Test for Flight Equipment, the Functional Test for Ground Equipment, and the Crash Hazard Test for Ground Equipment followed modified parameters detailed in the Joint Test Protocol. An additional step stress test will then be conducted (see Figure 7) with the shocks being applied in the Z-axis only. For Level 6 (300 G's), 400 shocks will be applied instead of 100. Testing continued until a majority (approximately 63 percent) of components was failed.

Drop (Celestica; Toronto, Ontario, Canada)
This test determines the resistance of board level interconnects to board strain induced by dynamic bending as a result of drop testing. Boards tested using this method typically fail either as interfacial fractures in the solder joint (most common with ENIG) or as pad cratering in the component substrate and/or board laminate. These failure modes commonly occur during manufacturing, electrical testing (especially in-circuit test), card handling and field installation. The root cause of these types of failures is typically a combination of excessive applied strain due to process issues and/or weak interconnects due to process issues and/or the quality of incoming components and/or boards. Specific details on the drop test can be found in the Joint Test Protocol. Figure 8 illustrates the test vehicles loaded onto the drop test fixture.

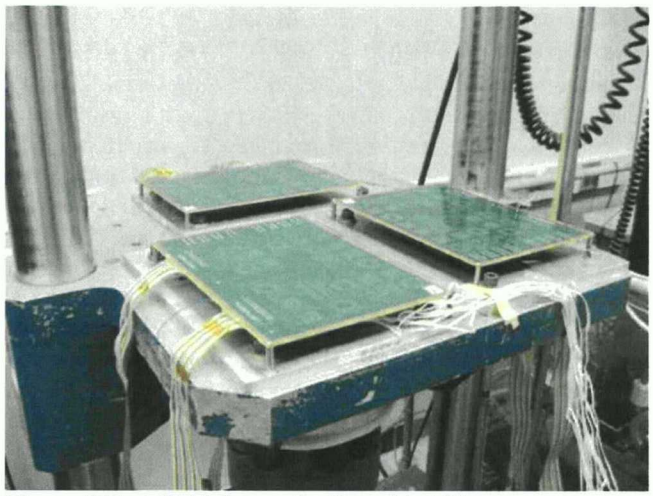


Figure 8 Test Vehicles on the Drop Test Fixture

Interconnect Stress Test (PWB Interconnect Solutions Inc.; Nepean, Ontario, Canada)
Interconnect Stress Test (IST) is an industry recognized test method (IPC) that accelerates thermal cycling testing by heating a specifically designed test coupon to 150°C in exactly 3 minutes followed by cooling to ambient in approximately two minutes. IST test coupons have two circuits, a sense circuit and a power circuit, to monitor

material delamination and crazing. The power circuit heats the coupon. The sense circuit is a passive circuit that monitors temperature and measures damage accumulation of the interconnect structure, typically a plated through-hole (PTH). There are usually 400 to 800 structures per circuit to achieve a higher, statistically relevant, sample size. Both the power and sense circuits change in resistance (milliohms) and temperature (°C) throughout the coupons during the thermal cycle. Thermal cycling continues until end of test or a 10% increase in resistance on either circuit. Each coupon is heated, monitored, and tested individually. This gives a number of advantages that include no hold time at temperature, tight test control in the ability to achieve any test temperature in three minutes +/- 5 seconds, the ability to stop testing within seconds of the circuit achieving a 10% increase in resistance allowing analysis of a developing failure rather than a catastrophic failure. Testing stops immediately when the circuit achieves 10% increase in resistance, allowing a failed circuit to have a low amount of power applied that creates a hot spot at the failure site visible by a thermal imaging camera. Specific details on IST can be found in the Joint Test Protocol.

Copper Dissolution (Celestica; Toronto, Ontario, Canada and Rockwell Collins; Cedar Rapids, Iowa)
The purpose of the copper dissolution testing is to characterize, document, and compare the impact of soldering process on the copper plated through-hole and surface pad structures for the NASA-DoD test vehicles with the SAC305 and SN100C solder alloy systems. The copper dissolution test results will provide a data set which can be used as a first order approximation of the copper plating thickness loss due to lead-free solder processing. Additionally, the copper dissolution test results can be compared to other published industry results for alternative solder alloy systems and different soldering processes.

Printed Circuit Board (PCB) and plated through-holes can be eroded or dissolved away in the presence of molten solder rendering the PCB non-functional. Significant dissolution can occur with the use of certain new Sn-rich alloys and is further exacerbated by higher process temperatures. Clearly this phenomenon represents a serious risk to circuit reliability. There is a clear need to determine the dissolution rate of copper pads with lead-free solders under various conditions. Specific details on copper dissolution can be found in the Joint Test Protocol.

TEST RESULTS

At the time this document was drafted, only a portion of the testing activities had been completed. For the testing activities that were complete, failure analysis activities were ongoing or in the planning stages. All test reports will be made available on the NASA TEERM website.

DISCUSSION

Based on the work that has been completed to date, assembly of high-performance electronics using lead-free solder alloys is possible without a total retrofit of the factory.

Some control of equipment is necessary to eliminate the cross contamination of lead-free and SnPb solder alloys to ensure optimal reliability for some component types. Significant resources will be required for component configuration management to assure that incompatible metallurgies are not mixed in the factory. The huge potential for mixed components from suppliers will drive validation and inspection costs throughout the factory.

FUTURE WORK

For the testing activities that have been completed, failure analysis activities are schedule to be conducted later this year.

The thermal cycle testing (-20 to +80°C and -55 to +125°C) was on going at the time this paper was drafted. -55 to +125°C testing is expected to be completed over the summer with data and failure analysis to be completed later in the year. It is unknown when the -20 to +80°C testing will be complete.

ACKNOWLEDGEMENTS

The author would like to thank Lety Campuzano-Contreras of BAE Systems; Dr. Tom Woodrow of Boeing; Dave Hillman of Rockwell Collins; Cynthia Garcia and Jeff Bradford of Raytheon; Dr. Polina Snugovsky, Jason Bragg, and Jeff Kennedy of Celestica; Linda Woody and Ed Morris of Lockheed Martin; Paul Reid and Bill Birch of PWB Interconnect Solutions Inc; Jim Blanche of Jacobs Engineering; Vance Anderson of Defense Microelectronics Activity; Andy Ganster and Gary Latta of Crane Division, Naval Surface Warfare Center and David Amidei and Chuck Griffin of NASA.

The author would also like to acknowledge the other members of the NASA-DoD Lead-Free Electronics Consortium not mentioned by name. This effort would not be possible without their contributions.

REFERENCES

[1] NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center website; http://teerm.nasa.gov
[2] NASA-DoD Lead-Free Electronics Project Consortium, "NASA-DoD Lead-Free Electronics Project Plan"; March 2010
[3] MIL-STD-810F: Environmental Engineering Considerations and Laboratory Tests January 2000
[4] IPC SM 785: Guidance for Accelerated Reliability Testing of Surface Mount Solder Attachments Nov. 1992
[5] IPC TM 650: Test Methods Manual January 2007
[6] NASA-DoD Lead-Free Electronics Project Consortium, "NASA-DoD Lead-Free Electronics Project, Joint Test Protocol"; September 2009

National Aeronautics and Space Administration

NASA-DoD Lead-Free Electronics Project

Pb-free Electronics Risk Management (PERM)

January 5, 2010

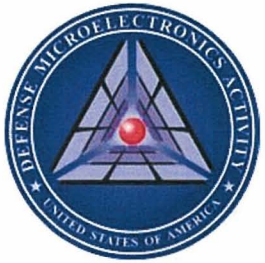
Resources

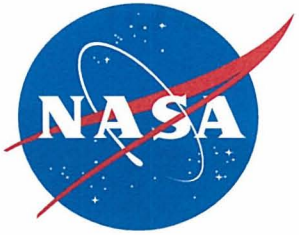
Project documents, test plans, test reports and other associated information will be available on the web:

- NASA-DoD Lead-Free Electronics Project: http://www.teerm.nasa.gov/projects/NASA_DODLeadFreeElectronics_Proj2.html
  - Joint Test Protocol
  - Project Plan

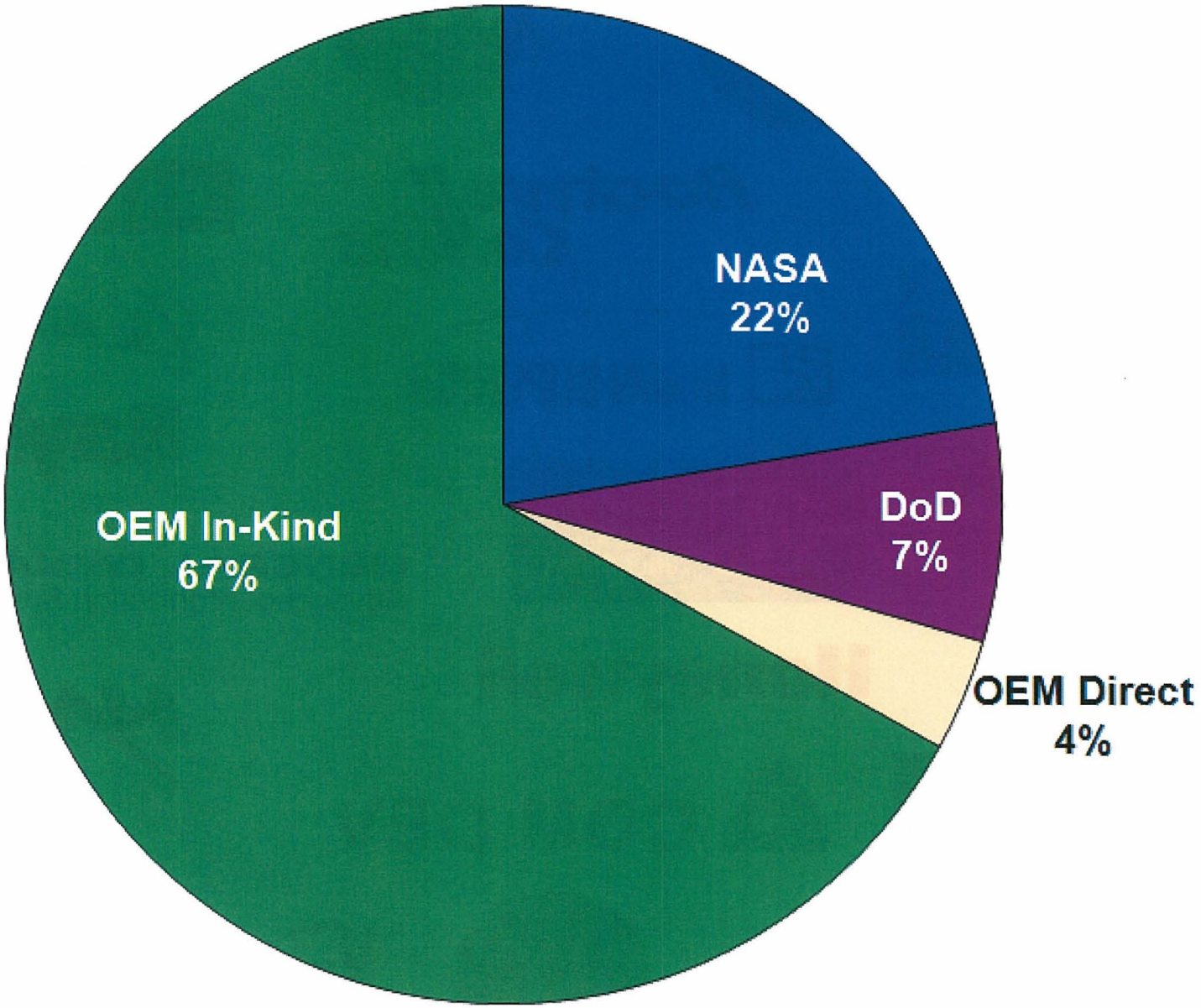
- JCAA/JGPP Lead-Free Solder Project http://www.teerm.nasa.gov/projects/LeadFreeSolderTestingForHighReliability_Proj1.html

Project Stakeholders



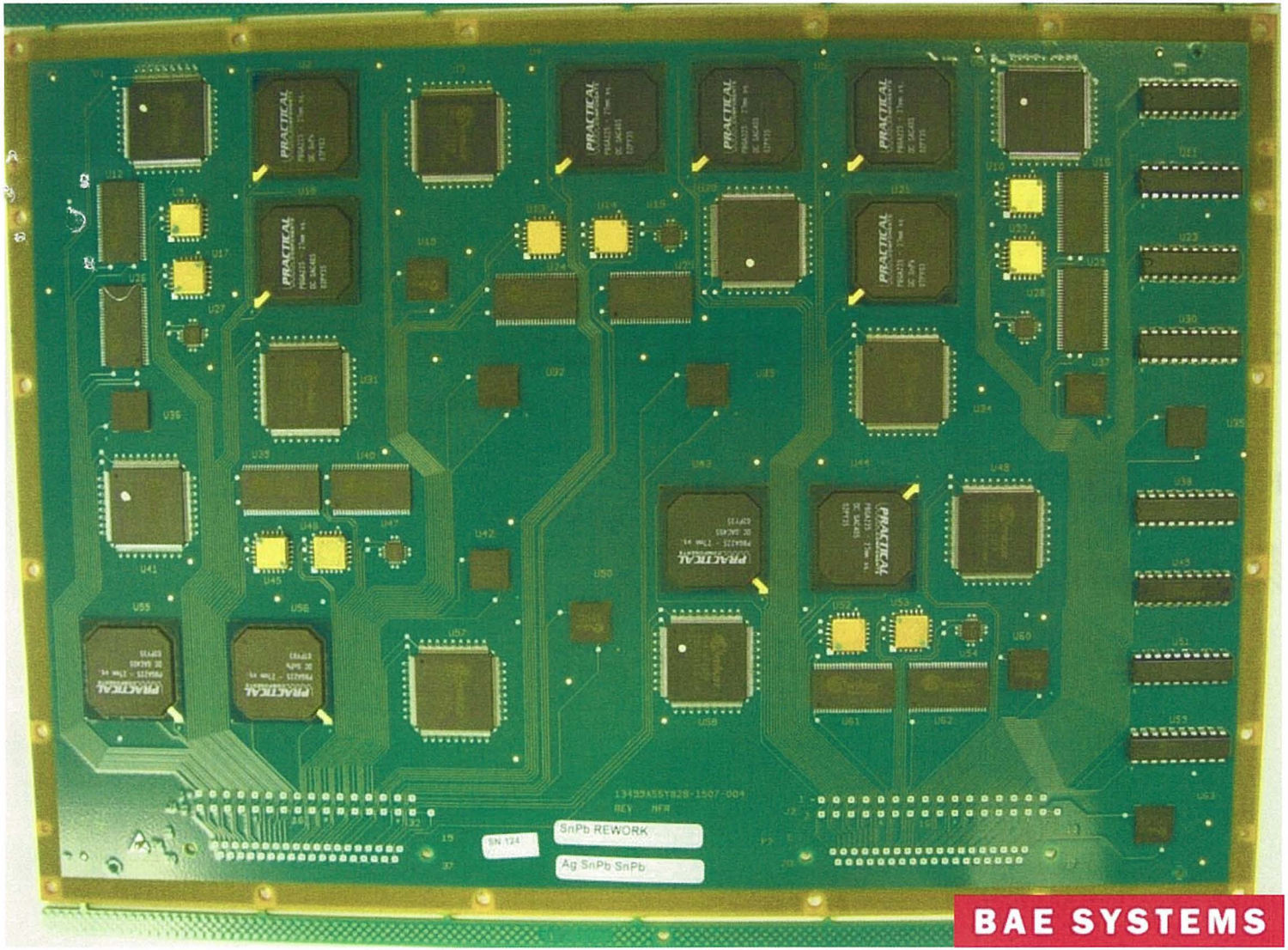


Contributions to the NASA-DoD Lead-Free Electronics Project ~$2.1 Million



Test Vehicles

- 193 Test Vehicles Assembled by BAE Systems (Irving, Texas)
  120 = “Manufactured”
  73 = “Rework”



Circuit Cards

- 14.5”X 9”X 0.09”
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170ºC (Isola 370HR)
- Pho-Tronics

NAVSEA Crane Rework Effort

Built 30 test vehicles (sub-set of the 193 assembled)

- Test vehicles were built with Lead-Free solder and Lead-Free component finishes only = similar to Manufactured test vehicles for Mechanical Shock, Vibration and Drop Testing
- Lead-Free alloys, SAC305 and SN100C
- Rework was done using only SnPb solder
- Performed multiple pass rework 1 to 2 times on random Pb-free DIP, TQFP-144, TSOP-50, LCC and QFN components
- Testing
  - Thermal Cycling -55°C to +125°C – *Testing In-Progress with NASA-DoD test vehicles*

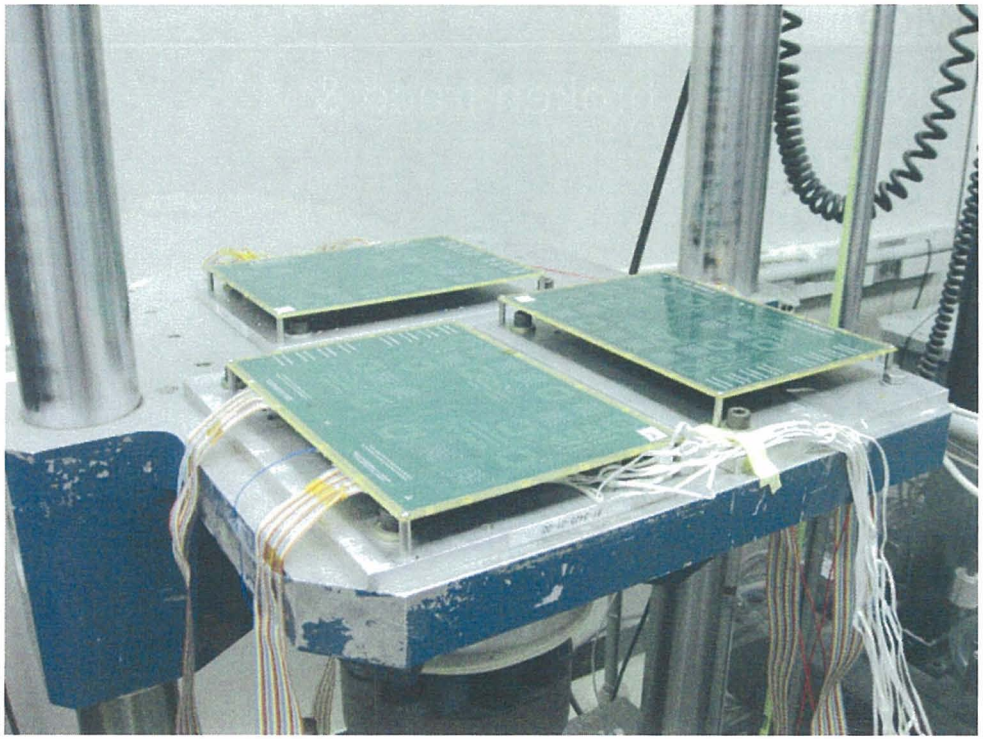
    Rockwell Collins
  - Vibration Testing CELESTICA. **COMPLETE**
  - Drop Testing CELESTICA. **COMPLETE**

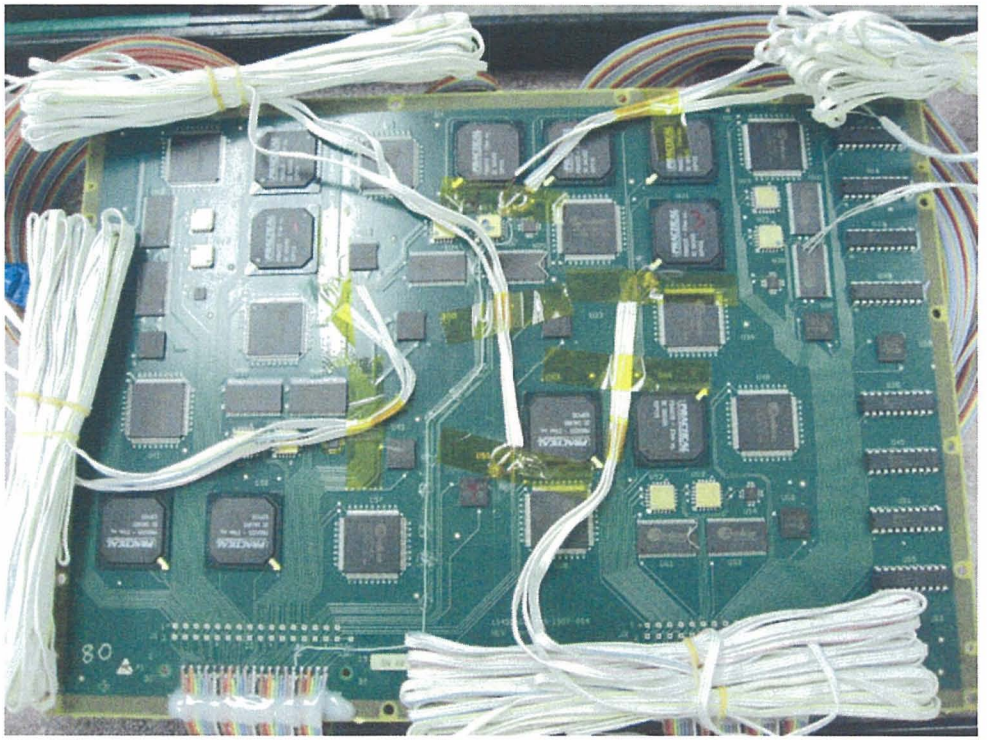
Drop Testing

CELESTICA

NSWC Crane Test Vehicles

- Shock parameters: 500 G, 2.0 ms duration (340 G for cards 80, 82, 87 for first
- 10 drops)
- Number of drops: 20
- 9 cards in total / 3 cards tested per drop
- Each card monitored for shock response
- Each card monitored for resistance
- Cards 80, 83, 86 monitored for strain



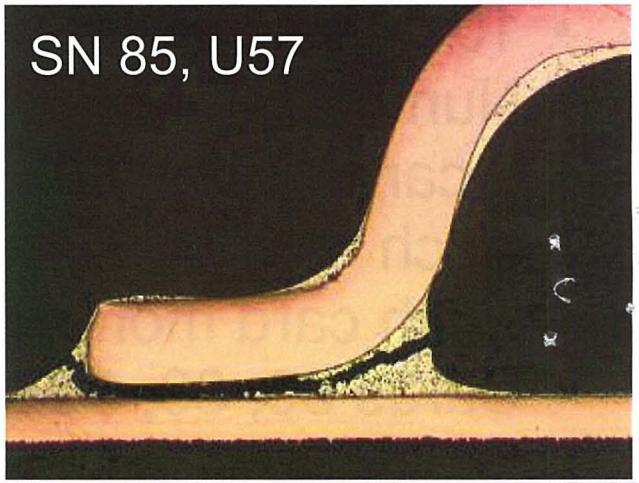


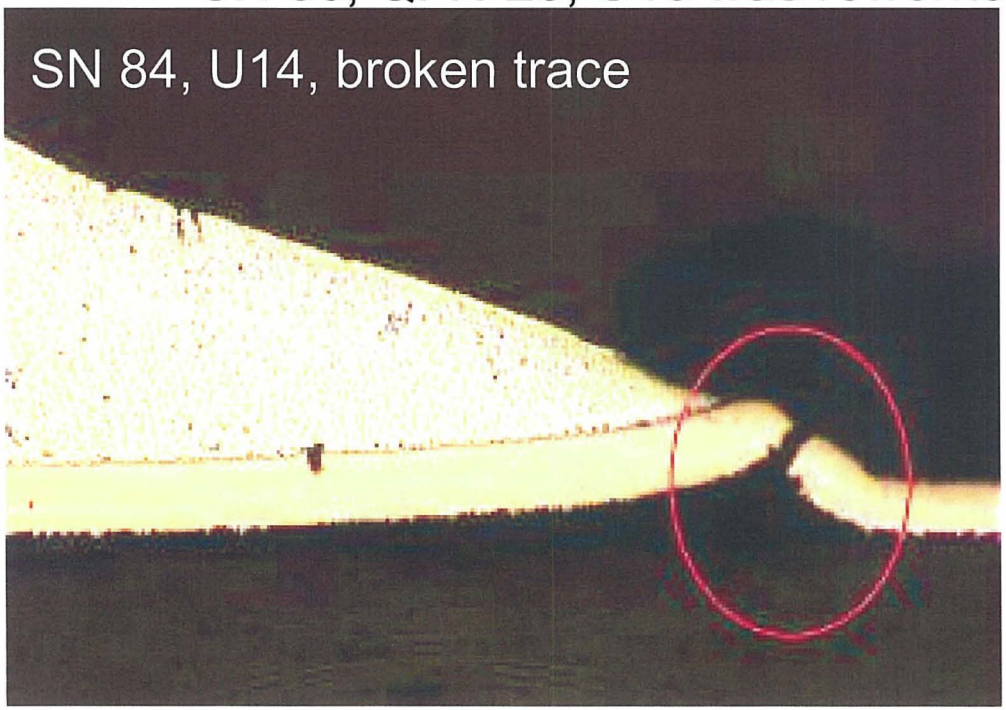
Drop Testing

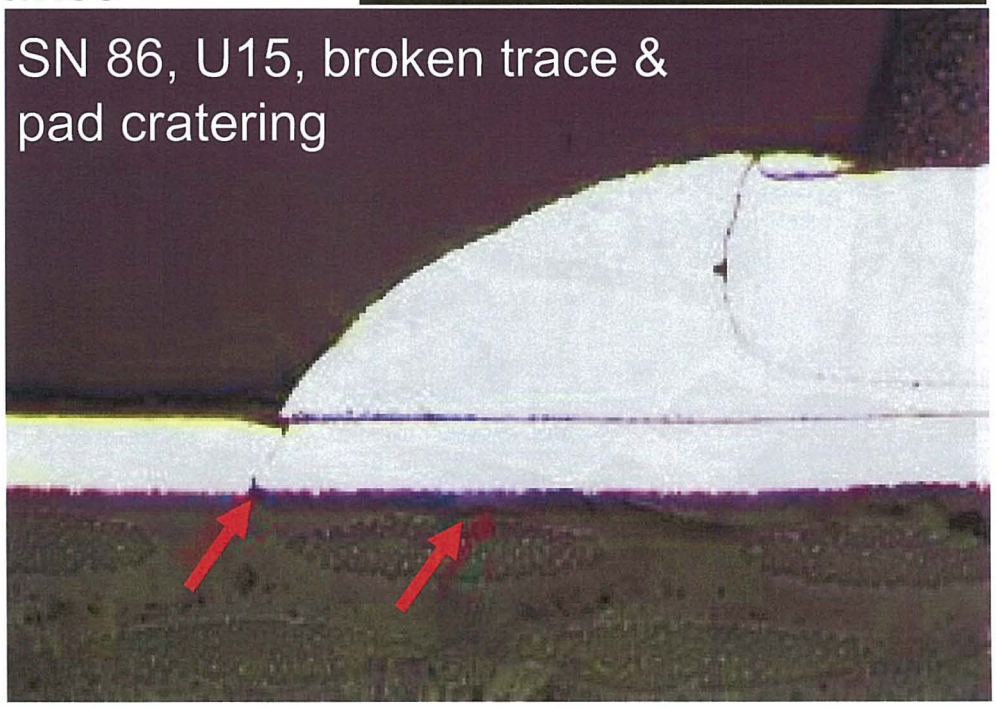
CELESTICA

NSWC Crane Test Vehicles

- Only component to have significant failures – BGA 225
- The 4 non-BGA samples that had an electrical failure had the following rework histories:
  - SN 85, TQFP 144, U57 was reworked once
  - SN 85, PDIP-20, U8 was reworked once
  - SN 84, CLCC-20, U14 was not reworked
  - SN 86, QFN-20, U15 was reworked twice







Testing Activities
NASA-DoD Test Vehicles

Specific testing details can be found in the Joint Test Protocol (JTP)
http://www.teerm.nasa.gov/projects/NASA_DODLeadFreeElectronics_Proj2.html

- Thermal Cycle Testing (-20/+80°C) BOEING
- Combine Environments Testing Raytheon COMPLETE
- Drop Testing CELESTICA. COMPLETE
- Thermal Cycle Testing (-55/+125°C) Rockwell Collins
- Vibration Testing BOEING COMPLETE
- Mechanical Shock Testing BOEING COMPLETE

<u>Not Covered in this Presentation</u>

- Interconnect Stress Test (IST) Interconnect PWB Solutions Inc COMPLETE
- Copper Dissolution CELESTICA. Rockwell Collins

Thermal Cycle Testing (-20/+80°C)

BOEING

Test Parameters

- 5 to 10°C/minute ramp
- 30 minute dwell at 80°C
- 10 minute dwell at -20°C

~ 3,000 Thermal Cycles Completed

National Aeronautics and Space Administration

NASA-DoD Lead-Free Electronics Project

DoD Soldering Technologies Working Group (STWG)

August 24 - 25, 2010

Resources

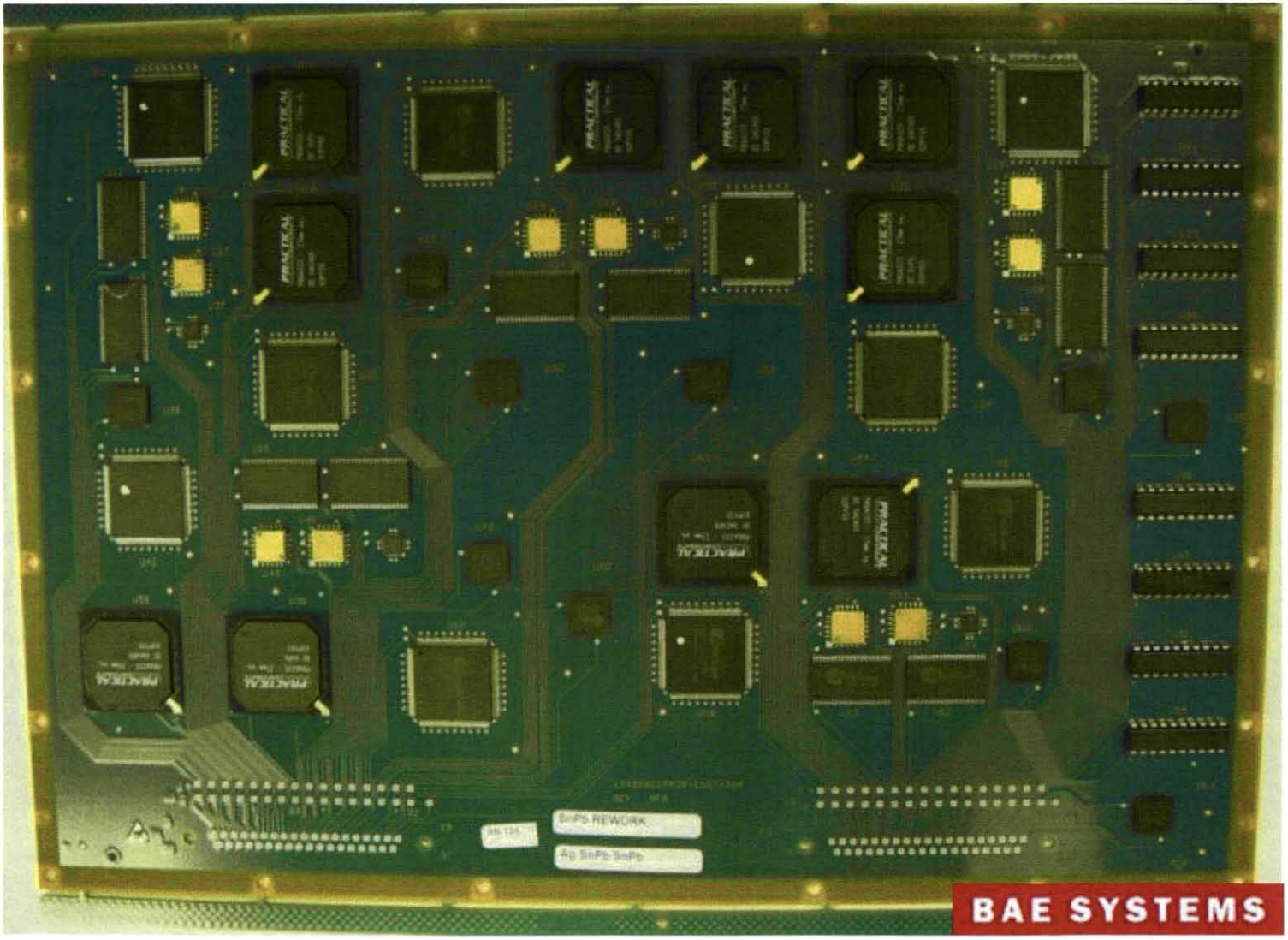
Project documents, test plans, test reports and other associated information will be available on the web:

- NASA-DoD Lead-Free Electronics Project: http://www.teerm.nasa.gov/projects/NASA_DODLeadFreeElectronics_Proj2.html
  - Joint Test Protocol
  - Project Plan
  - Test Reports

Project Stakeholders

Test Vehicles

- 193 Test Vehicles Assembled by BAE Systems (Irving, Texas)
  120 = "Manufactured"
  73 = "Rework"

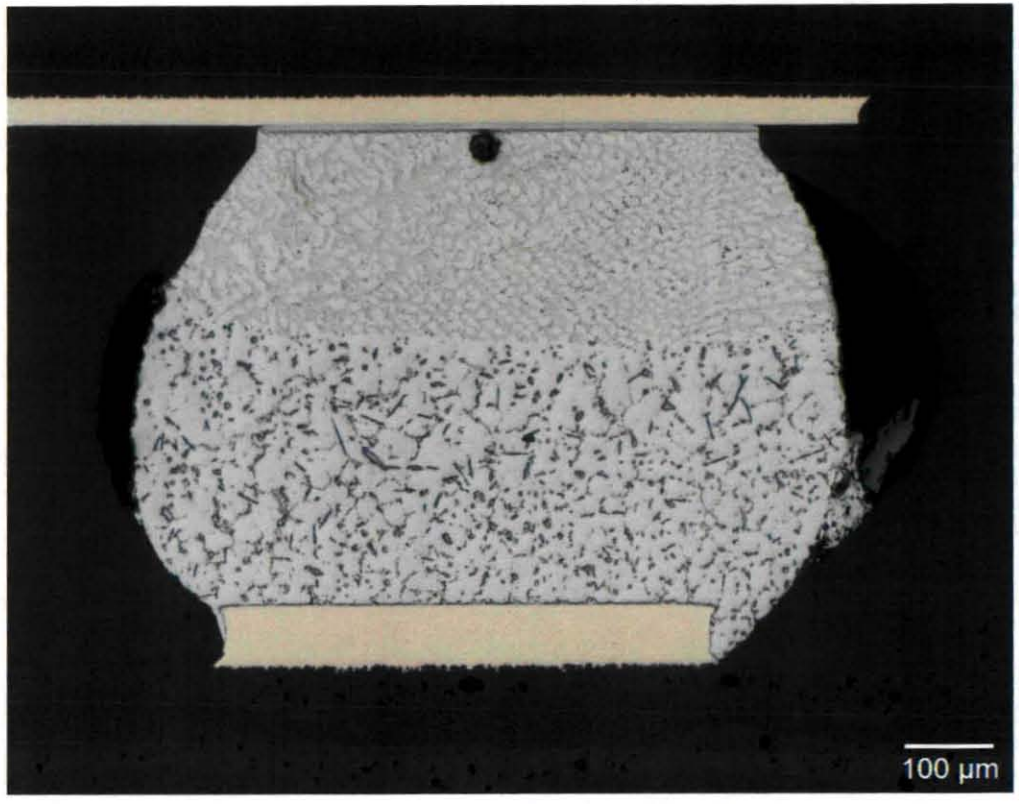


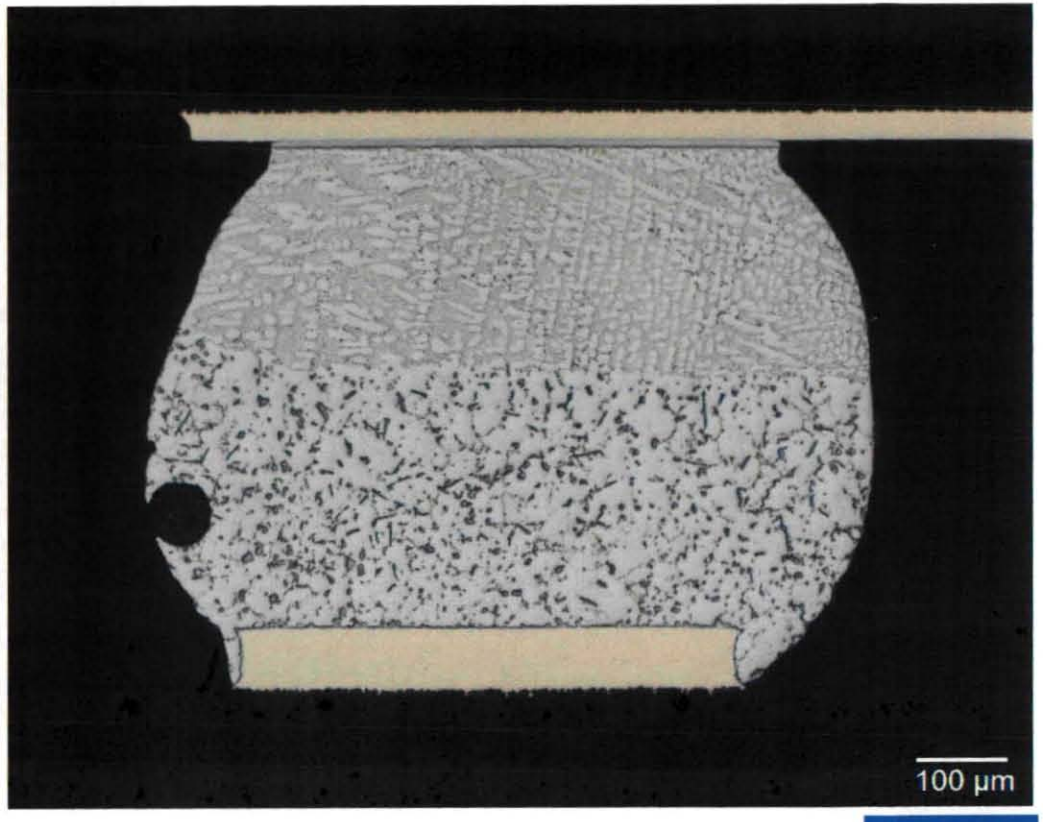
Circuit Cards

- 14.5"X 9"X 0.09"
- 6 layers of 0.5 ounce copper
- FR4 per IPC-4101/26 with a minimum Tg of 170°C (Isola 370HR)
- Pho-Tronics

Test Vehicle Characterization

Board # 3 SnPb As Fabricated
U18-BGA-225
Component Finish: SAC405, Reflow: SnPb



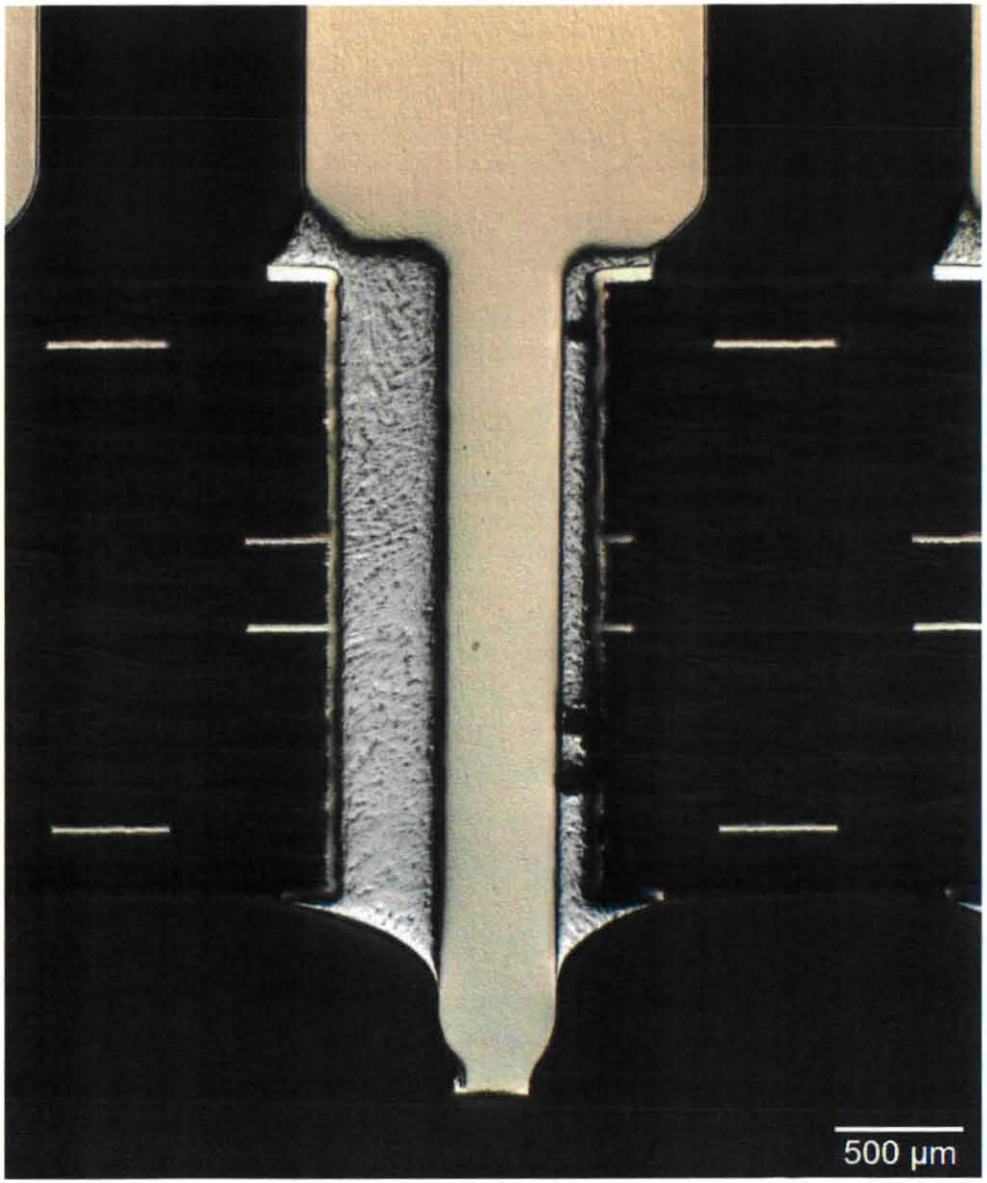


Reflow Soldering
Location – BAE Systems Irving, Texas
Reflow Profile = SnPb
- Preheat = ~ 120 seconds @140-183°C
- Solder joint peak temperature = 225°C
- Time above reflow = 60-90 sec
- Ramp Rate = 2-3 °C/sec

Sandia National Laboratories

Test Vehicle Characterization

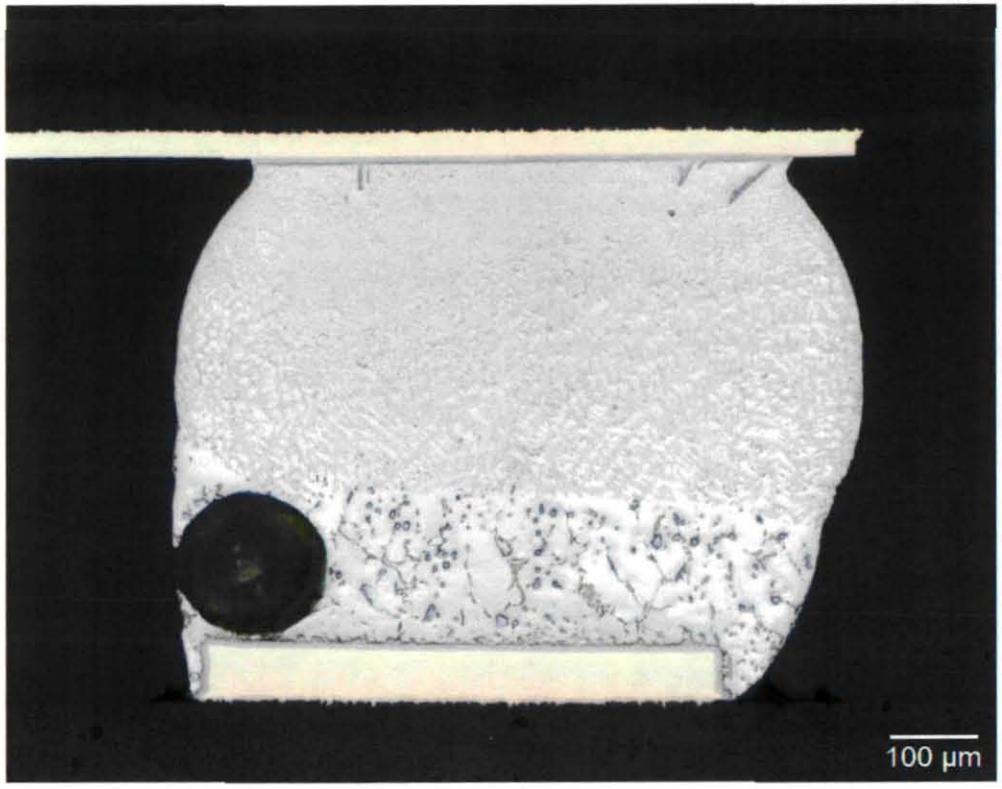
Board # 3 SnPb As Fabricated
U51-2 PDIP-20
Component Finish: Sn, Wave: SnPb

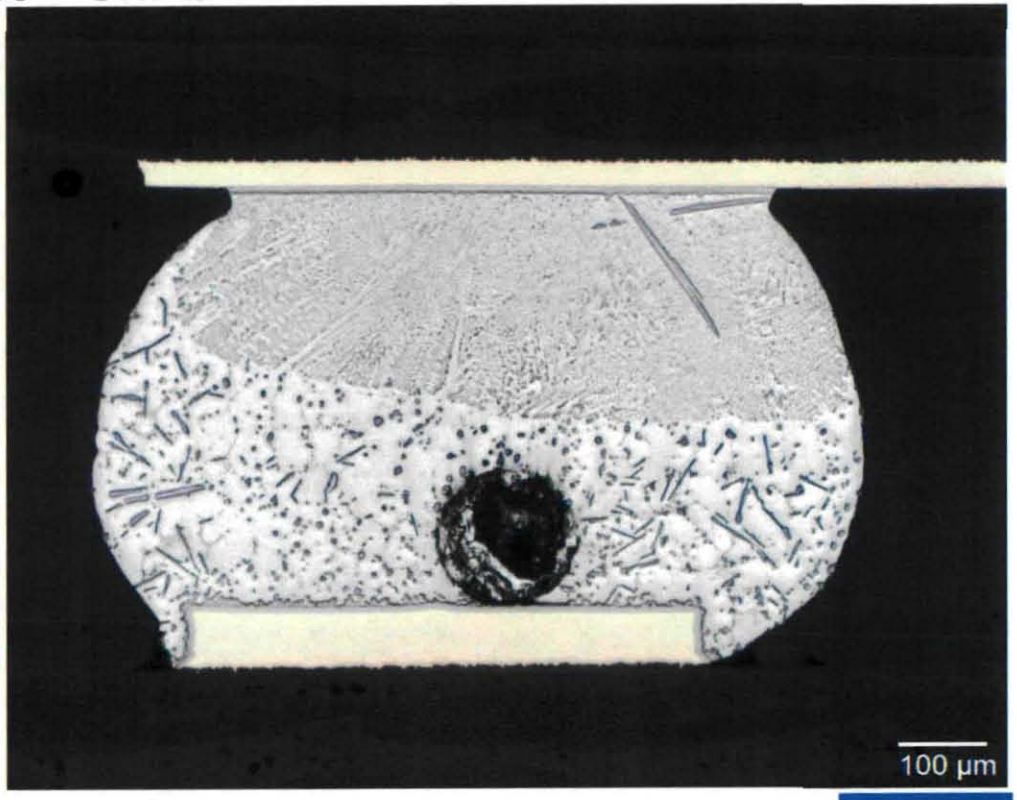


Sandia National Laboratories

Test Vehicle Characterization

Board # 154 SnPb Rework
U18 BGA-225
As assembled - Component Finish: SnPb, Reflow: SnPb
Reworked - Component Finish: SAC405, Rework Solder: SnPb
Rework Profile - SnPb

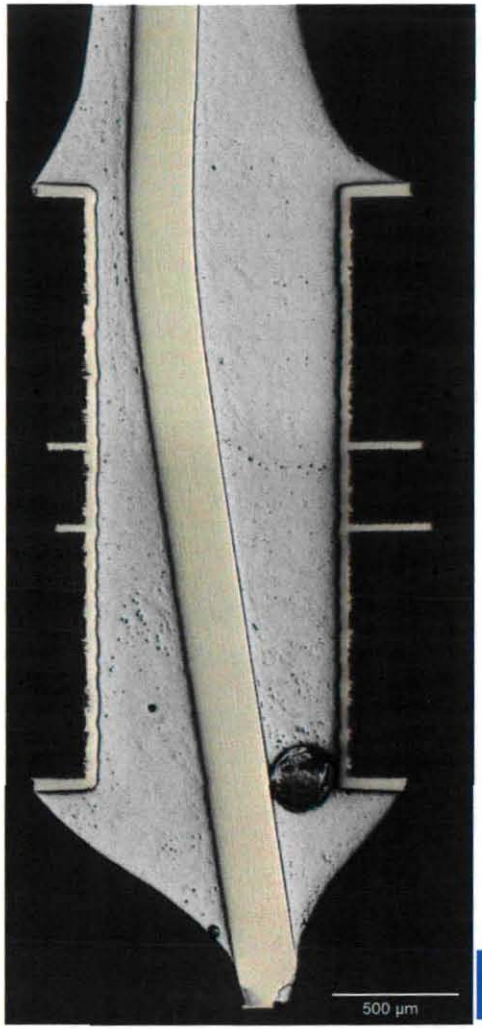




Sandia National Laboratories

Test Vehicle Characterization

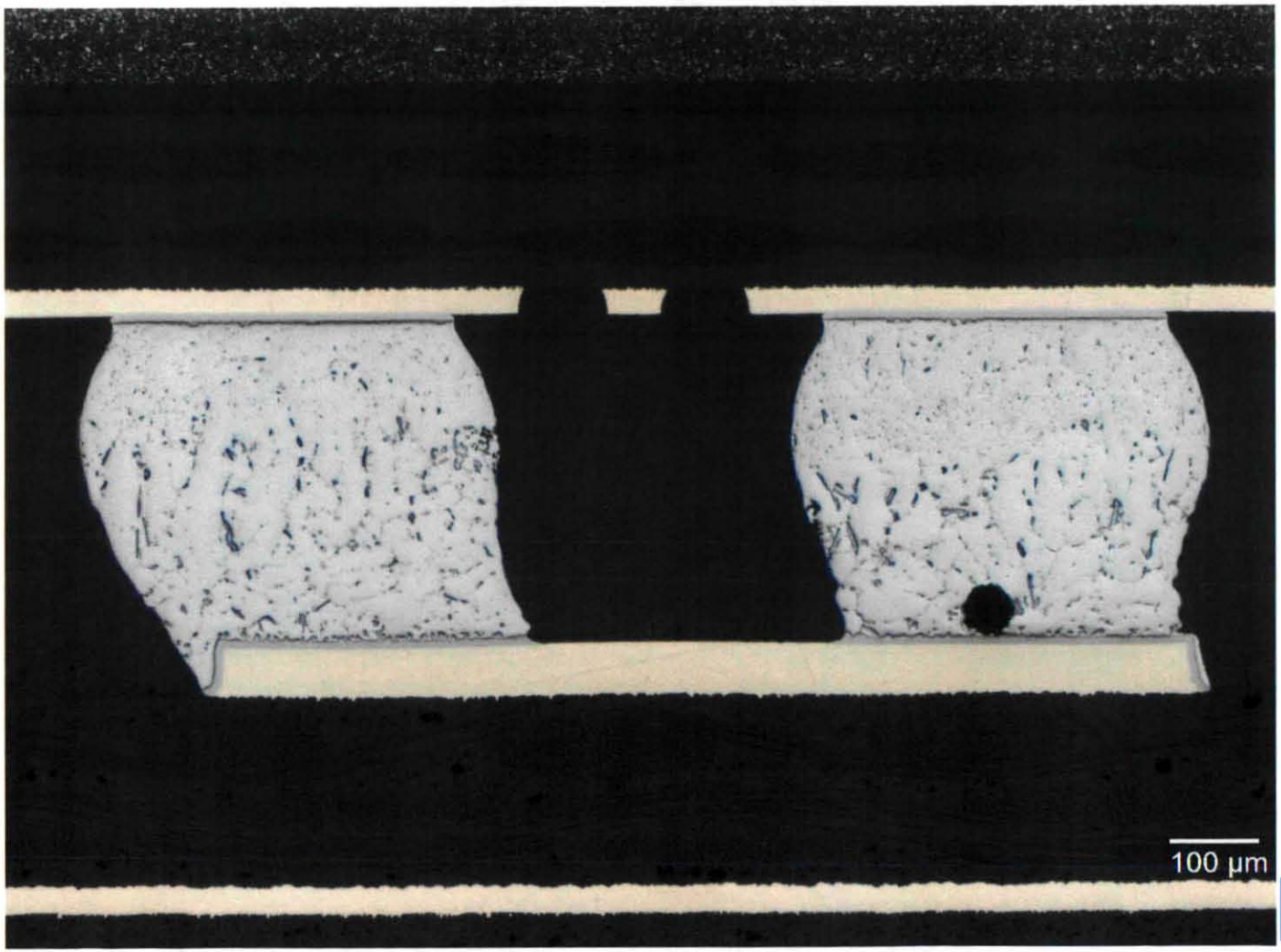
Board # 154 SnPb Rework
U51-1 PDIP-20
Component Finish: SnPb, Wave: SnPb
Reworked - Component Finish: Sn, Rework Solder: SnPb
Rework Profile - SnPb



Sandia National Laboratories

Test Vehicle Characterization

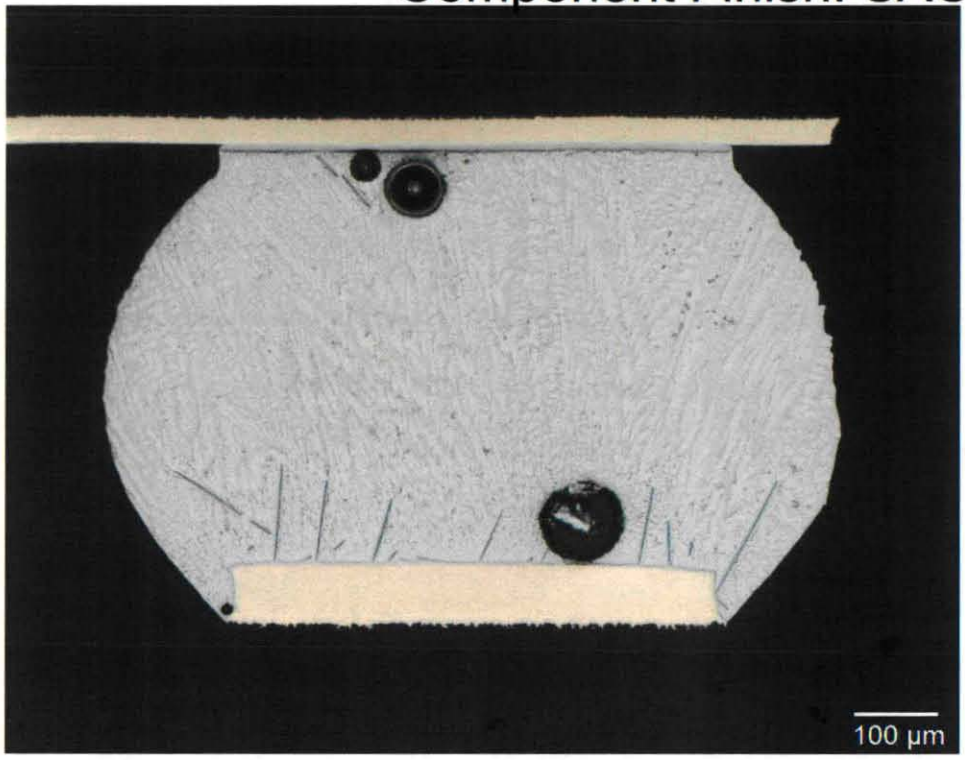
Board # 154 SnPb Rework
U60 CSP-100
Component Finish: SnPb , Reflow: SnPb
Reworked - Component Finish: SAC105, Rework Solder: SnPb
Rework Profile - SnPb

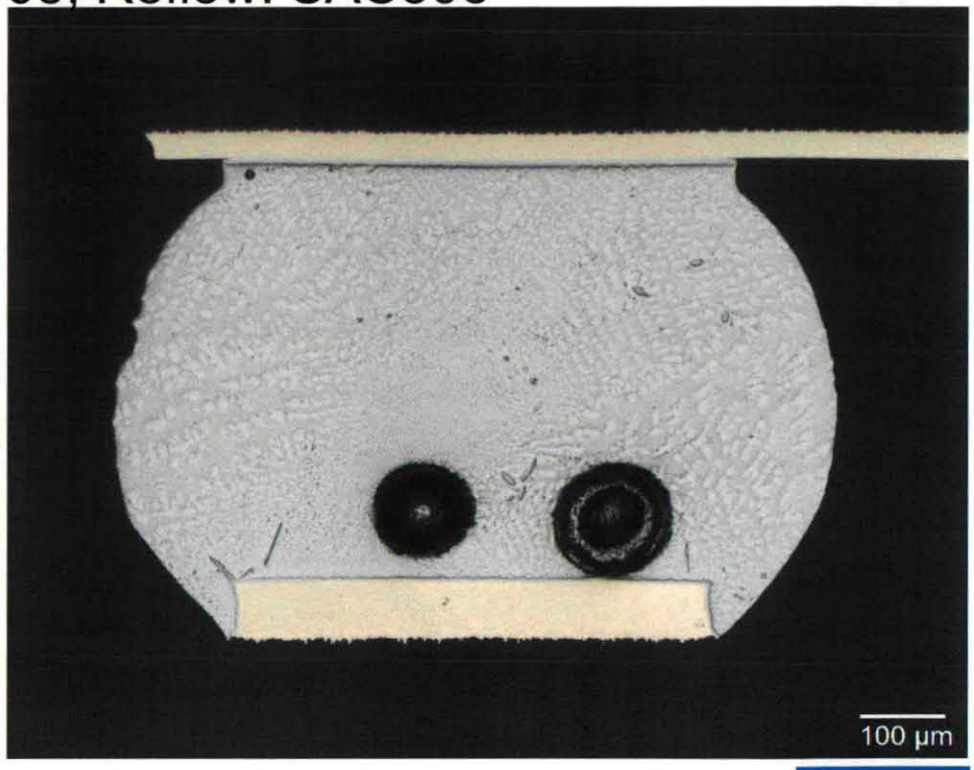


Sandia National Laboratories

Test Vehicle Characterization

Board # 39 Lead Free As Fabricated
U2 BGA-225
Component Finish: SAC405, Reflow: SAC305



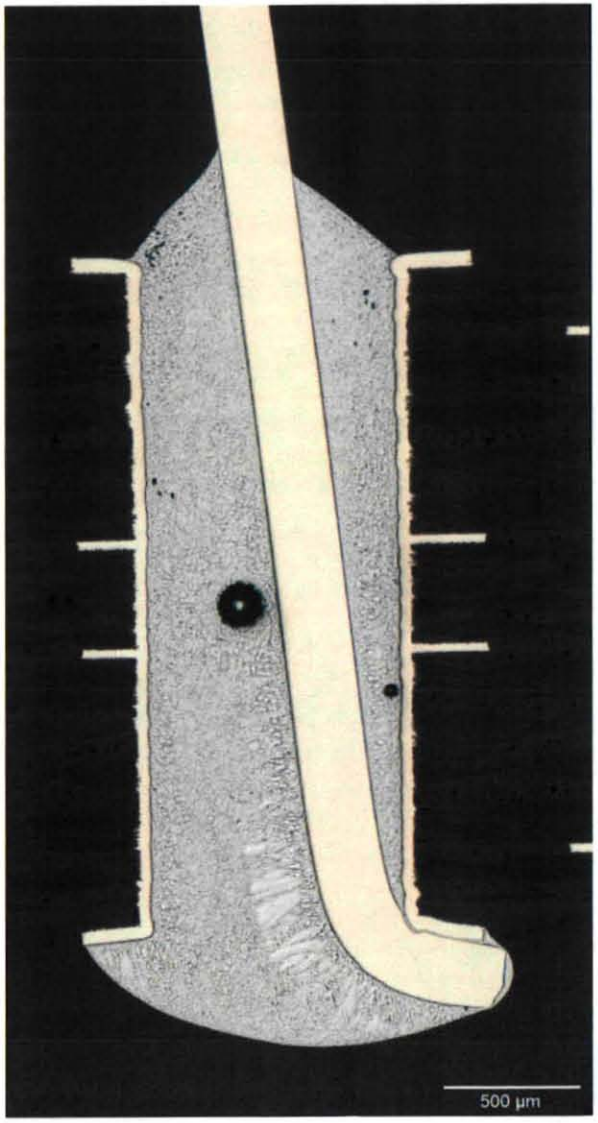


Sandia National Laboratories

Reflow Soldering
Location – BAE Systems Irving, Texas
Reflow Profile = SAC305
- Preheat = 60-120 seconds @150-190°C
- Peak temperature target = 243°C
- Reflow:~20 seconds above 230°C
- ~30-90 seconds above 220°C

Test Vehicle Characterization

Board # 39 Lead Free As Fabricated
U51-1 PDIP-20
Component Finish: NiPdAu, Wave: SN100C



Sandia National Laboratories

NAVSEA Crane Rework Effort

Built 30 test vehicles (sub-set of the 193 assembled)

- Test vehicles were built with Lead-Free solder and Lead-Free component finishes only = similar to Manufactured test vehicles for Mechanical Shock, Vibration and Drop Testing
- Lead-Free alloys, SAC305 and SN100C
- Rework was done using only SnPb solder
- Performed multiple pass rework 1 to 2 times on random Pb-free DIP, TQFP-144, TSOP-50, LCC and QFN components
- Testing
  - Thermal Cycling -55°C to +125°C Rockwell Collins **COMPLETE**
  - Vibration Testing CELESTICA **COMPLETE**
  - Drop Testing CELESTICA **COMPLETE**

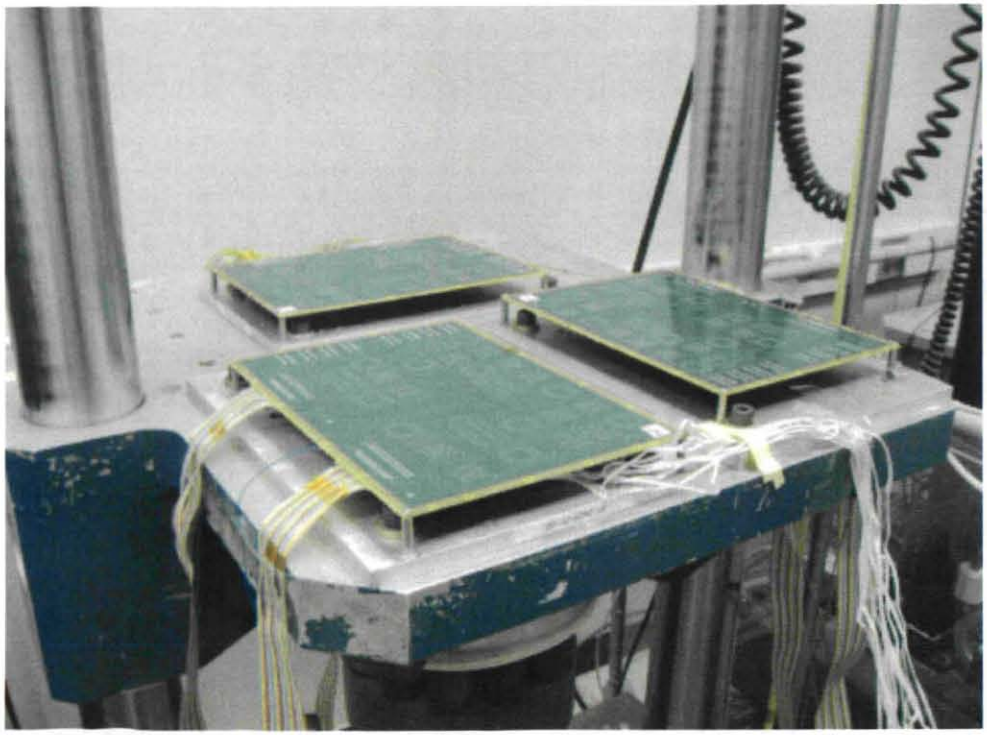
http://teerm.nasa.gov/NASA_DODLeadFreeElectronics_Proj2.html

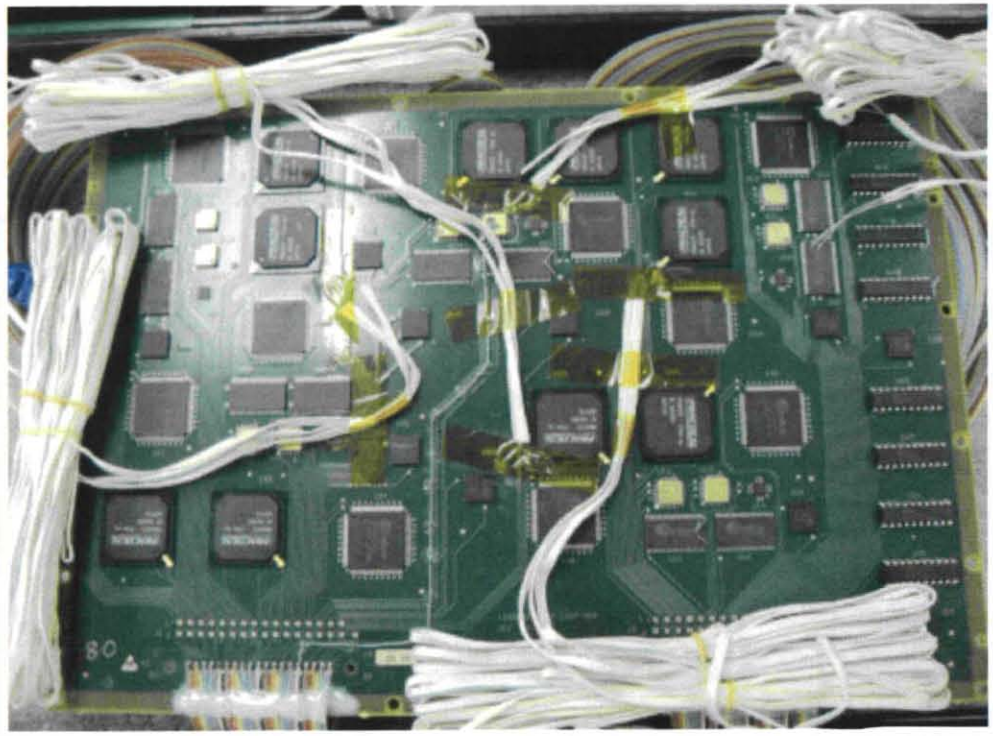
Drop Testing

CELESTICA

NSWC Crane Test Vehicles

- Shock parameters: 500 G, 2.0 ms duration (340 G for cards 80, 82, 87 for first
- 10 drops)
- Number of drops: 20
- 9 cards in total / 3 cards tested per drop
- Each card monitored for shock response
- Each card monitored for resistance
- Cards 80, 83, 86 monitored for strain



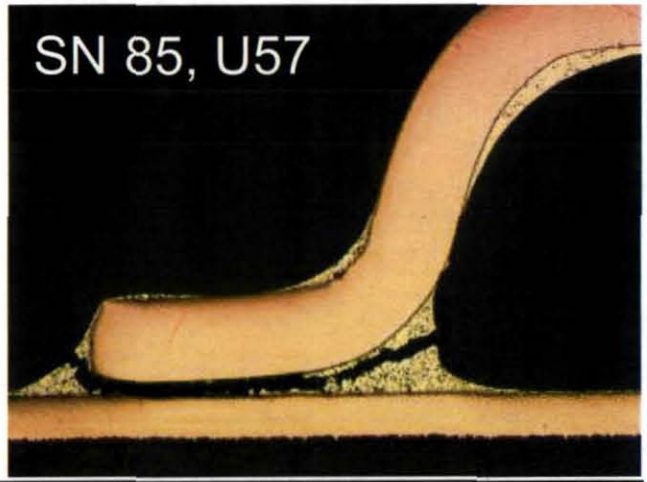


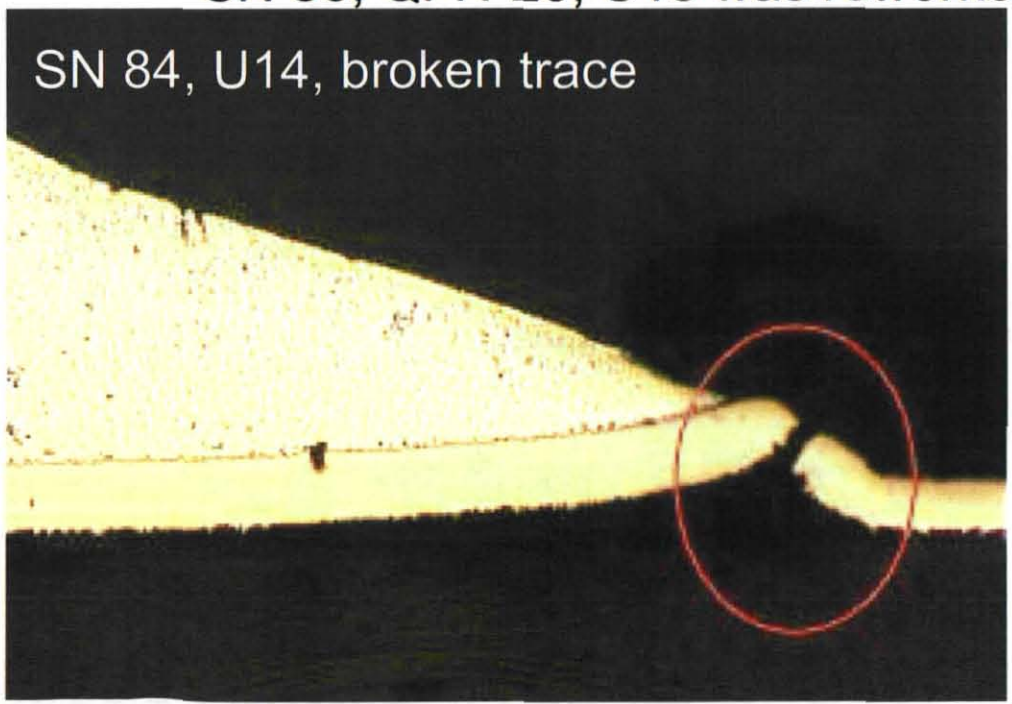
Drop Testing

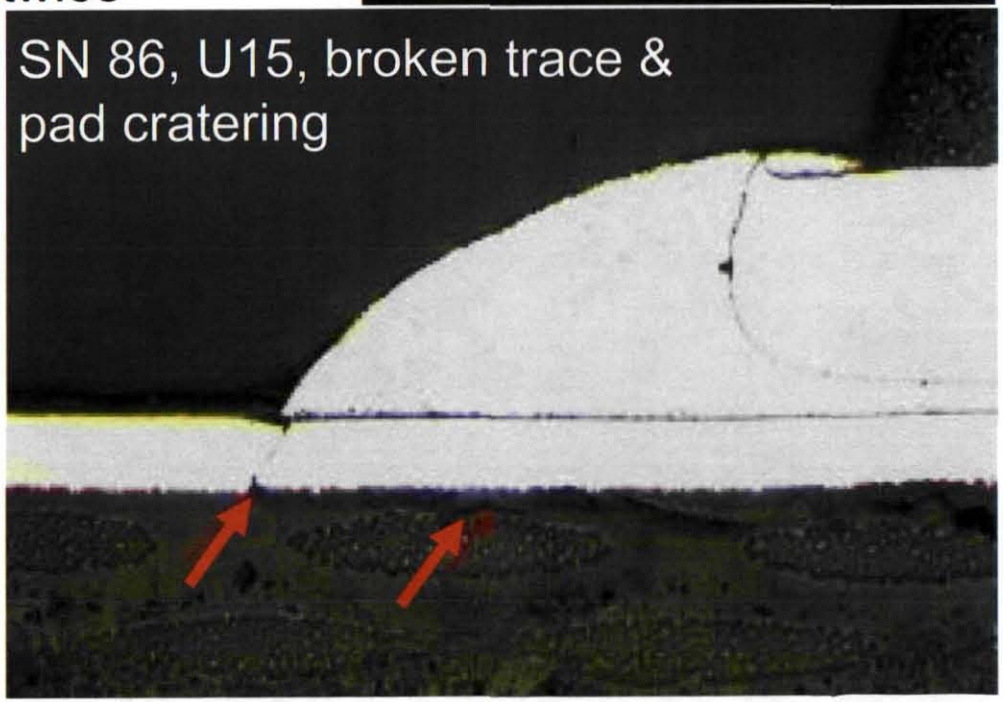
CELESTICA

NSWC Crane Test Vehicles

- Only component to have significant failures – BGA 225
- The 4 non-BGA samples that had an electrical failure had the following rework histories:
  - SN 85, TQFP 144, U57 was reworked once
  - SN 85, PDIP-20, U8 was reworked once
  - SN 84, CLCC-20, U14 was not reworked
  - SN 86, QFN-20, U15 was reworked twice



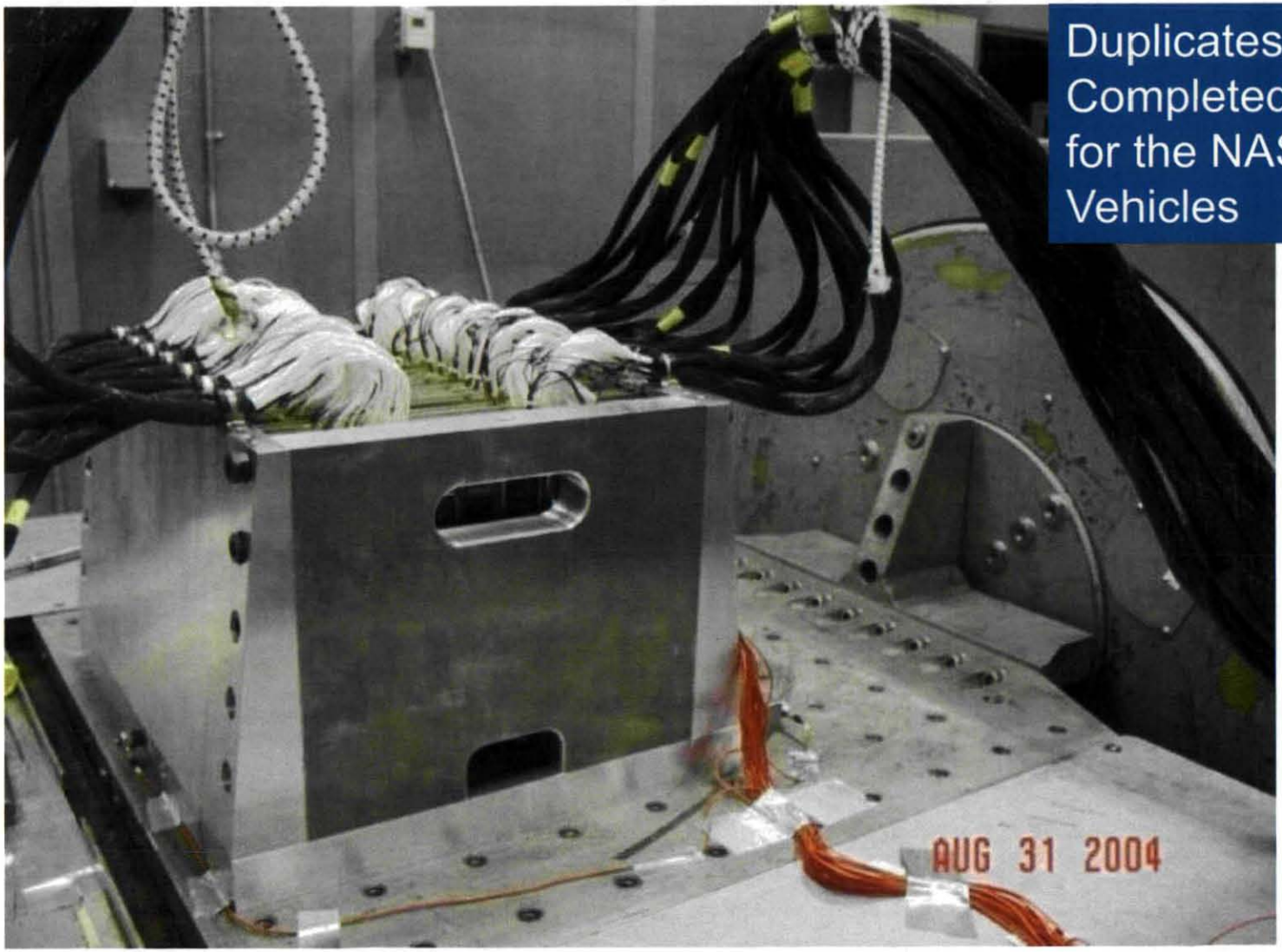




Vibration Testing

CELESTICA

Subject the test vehicles to 8.0 g_{rms} for one hour. Then increase the Z-axis vibration level in 2.0 g_{rms} increments, shaking for one hour per step until the 20.0 g_{rms} level is completed. Then subject the test vehicles to a final one hour of vibration at 28.0 g_{rms}.



Duplicates Testing Completed by Boeing for the NASA-DoD Test Vehicles

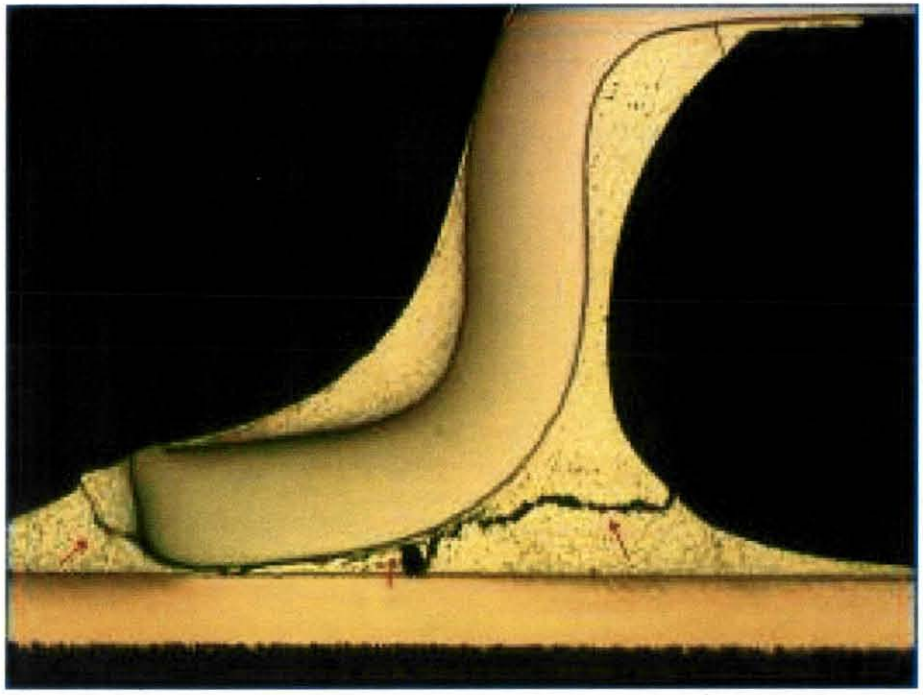
Vibration Testing

CELESTICA

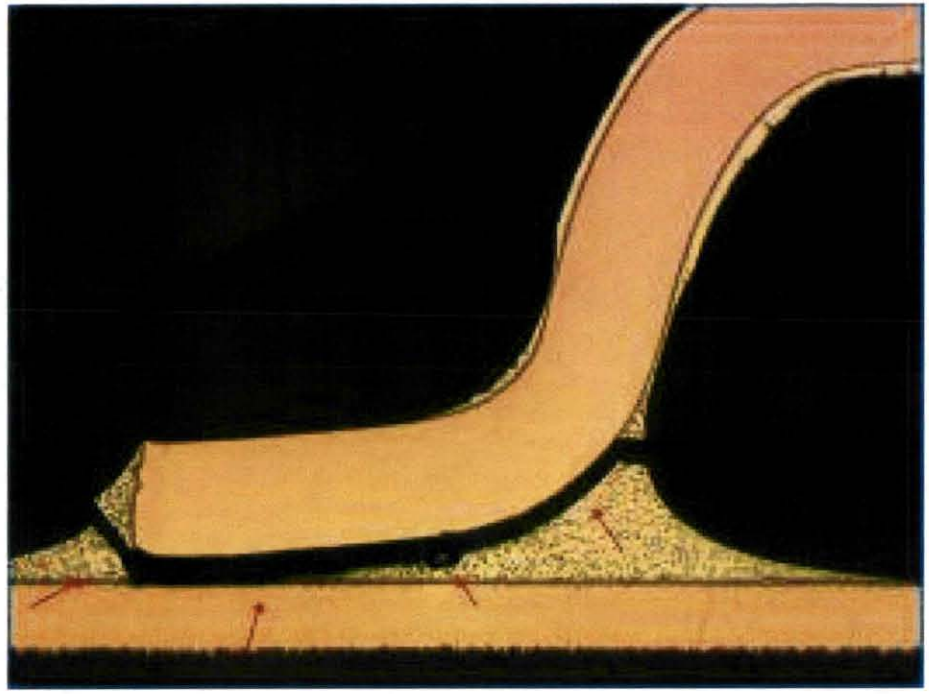
- Among the parameters tested, unexplained variation continues to dominate the results
  - Batch or Card S/N did not significantly influence the results
  - Component package style had a marked influence on both the time to failure (Tf) and on the number of cycles to 10% failure (N10)
- Rework
  - Did influence time to failure
  - Did not significantly influence N10
- Location on the board
  - Did significantly influence time to failure
  - Did not significantly influence N10

Vibration Testing

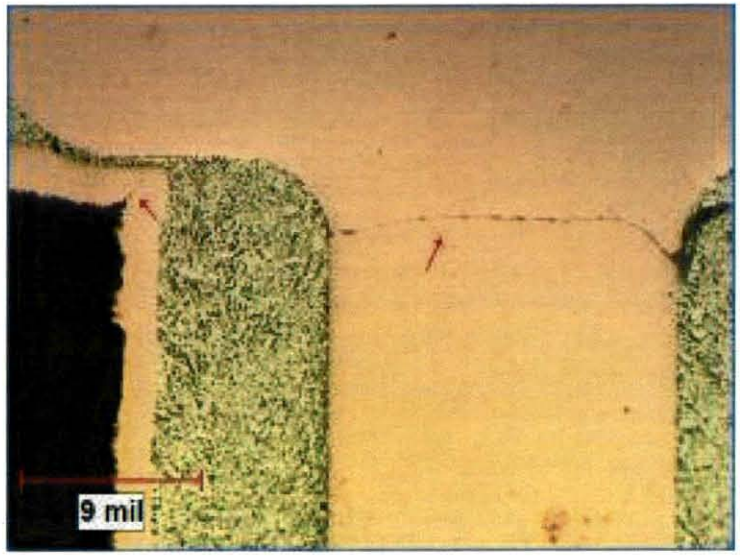
CELESTICA.



SN67, U61, left lead solder crack, 100x



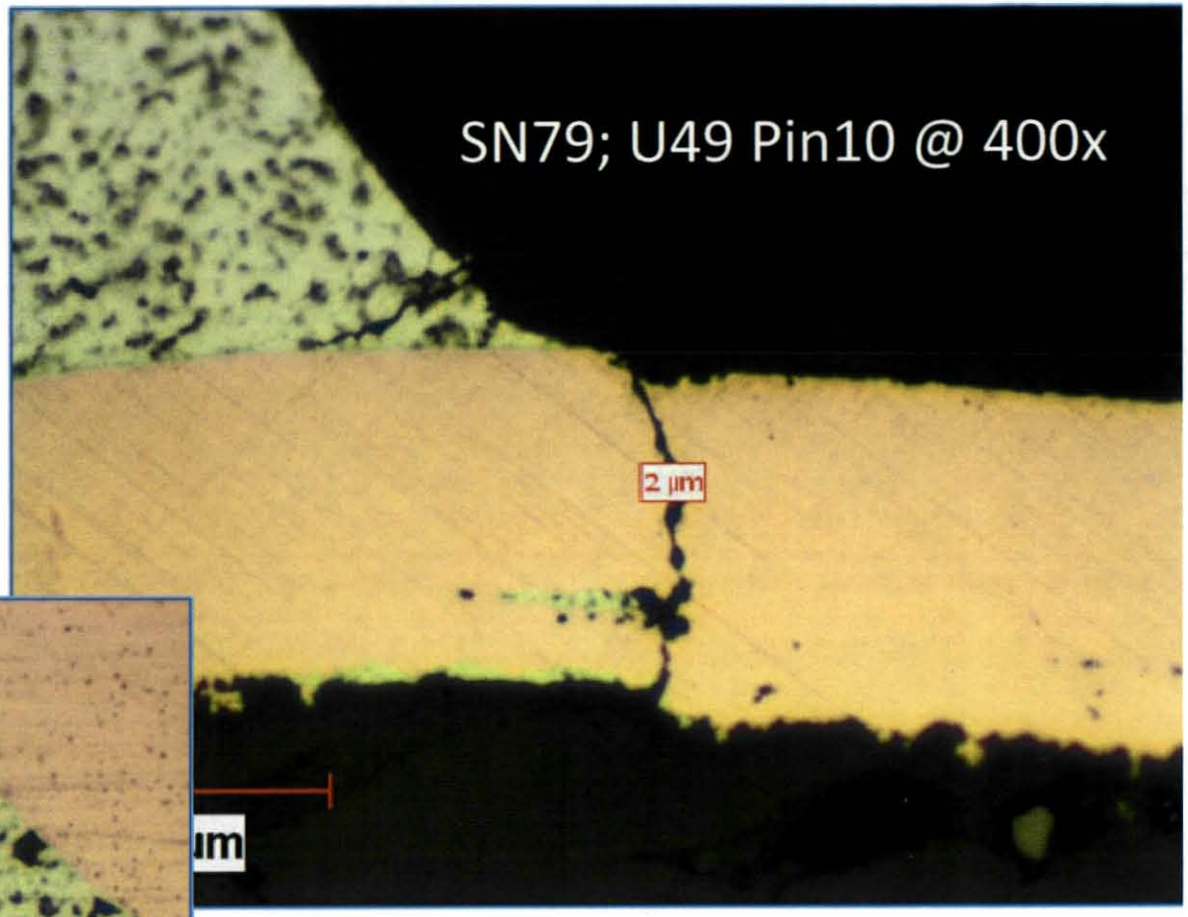
SN67, U31, left lead solder crack, 100x

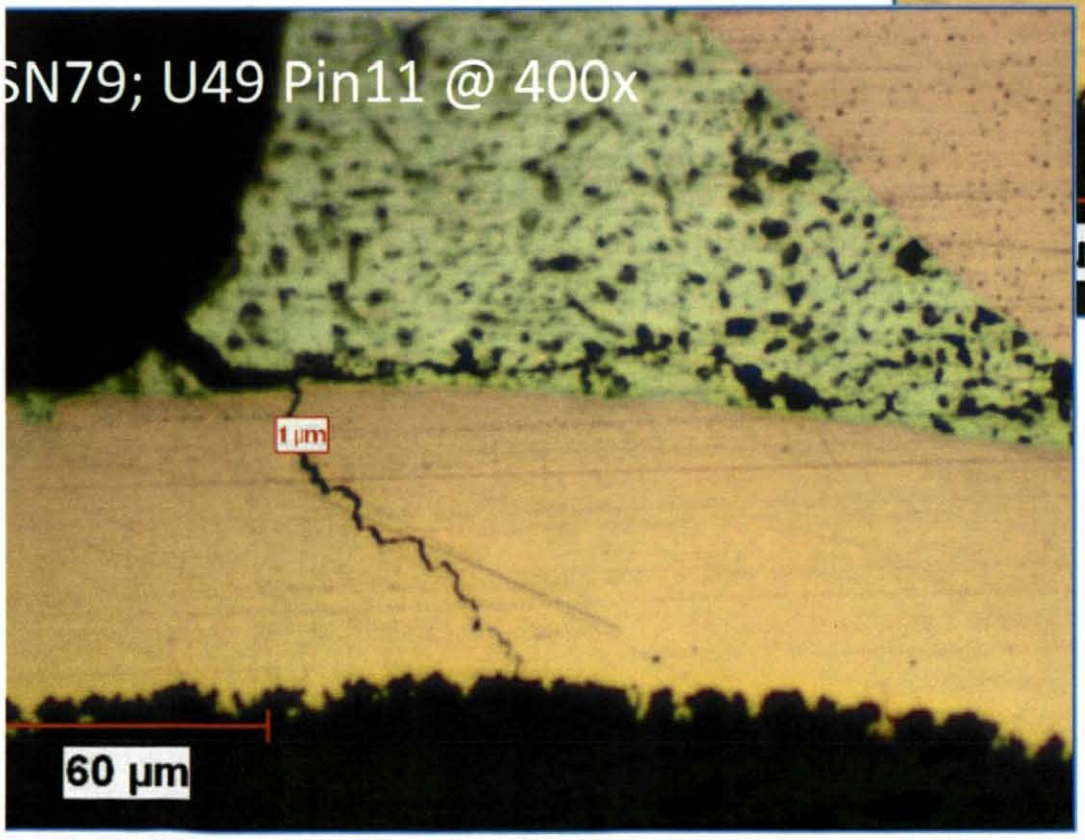


SN 79, U49, pin 11, 100x

Vibration Testing

CELESTICA





Testing Activities
NASA-DoD Test Vehicles

Specific testing details can be found in the Joint Test Protocol (JTP)
http://www.teerm.nasa.gov/projects/NASA_DODLeadFreeElectronics_Proj2.html

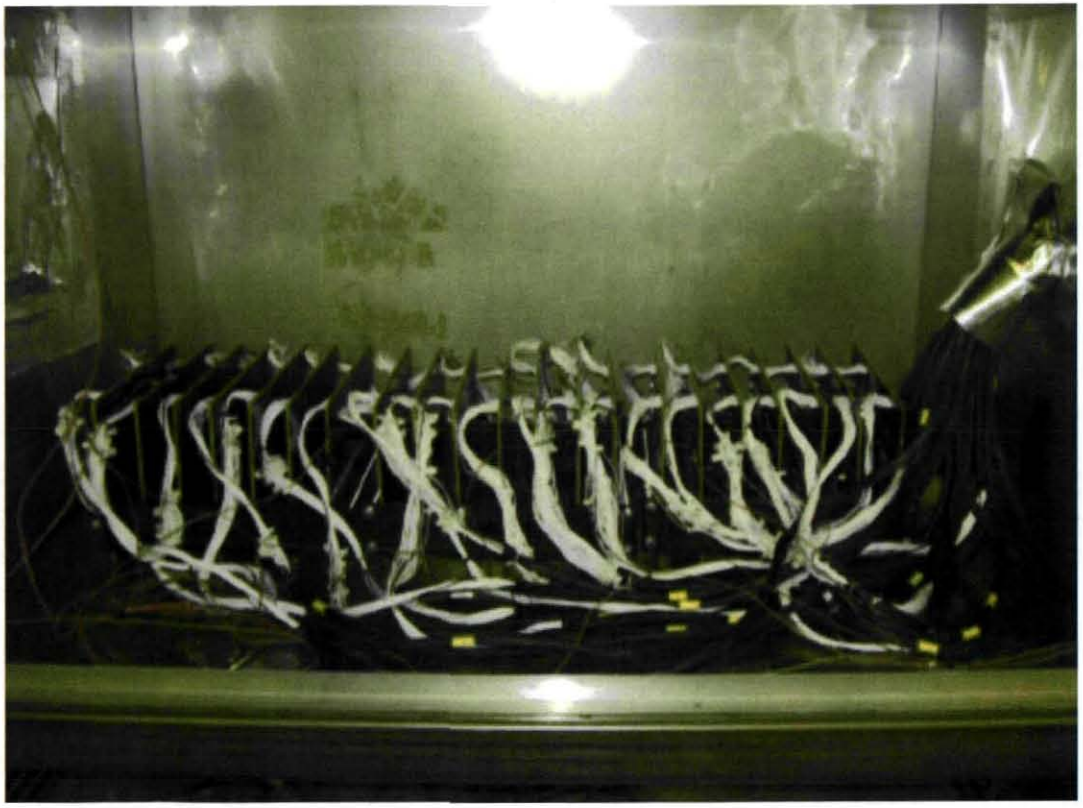
- Thermal Cycle Testing (-20/+80°C) BOEING
- Combine Environments Testing Raytheon COMPLETE
- Drop Testing CELESTICA COMPLETE
- Thermal Cycle Testing (-55/+125°C) Rockwell Collins COMPLETE
- Vibration Testing BOEING COMPLETE
- Mechanical Shock Testing BOEING COMPLETE
- Interconnect Stress Test (IST) Interconnect PWB Solutions Inc. COMPLETE
- Copper Dissolution CELESTICA Rockwell Collins

Thermal Cycle Testing (-20/+80°C)

BOEING

Test Parameters

- 5 to 10°C/minute ramp
- 30 minute dwell at 80°C
- 10 minute dwell at -20°C



~ 7,000 Thermal Cycles Completed

Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Test Parameters

- 5 to 10°C/minute ramp
- 30 minute dwell at 125°C
- 10 minute dwell at -55°C

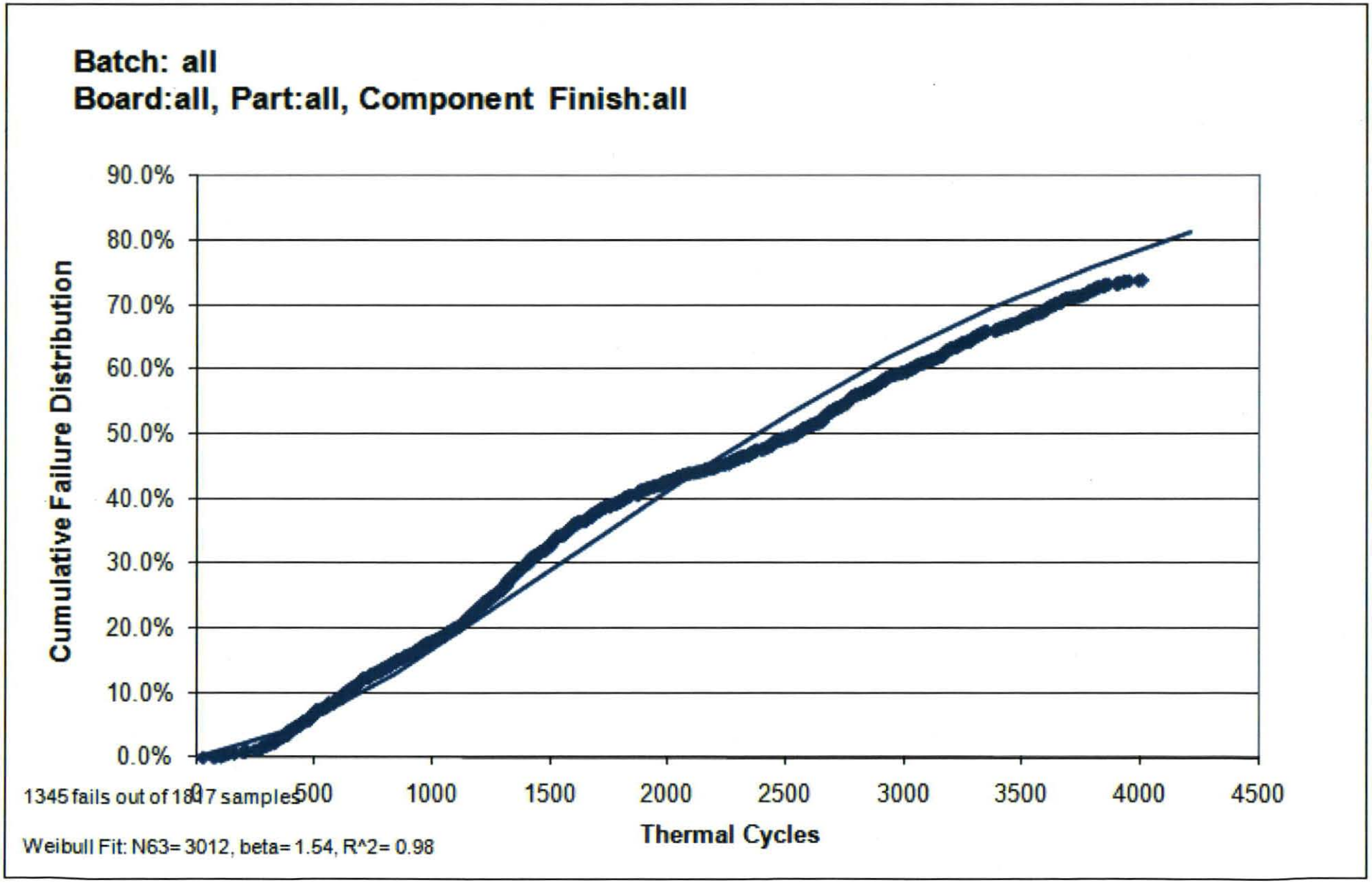
~4,000 Thermal Cycles Completed

Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Data Snapshot from "Manufactured" Test Vehicles

- No "Rework" Data

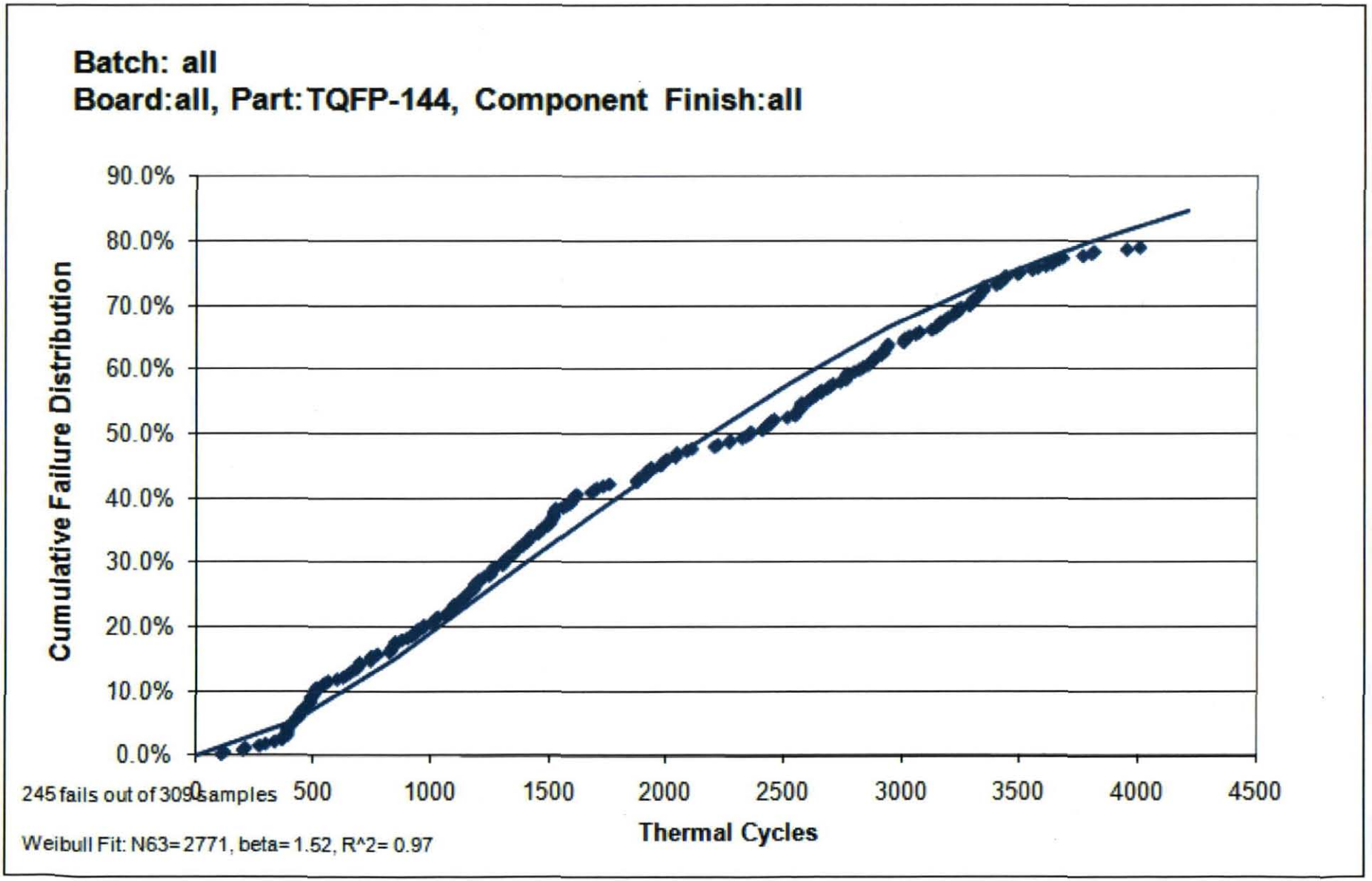


Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Data Snapshot from "Manufactured" Test Vehicles

- No "Rework" Data
- TQFP-144

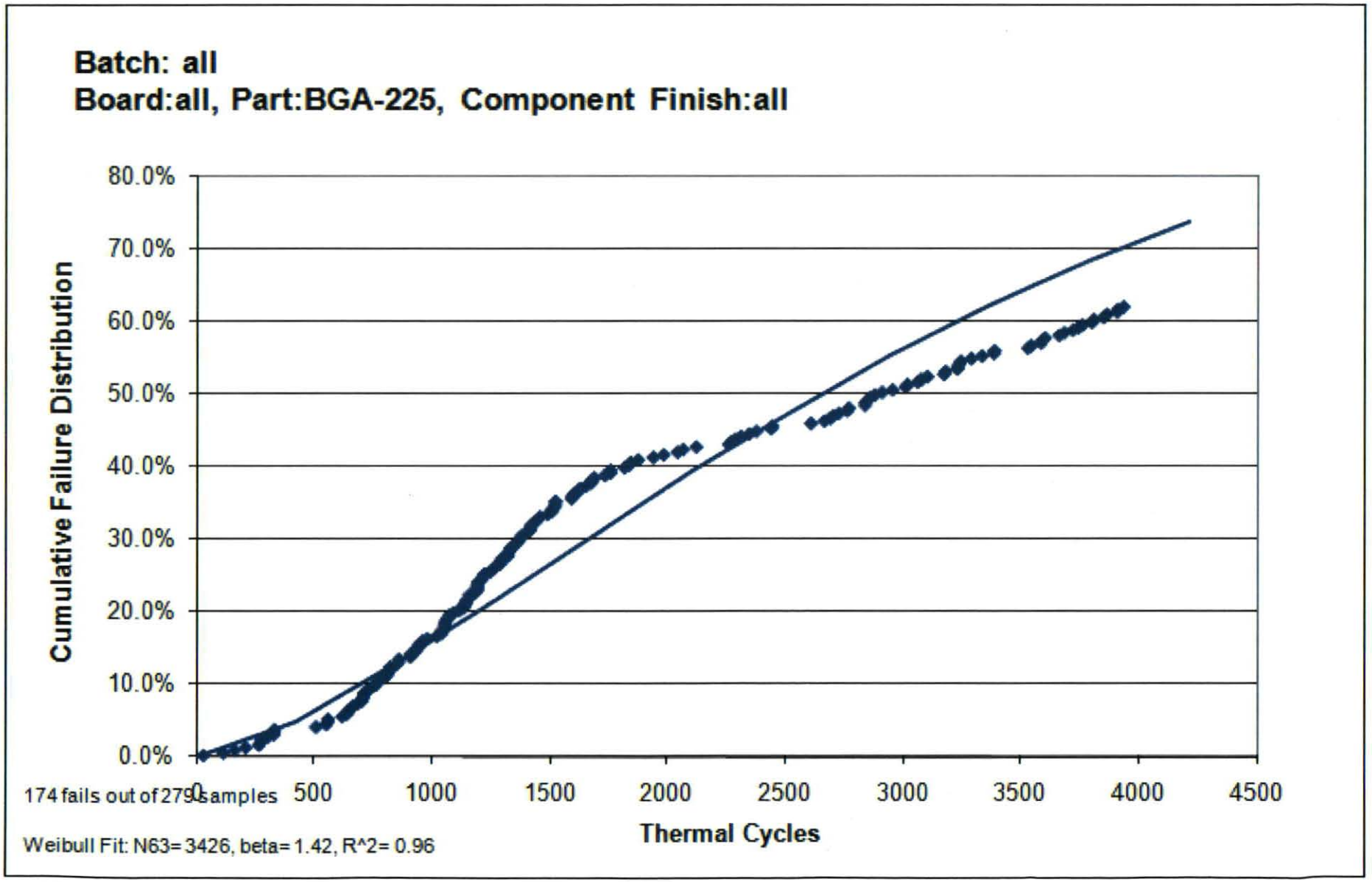


Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Data Snapshot from "Manufactured" Test Vehicles

- No "Rework" Data
- BGA-225

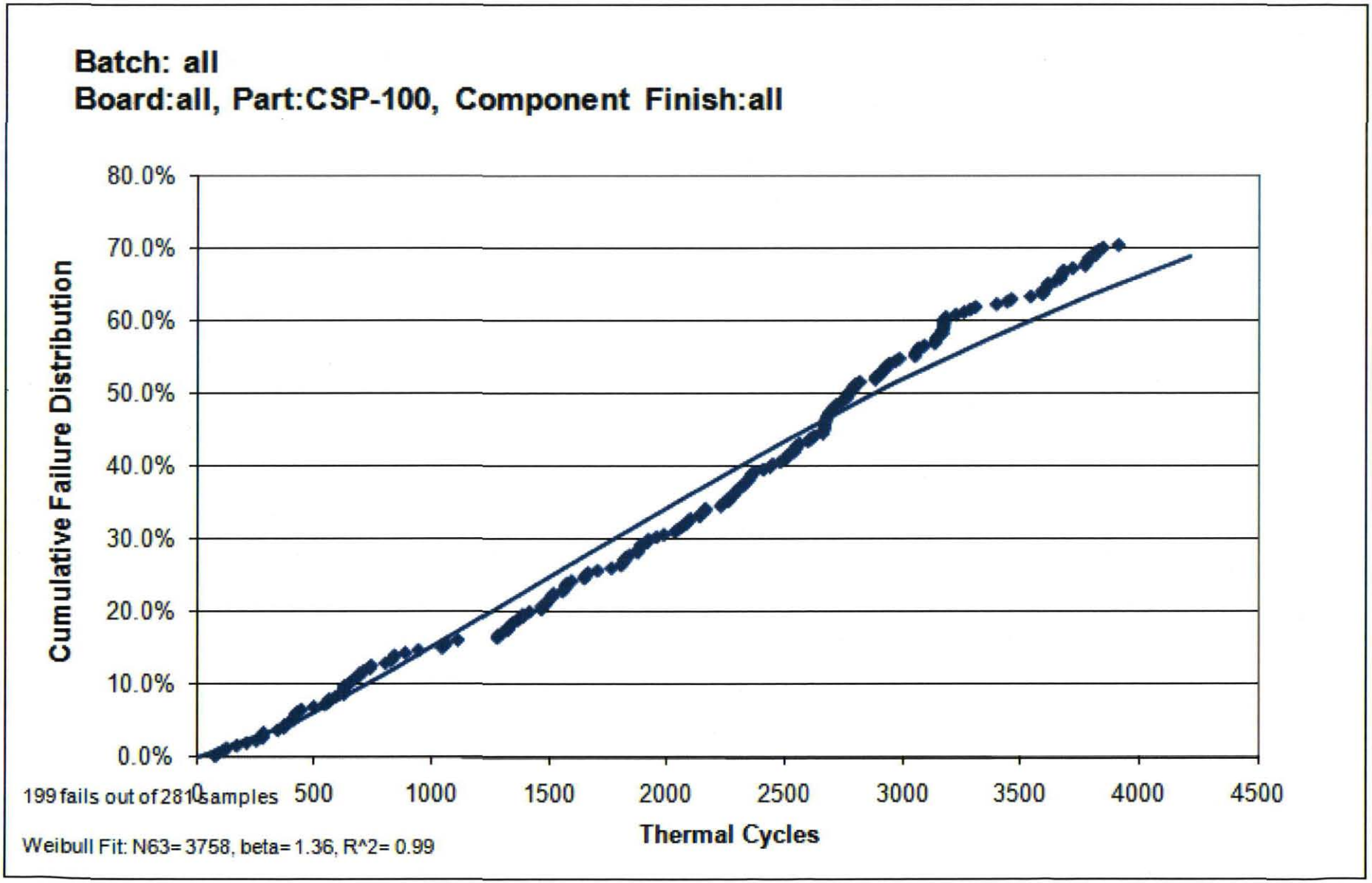


Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Data Snapshot from "Manufactured" Test Vehicles

- No "Rework" Data
- CSP-100

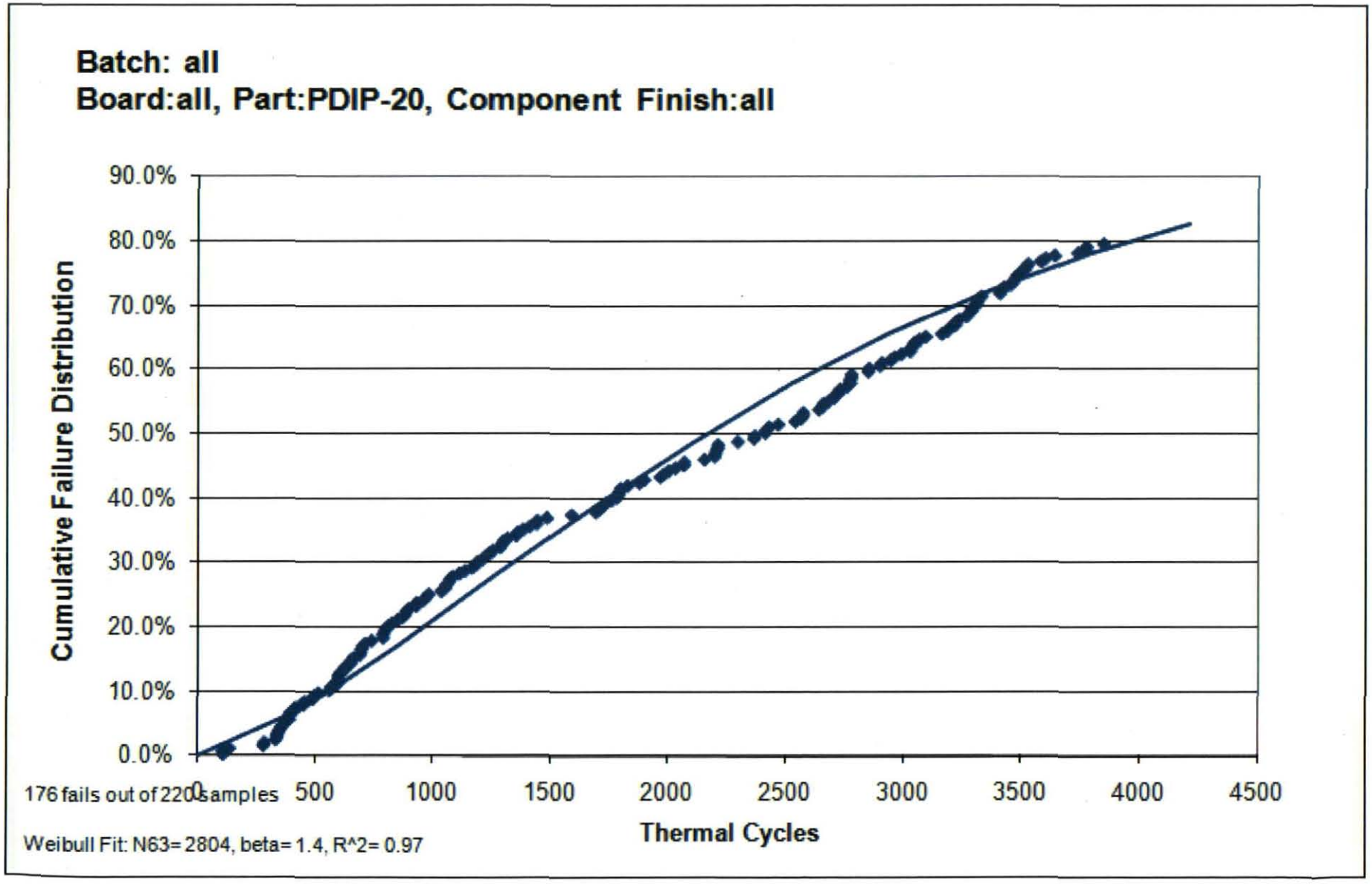


Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Data Snapshot from "Manufactured" Test Vehicles

- No "Rework" Data
- PDIP-20

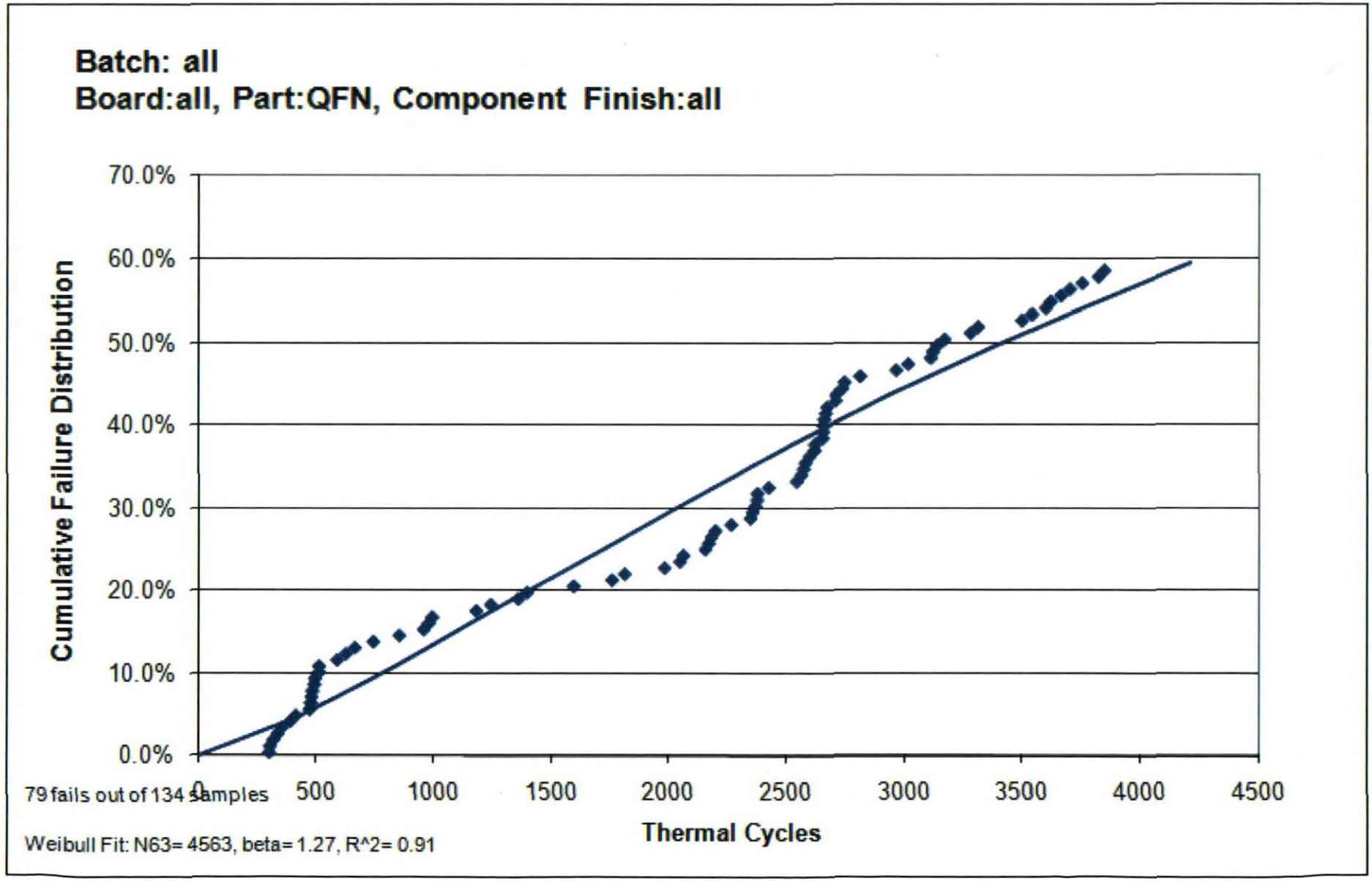


Thermal Cycle Testing (-55/+125°C)

Rockwell Collins

Data Snapshot from "Manufactured" Test Vehicles

- No "Rework" Data
- QFN

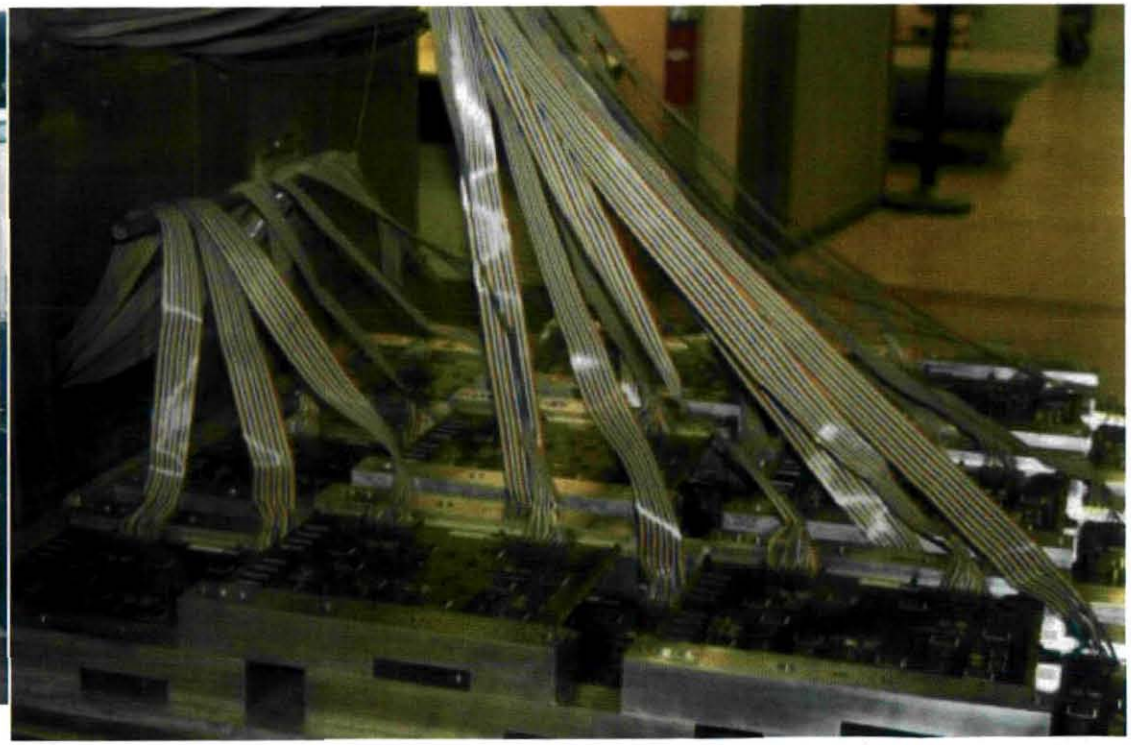


Combine Environments Testing

Raytheon

Thermal Cycle with Vibration

- -55°C to +125°C
- 20°C/minute ramp
- 15 minute dwell at -55°C and +125°C
- Vibration for the duration of the thermal cycle
- 10 g_{rms} pseudo-random vibration initially
- Increase vibration level 5 g_{rms} after every 50 cycles
- 55 g_{rms} maximum

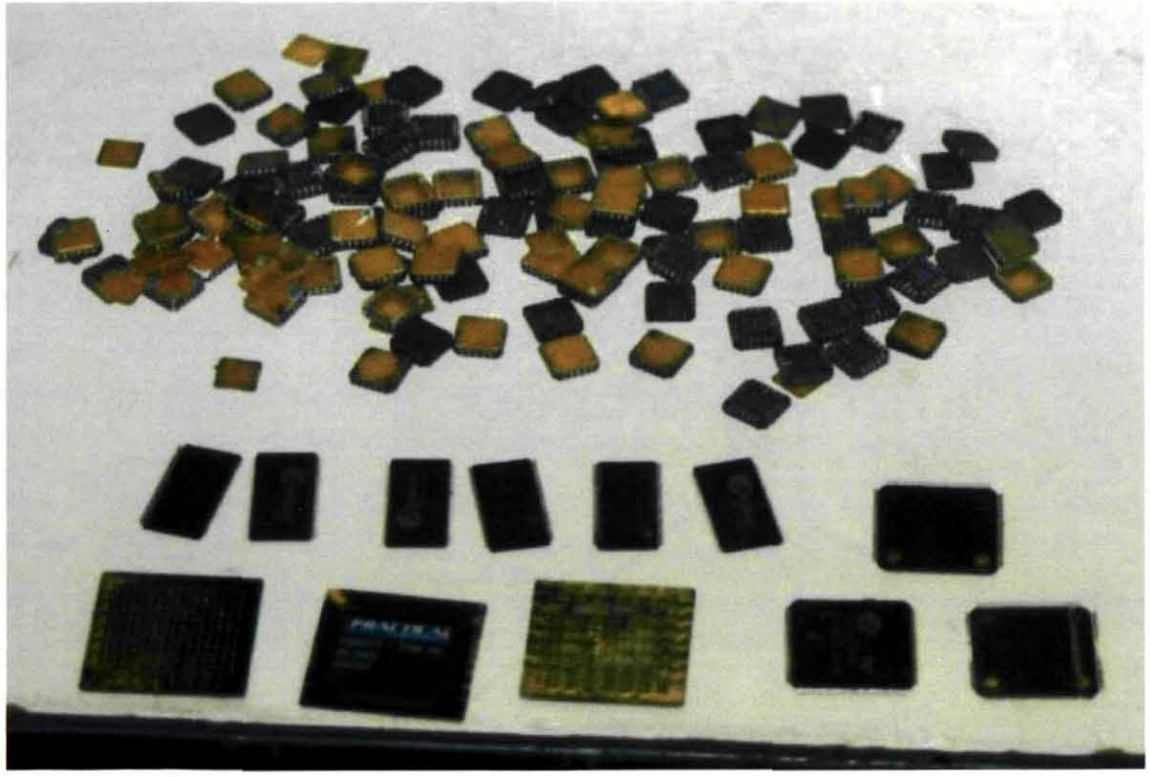


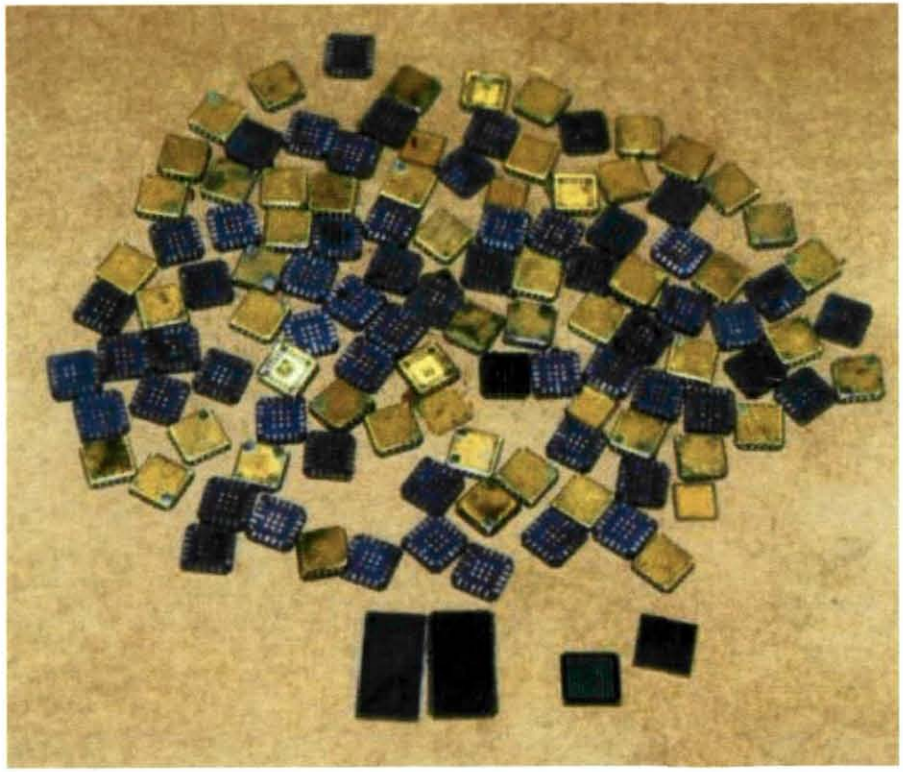
Combine Environments Testing

Raytheon

Overall, the component type had the greatest effect on solder joint reliability performance.

- The plated-through-hole components proved to be more reliable than the surface mount technology components.
- The plated-through-holes (PTH), PDIP-20, TQFP-144 and QFN-20 components per-formed the best.
- The BGA-225 components performed the worst.





Combine Environments Testing

Raytheon

Solder alloy had a secondary effect on solder joint reliability.

- In general, tin-lead finished components soldered with tin-lead solder paste were the most reliable with the exception of some components with lead contamination in the solder joints.
- In general, tin-silver-copper soldered components were less reliable than the tin-lead solder controls.
- In several cases, tin-silver-copper solder performed statistically as good as or equal to the baseline, eutectic tin-lead solder.

In general, reworked components were less reliable than the unreworked components. This is especially true with reworked lead-free CSP-100, reworked lead-free BGA-225

Combine Environments Testing

Raytheon

From this testing, it appears the selection of component type and lead-free solder combinations should be considered critical factors when considering converting to lead-free solder assembly, especially for surface mount technology design configurations.

Manufactured Test Vehicles

Board Finish	Component	Finish	Solder	Number of Failed Components
Im. Ag	BGA-225	SAC405	SAC305	76% (19 of 25)
			SN100C	76% (19 of 25)
			SnPb	92% (23 of 25)
		SnPb	SAC305	84% (21 of 25)
			SN100C	88% (22 of 25)
			SnPb	60% (15 of 25)
Im. Ag	CLCC-20	SAC305	SAC305	96% (24 of 25)
			SN100C	96% (24 of 25)
			SnPb	92% (23 of 25)
		SnPb	SAC305	100% (25 of 25)
			SN100C	88% (22 of 25)
			SnPb	84% (21 of 25)
Im. Ag	QFN-20	Matte Sn	SAC305	20% (5 of 25)
			SN100C	40% (10 of 25)
			SnPb	20% (5 of 25)
Im. Ag	TQFP-144	Matte Sn	SAC305	24% (6 of 25)
			SN100C	52% (13 of 25)
			SnPb	32% (8 of 25)
		SnPb Dip	SAC305	0% (0 of 25)
			SN100C	60% (15 of 25)
			SnPb	8% (2 of 25)

Combine Environments Testing

Raytheon

Rework Test Vehicles

Board Finish	Component	Finish	Solder	New Component Finish	Rework Solder	Number of Failed Components
Im. Ag	BGA-225	SAC405	SAC305	SAC405	Flux Only	60% (9 of 15)
					SnPb	33% (5 of 15)
			SnPb			50% (10 of 20)
		SnPb	SAC305			65% (13 of 20)
			SnPb	SAC405	SnPb	80% (12 of 15)
				SnPb	Flux Only	20% (3 of 15)
Im. Ag	PDIP-20	NiPdAu	SnPb			7% (1 of 15)
		Sn	SN100C	Sn	SN100C	20% (2 of 10)
						7% (2 of 30)
			SnPb			13% (2 of 15)
		SnPb	SnPb	Sn	SnPb	40% (4 of 10)
Im. Ag	TSOP-50	Sn	SAC305	Sn	SnPb	60% (6 of 10)
			SnPb			20% (3 of 15)
		SnBi	SAC305	SnBi	SAC305	90% (9 of 10)
						67% (10 of 15)
			SnPb			33% (5 of 15)
		SnPb	SAC305			33% (5 of 15)
			SnPb	Sn	SnPb	50% (5 of 10)
				SnPb	SnPb	60% (6 of 10)

Combine Environments Testing

Raytheon

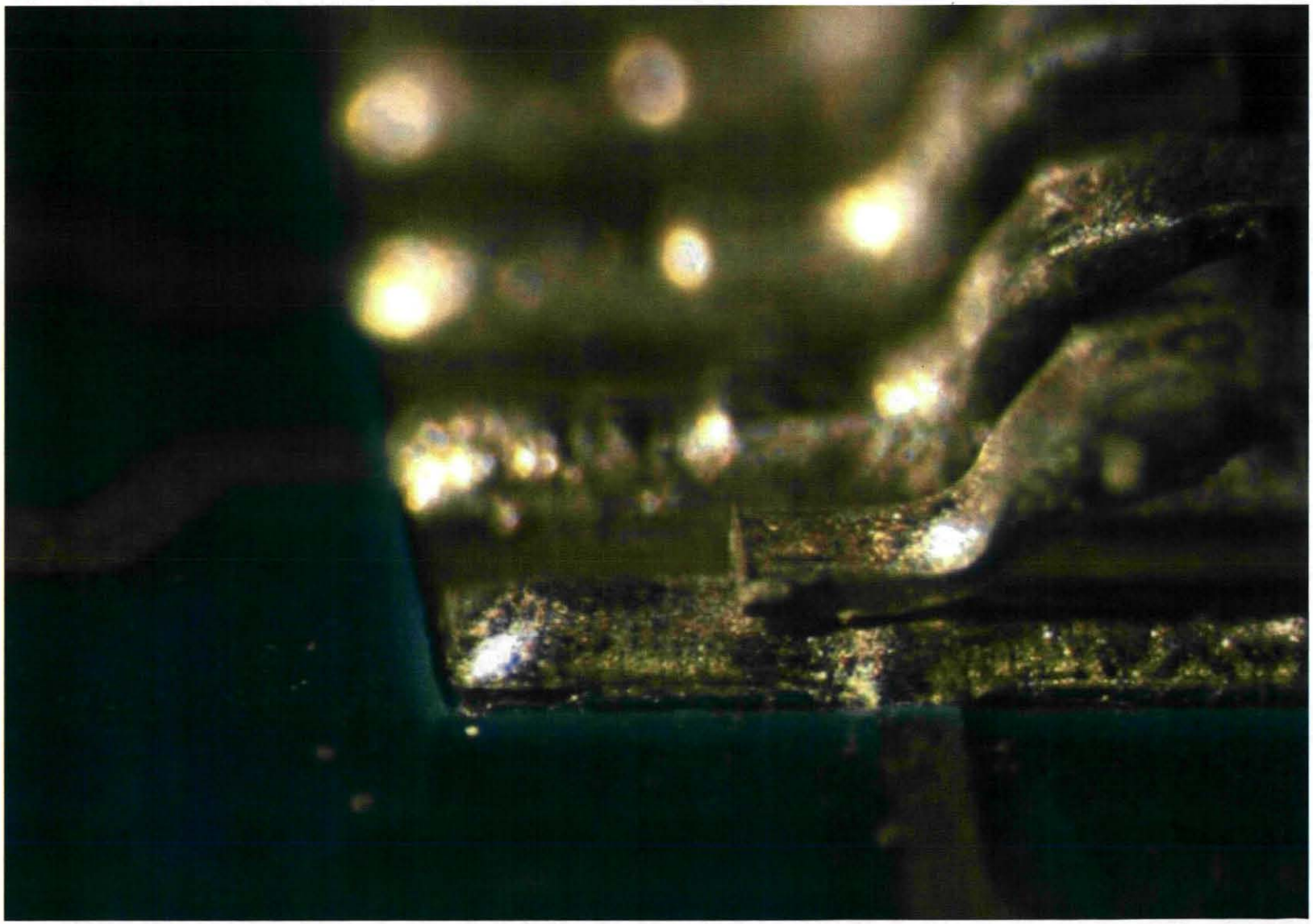
Failure Analysis In-Progress

Failure Analysis Location	Test Vehicle	Component Location	Selection Criteria
COM DEV	21	U34	Mfg group - No signal, failed at 0 cycles
	21	U57	Mfg group - Failed at cycle 1
	119	U36	Mfg group - Surrounded by components that fell off; failed at 233 cycles
	119	U39	Mfg group - Surrounded by components that fell off; failed at 318 cycles
	142	U13	Rwk group - Adjacent to rwked components, survived all 650 cycles
	181	U56	Rwk group - Rwked component failed at cycle 1
	181	U25	Rwk group - Rwked component failed at cycle 1
Lockheed Martin	117	U4	Mfg group - Failed at 20 cycles; SN100C solder paste used
	140	U11	Rwk group - Damaged pad from rwk - Failed at 398 cycles
	183	U41	Rwk group - Failed at cycle 1, was not rwked
Nihon Superior	23	U30	Mfg group - Survived 650 cycles, surrounded by components that fell off
	23	U43	Mfg group - Failed at 120 cycles, located near center of TV
	72	U29	Mfg group - Location in chamber (low fails); failed at 161 cycles
	158	U6	Rwk group - Rwked component failed at cycle 1
	180	U21	Rwk group - Rwked component failed at cycle 1

Combined Environments Failure Analysis

COM DEV

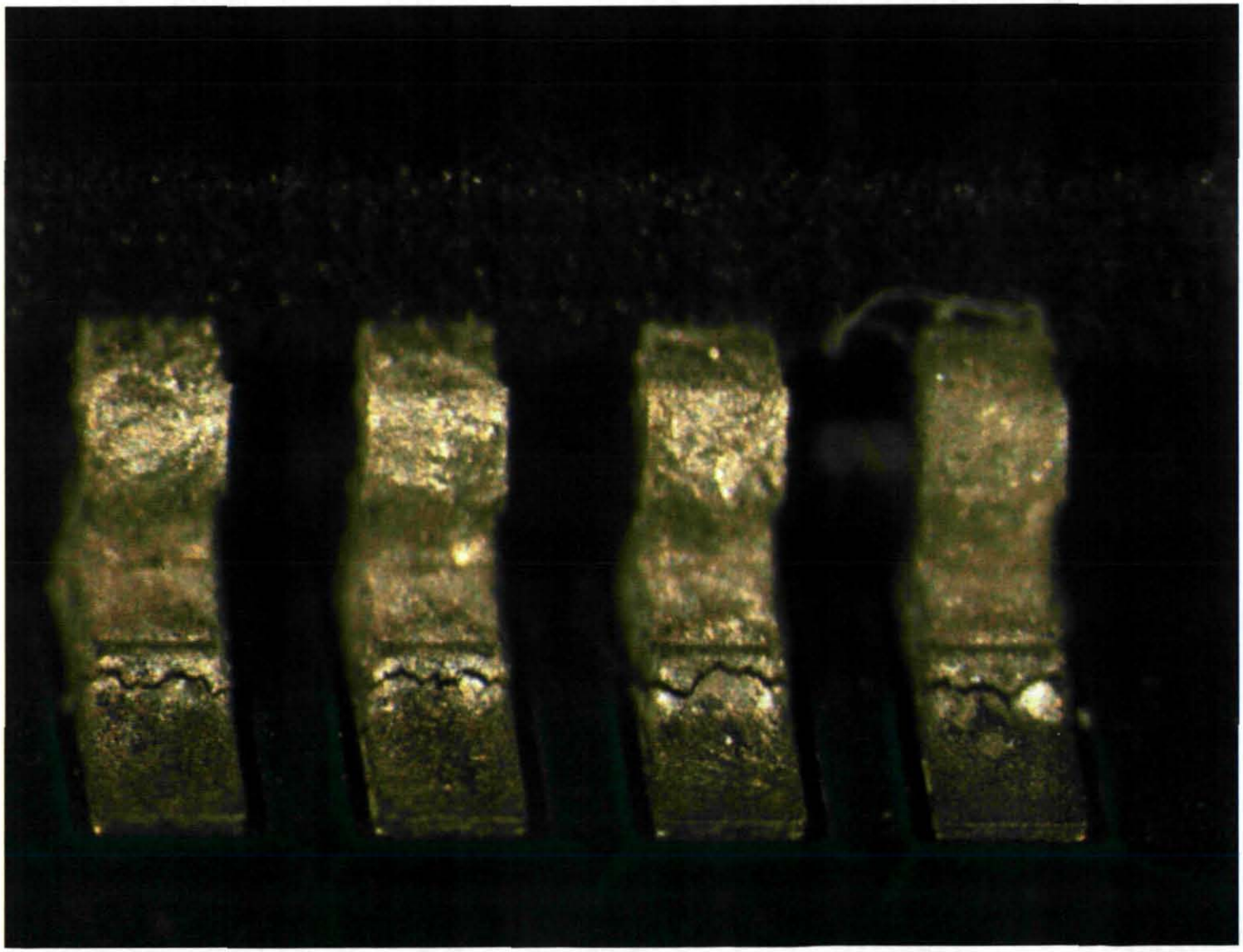
Test Vehicle 21; Component U34 – TQFP 144; Board Finish – Imm. Ag
SnPb Manufactured (Batch C) - Solder (SnPb) - Component Finish (SnPb Dip): No signal, failed at 0 cycles



Combined Environments Failure Analysis

COM DEV

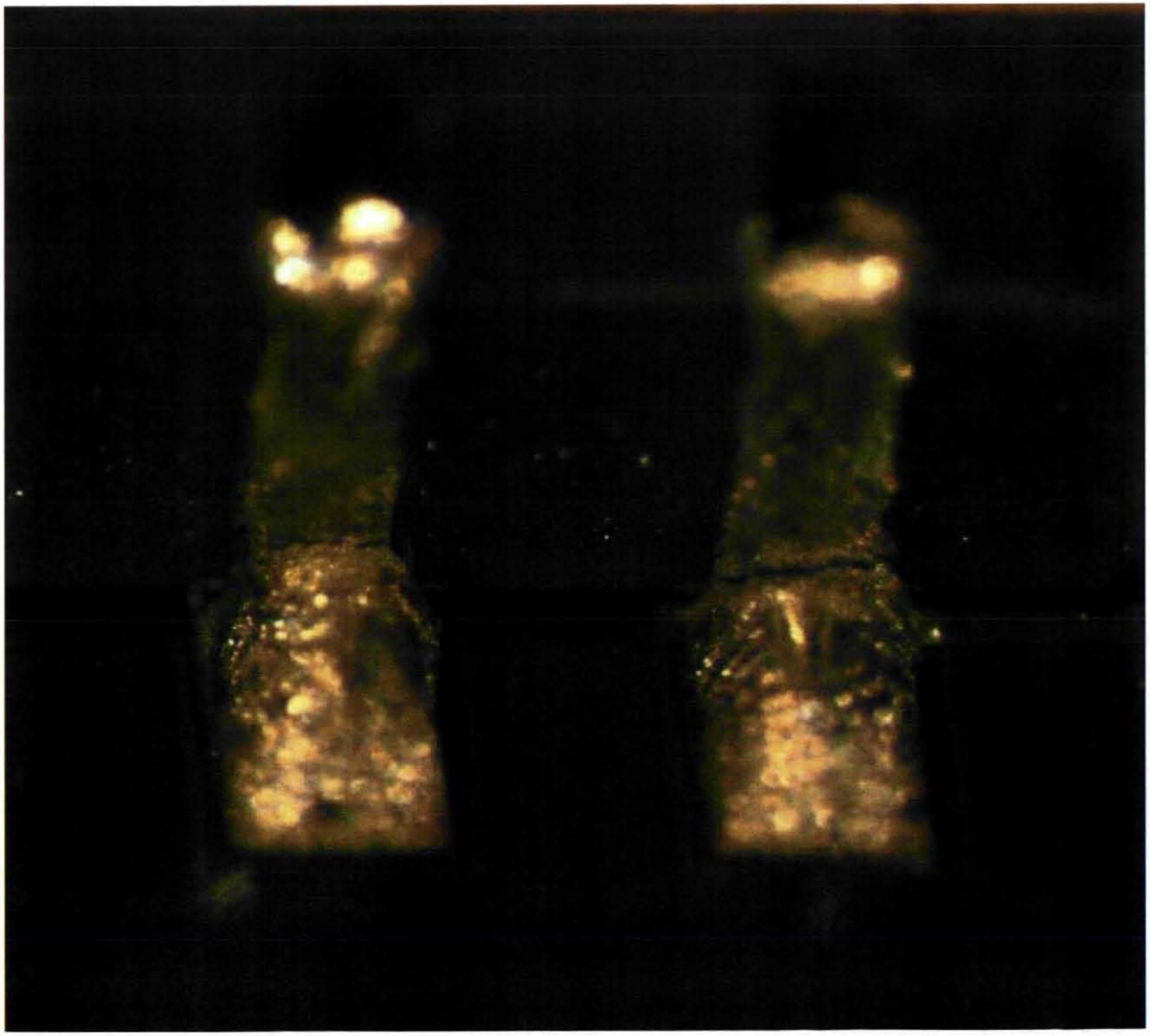
Test Vehicle 119; Component U39 – TSOP 50; Board Finish – Imm. Ag
Lead-Free Manufactured (Batch G) - Solder (SN100C) - Component Finish (SnPb)
Surrounded by components that fell off; failed at 318 cycles



Combined Environments Failure Analysis

COM DEV

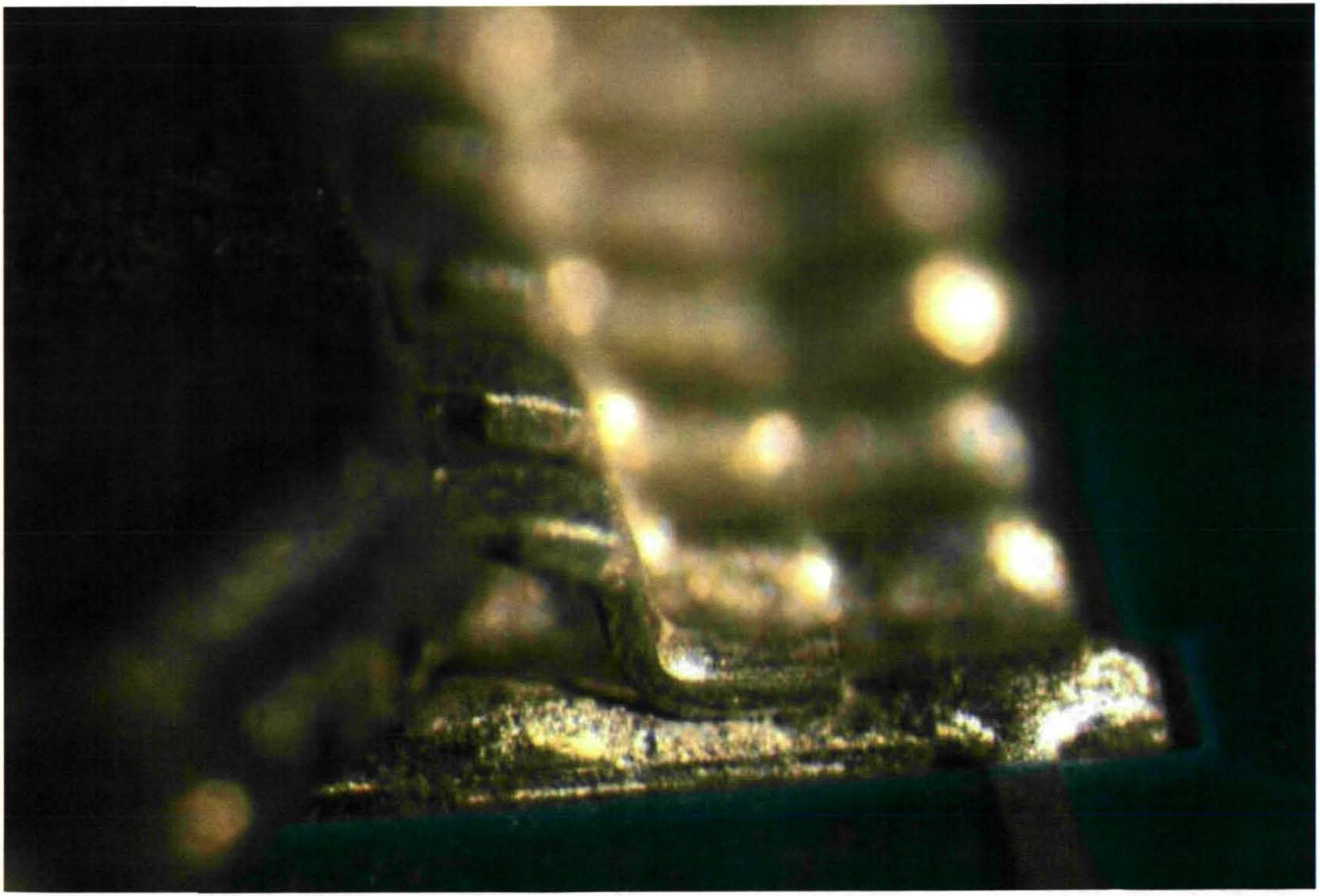
Test Vehicle 142; Component U13 – CLCC; Board Finish – Imm. Ag
SnPb Rework (Batch B) - Solder (SnPb) - Component Finish (SAC305)
Adjacent to reworked components, survived all 650 cycles



Combined Environments Failure Analysis

COM DEV

Test Vehicle 21; Component U57 – TQFP 144; Board Finish – Imm. Ag
SnPb Manufactured (Batch C) - Solder (SnPb) - Component Finish (SnPb Dip)
Failed at cycle 1

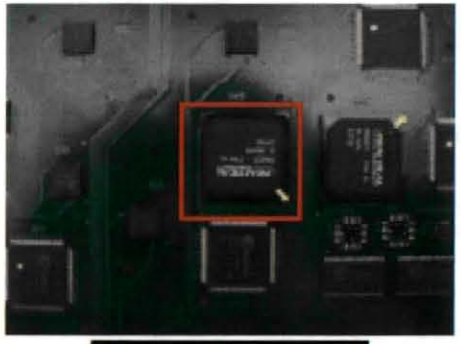


Combined Environments Failure Analysis

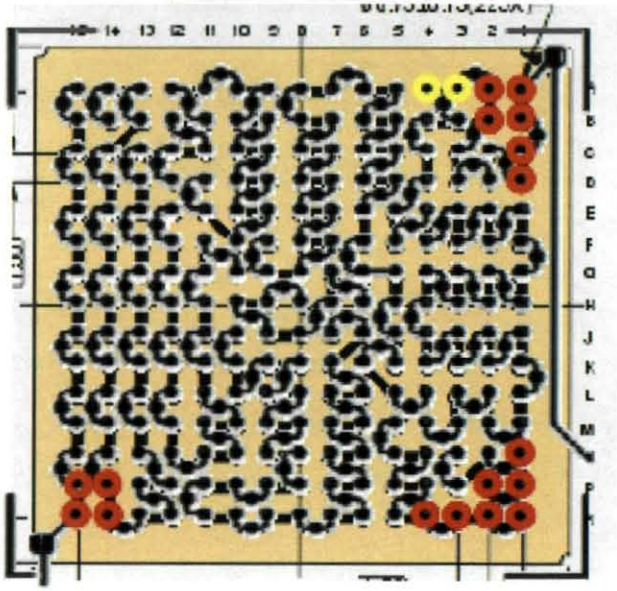
your partner for soldering solution
NIHON SUPERI

Test Vehicle 23

SnPb Manufactured
Ag-SnPb-SnPb

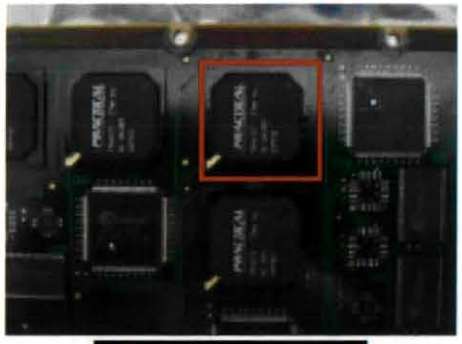


② U43(BGA225)

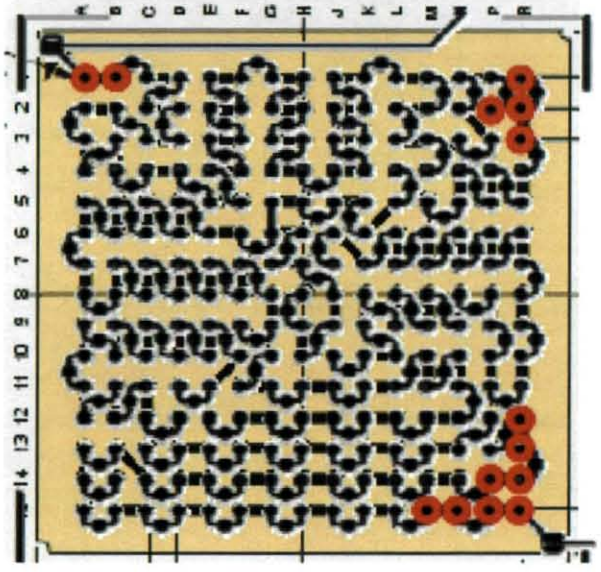


Test Vehicle 158

SnPb REWORK
ENIG-SnPb-SnPb

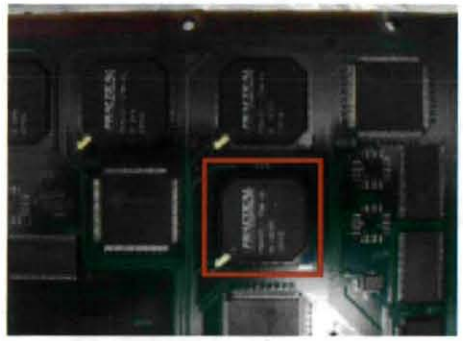


④ U6(BGA225)

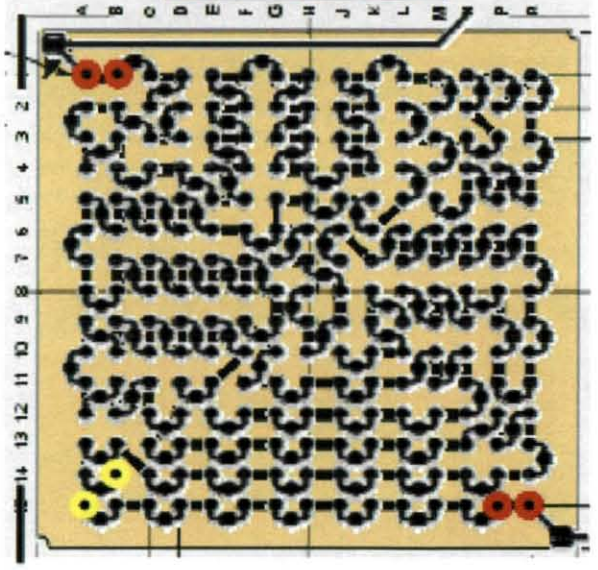


Test Vehicle 180

Pb-Free REWORK
Ag-SAC305-SnCu



⑤ U21(BGA225)

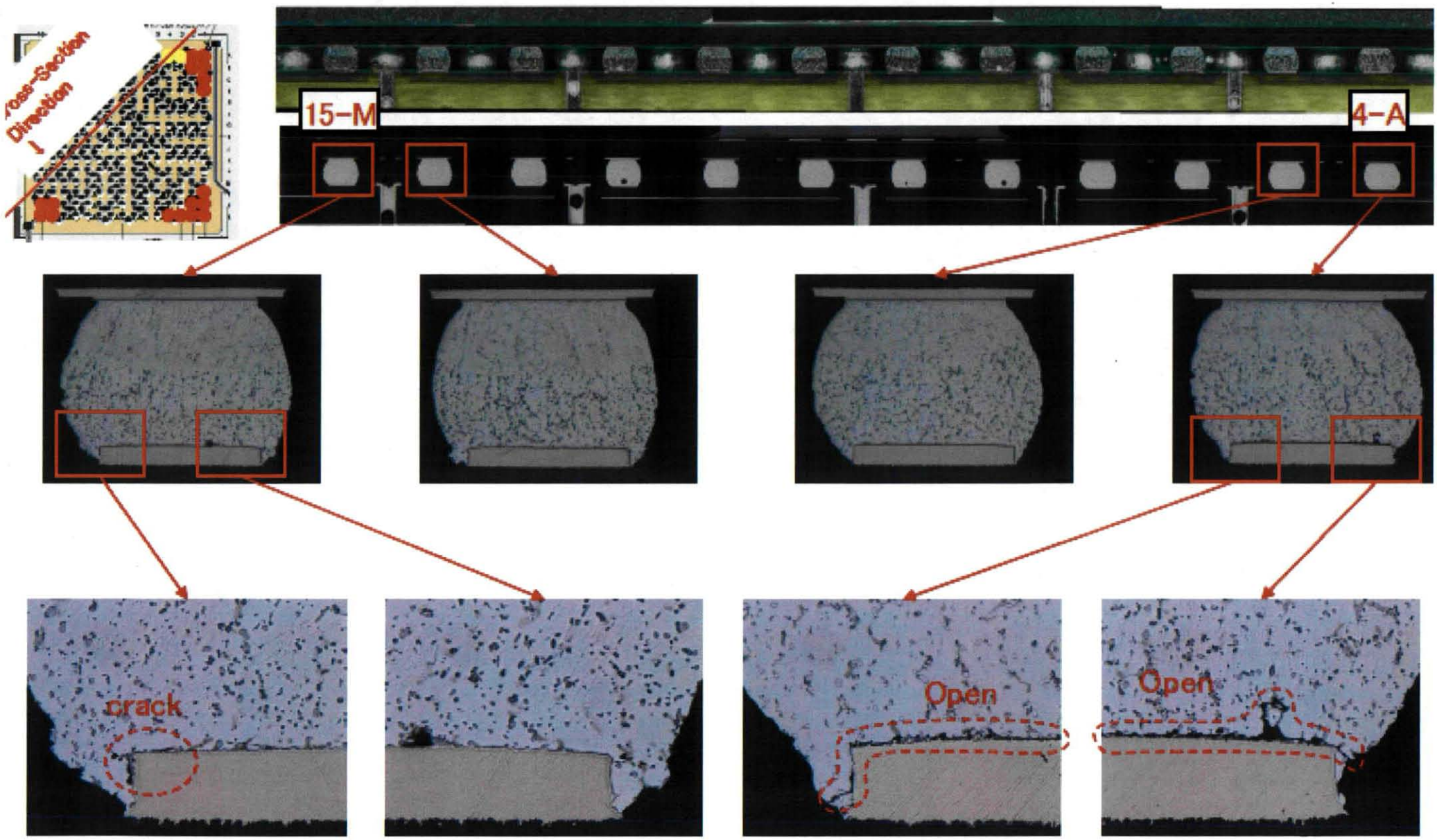


:Open
:High resistance

Combined Environments Failure Analysis

NIHON SUPERI

SAC405 solder balls / SnPb solder paste / SnPb reflow profile



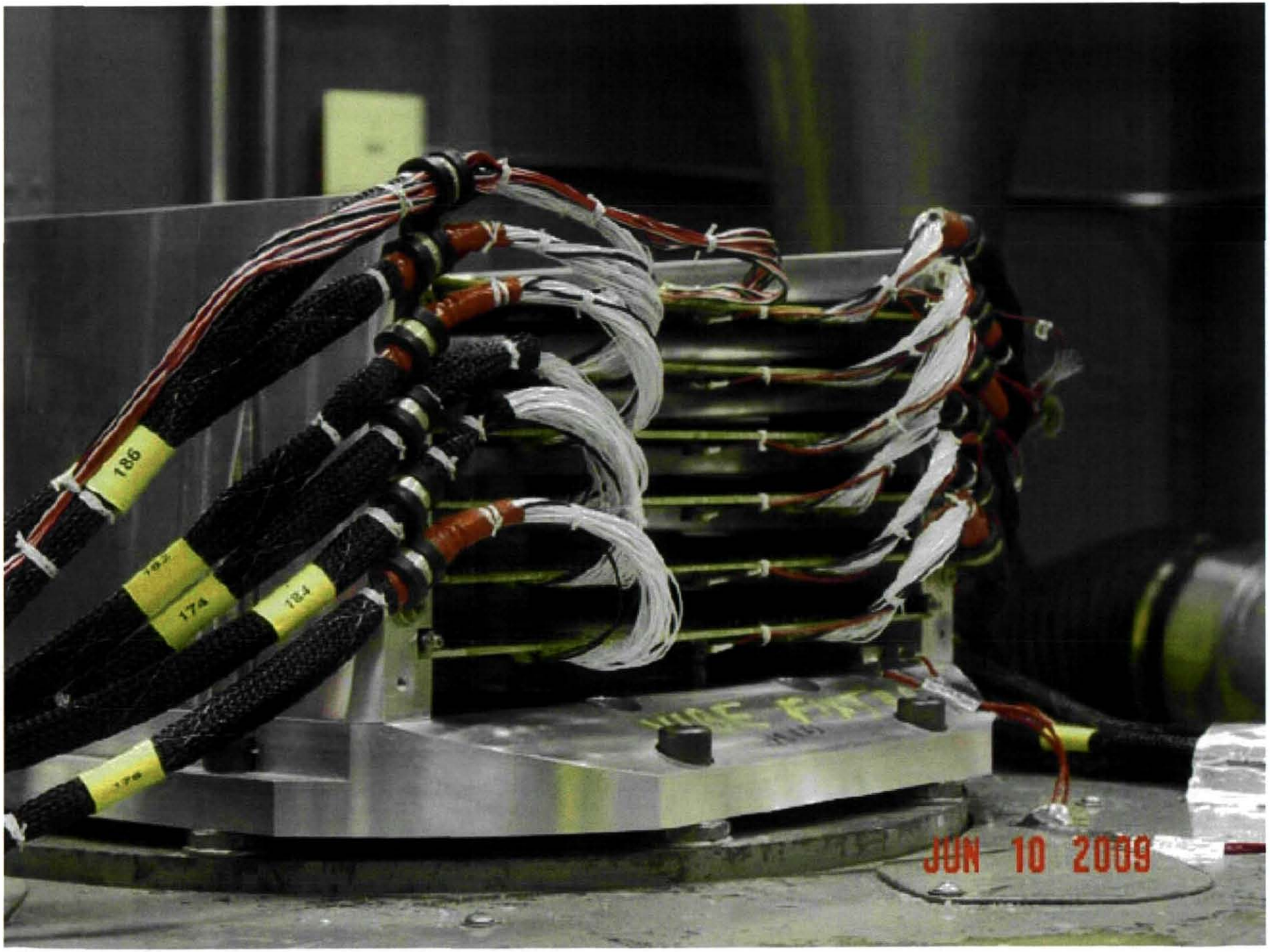
Mechanical Shock Testing

Project representatives felt that only testing in the Z-axis was required as this is the only axis which allows significant board bending and subsequent solder joint failures.

Parameters	The shock transients will be applied perpendicular to the plane of the board and will be increased after every 100 shocks (i.e., a step stress test). For Level 6 (300 G's), 400 shocks will be applied. Frequency range is 40 to 1000 Hz. SRS damping: 5%			
	Test Shock Response Spectra	Amplitude (G's)	Te (msec)	Shocks per Level
	Modified Functional Test for Flight Equipment (Level 1)	20	<30	100
	Modified Functional Test for Ground Equipment (Level 2)	40	<30	100
	Modified Crash Hazard Test for Ground Equipment (Level 3)	75	<30	100
	Level 4	100	<30	100
	Level 5	200	<30	100
	Level 6	300	<30	400

Number of Test Vehicles Required				
Manufactured		Rework		
Mfg. SnPb	Mfg. LF	Rwk. SnPb	Rwk. SnPb ENIG	Rwk. LF
5	5	5	1	5
Trials per Specimen		1		

Mechanical Shock Testing



Mechanical Shock Testing

- The very first components to fail were lead-free PDIP components
  - Lead cracking in the fillet area is being observed as well as some trace cracking near the corner leads. It is not possible to determine if one event happened before the other or if the events are happening simultaneously.
- All of the test vehicles passed the first 3 levels of testing which were conducted per MIL-STD-810F, Method 516.5; Modified Functional Test for Flight Equipment (Level 1), Modified Functional Test for Ground Equipment (Level 2), and Modified Crash Hazard Test for Ground Equipment (Level 3).
  - 100 shocks were conducted in the z-axis for each of the three levels, equating to conducting each of the three tests 33 times.
- It appears that the predominant failure mechanism for the BGA components was pad cratering no matter the solder alloy; lead-free or SnPb.

Mechanical Shock Testing

In general SAC305 performed as well as the SnPb for surface mount components.

	% of Components Failed During Mechanical Shock Testing			
	"Manufactured" Test Vehicles		"Rework" Test Vehicles	
	SnPb	Pb-Free	SnPb	Pb-Free
Component				
BGA-225	94	96	95	100
CLCC-20	22	30	22	30
CSP-100	32	26	42	38
PDIP-20	53	73	54	58
QFN-20	0	10	0	0
TQFP-144	70	62	68	80
TSOP-50	4	0	22	20

Mechanical Shock Testing

BOEING

	Relative Ranking (Solder Alloy / Component Finish)									
BGA-225	Sn37Pb/ Sn37Pb	SAC305/ SAC405	Sn37Pb/ SAC405	SAC305/ Sn37Pb	Rwk Flux Only/ Sn37Pb	Rwk Flux Only/ SAC405	Rwk Sn37Pb/SAC405 (SnPb Profile)	Rwk Sn37Pb/SAC405 (Pb-Free Profile)		
	1	1	2	1	1	1	2	1		
CLCC-20	Sn37Pb/ Sn37Pb	SAC305/ SAC305	Sn37Pb/ SAC305	SAC305/ Sn37Pb						
	1	2	2	2						
CSP-100	Sn37Pb/ Sn37Pb	SAC305/ SAC105	Sn37Pb/ SAC105	SAC305/ Sn37Pb	Rwk Flux Only/ Sn37Pb	Rwk Flux Only/ SAC105	Rwk Sn37Pb/SAC105 (SnPb Profile)	Rwk Sn37Pb/SAC105 (Pb-Free Profile)		
	1	1	2	1	2	1	2	2		
PDIP-20	Sn37Pb/ SnPb	SN100C/ Sn	Sn37Pb/ NiPdAu	Rwk Sn37Pb/ Sn	Rwk Sn100C/ Sn					
	1	1	1	2	2					
QFN-20	Sn37Pb/ Sn37Pb	SAC305/ Sn	Sn37Pb/ Sn	SAC305/ Sn37Pb						
	X	X	X	X						
TQFP-144	Sn37Pb/ Sn	SAC305/ Sn	Sn37Pb/ NiPdAu	SAC305/ NiPdAu	Sn37Pb/ Sn37Pb Dip	SAC305/ SAC305 Dip				
	1	1	1	1	1	2				
TSOP-50	Sn37Pb/ SnPb	Sn37Pb/ Sn	Sn37Pb/ SnBi	SAC305/ Sn	SAC305/ SnBi	SAC305/ SnPb	Rwk Sn37Pb/ SnPb	Rwk Sn37Pb/Sn (SnPb Profile)	Rwk Sn37Pb/Sn (Pb-free Profile)	Rwk SAC305/ SnBi
	X	X	X	X	X	X	2	2	2	2

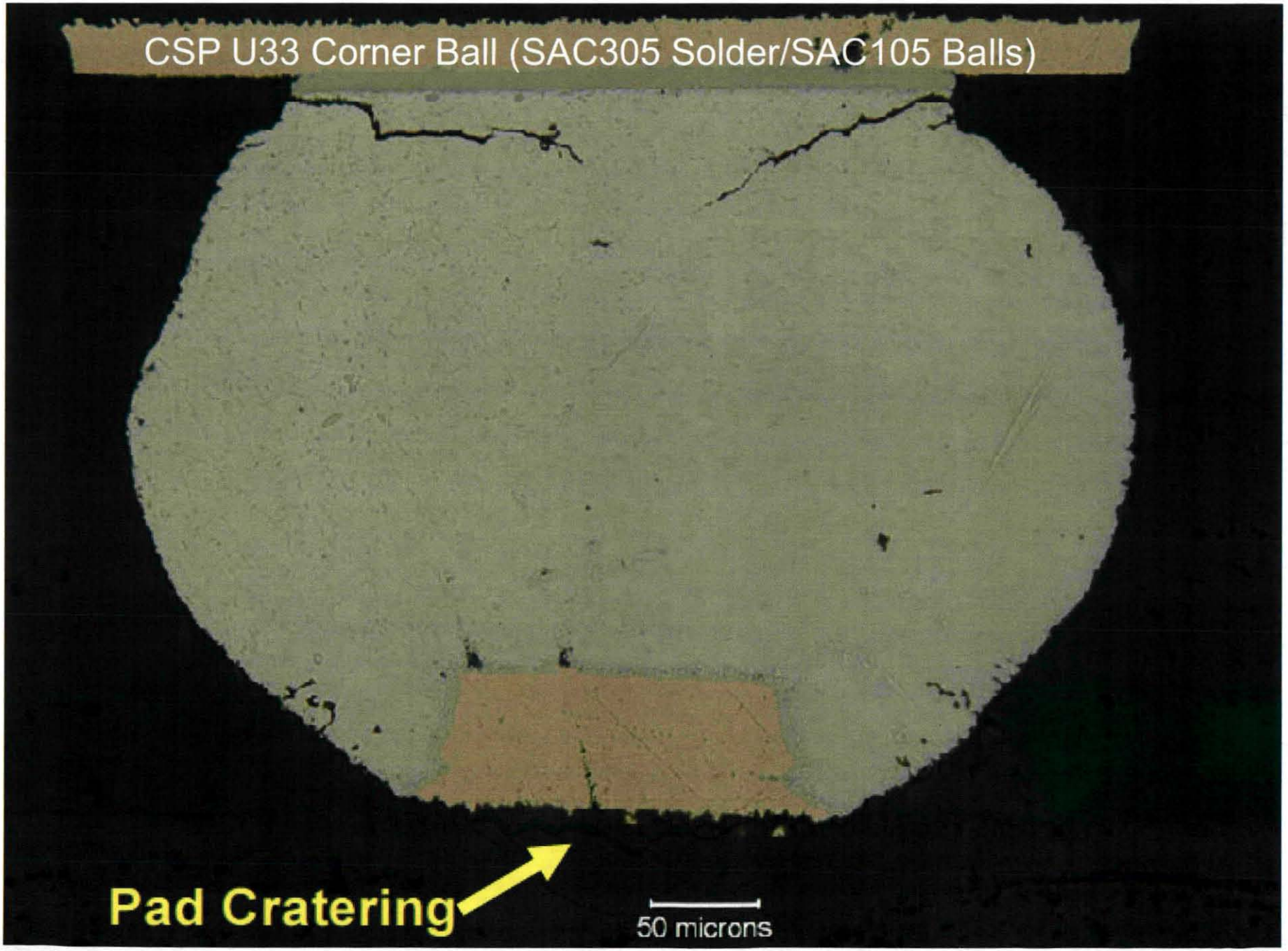
X = Not enough failures to rank

1 = as good as or better than Sn37Pb control

2 = worse than Sn37Pb control

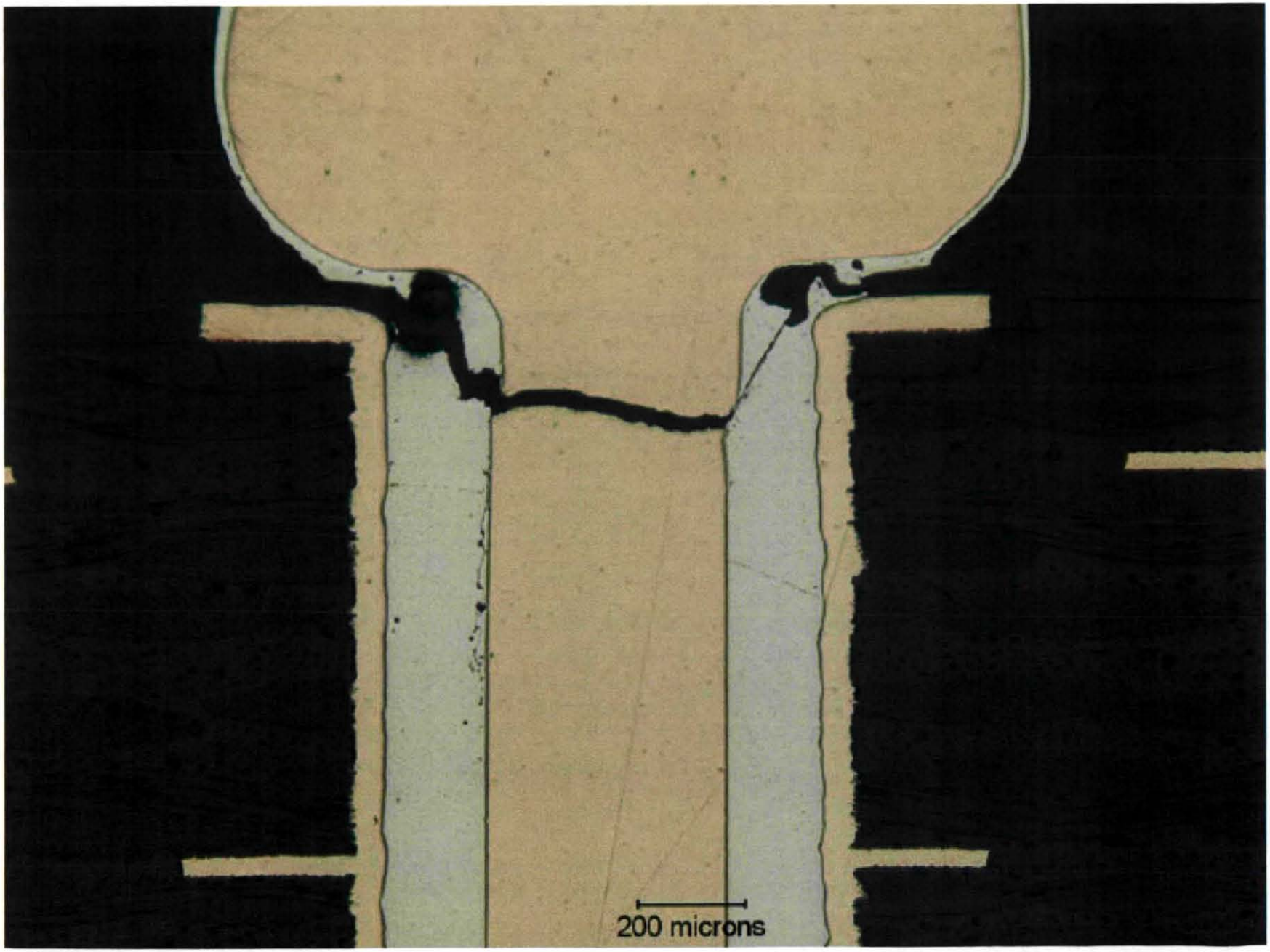
3 = much worse than Sn37Pb control

Mechanical Shock Testing



Mechanical Shock Testing

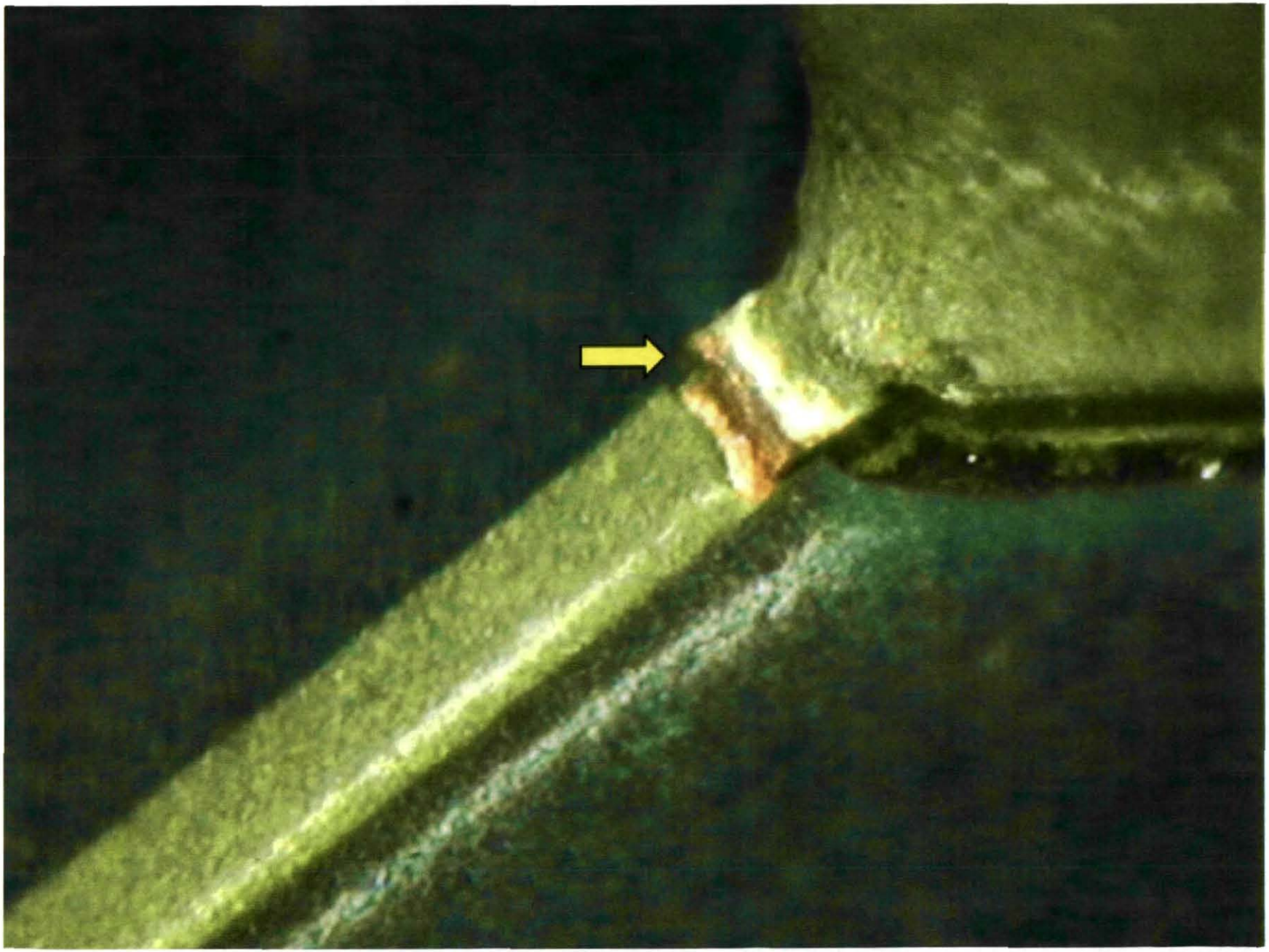
PDIP U8 Corner Lead (SN100C Solder/Sn Finish)



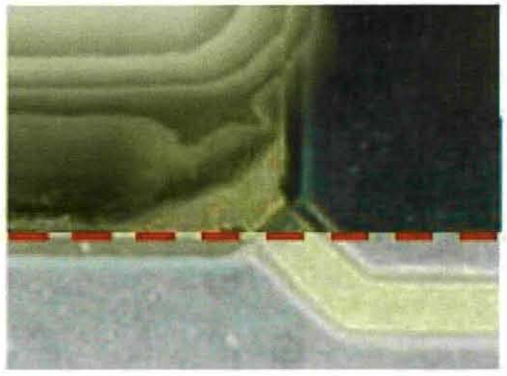
Mechanical Shock Testing

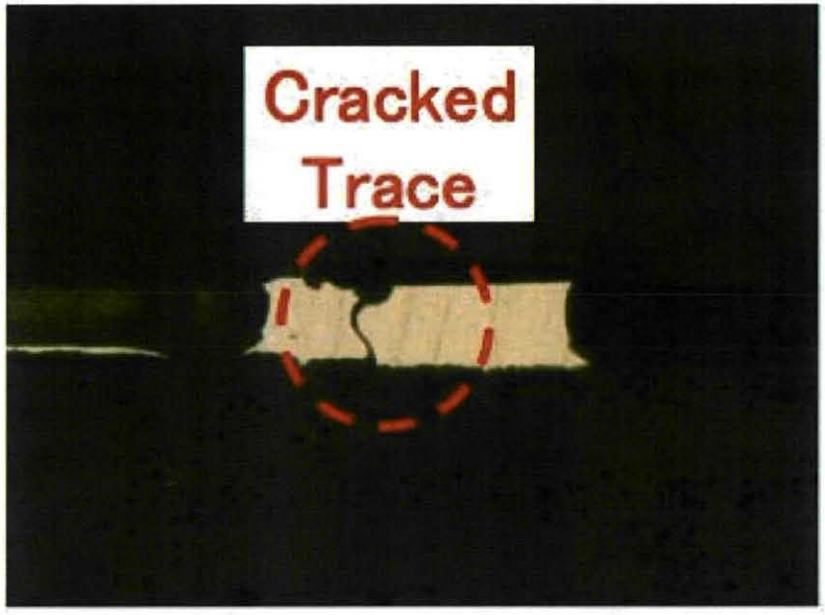
BOEING

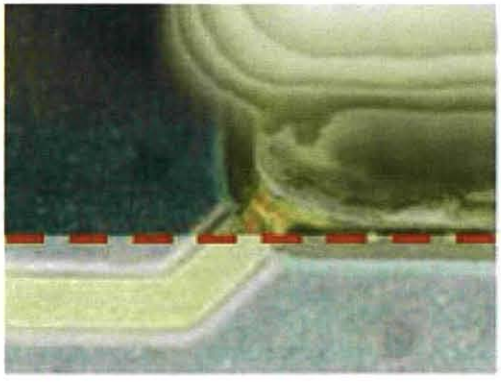
PDIP U38 Trace Crack (SN100C)

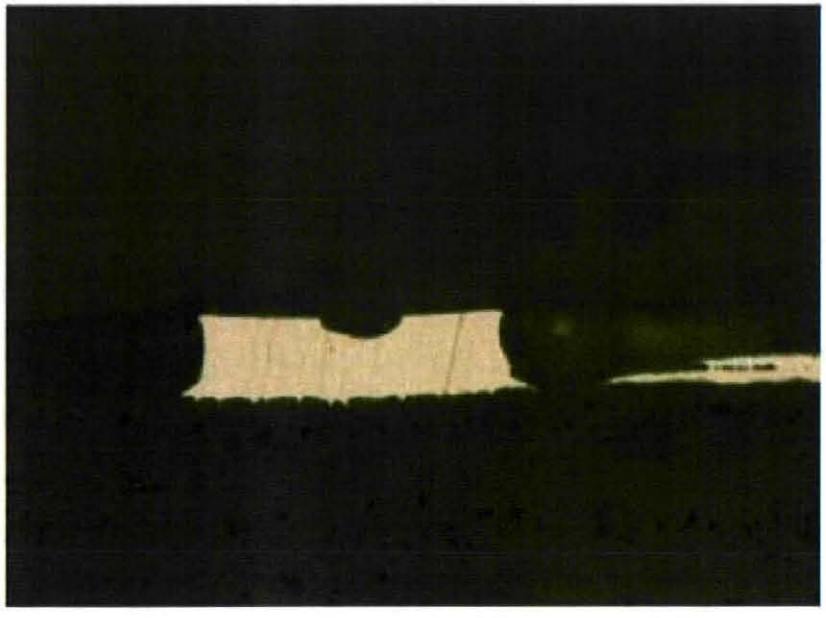


Mechanical Shock Testing





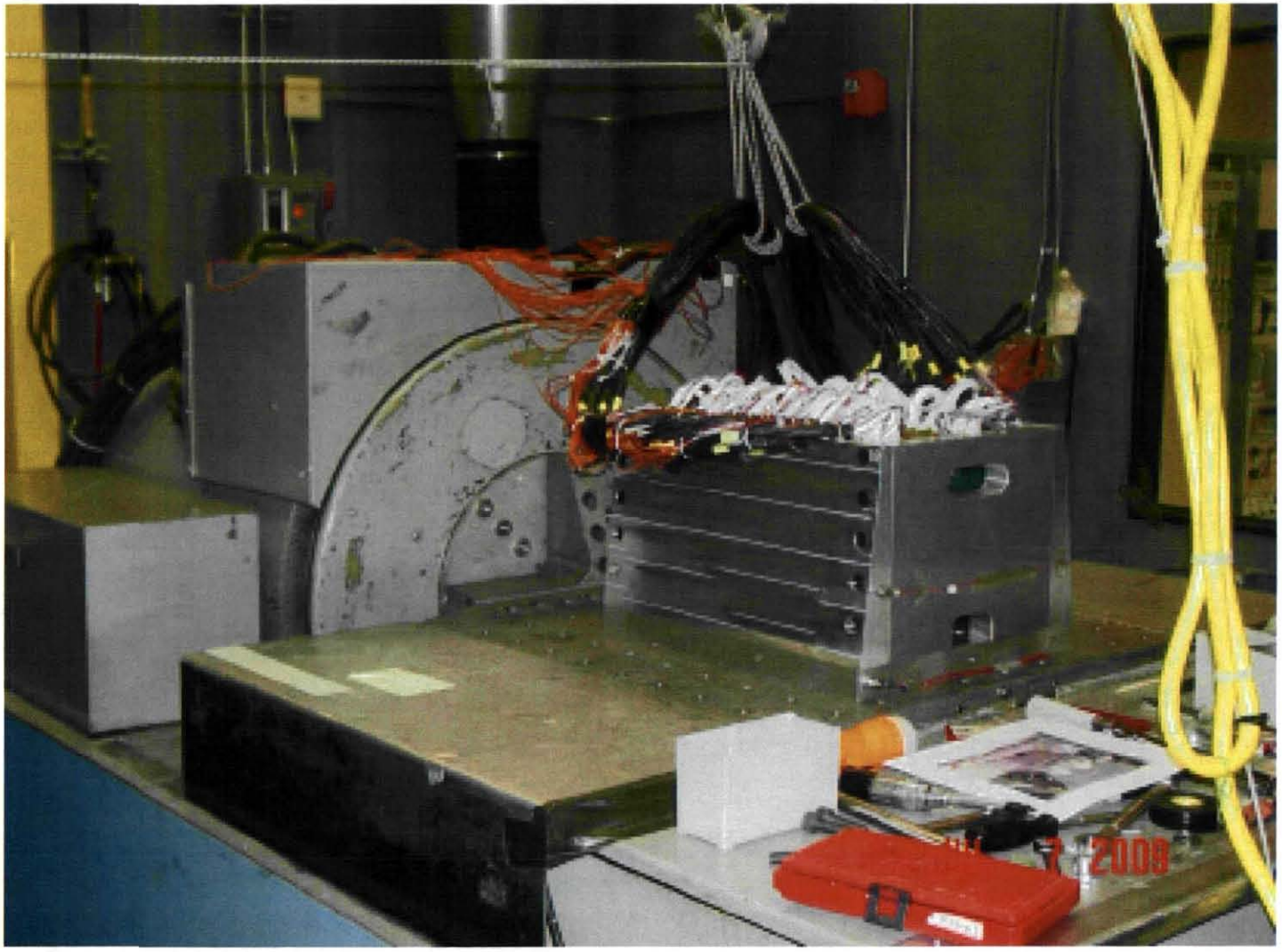




your partner for soldering solution
NIHON SUPERIOR

Vibration Testing

Subject the test vehicles to 8.0 g_{rms} for one hour. Then increase the Z-axis vibration level in 2.0 g_{rms} increments, shaking for one hour per step until the 20.0 g_{rms} level is completed. Then subject the test vehicles to a final one hour of vibration at 28.0 g_{rms}.



Vibration Testing

- Very early PDIP failures were observed.
- At an initial glance, the data does not look much different than the JCAA/JGPP test results.
- There does seem to be a big difference between solder alloys.

Vibration Testing

(Includes Mixed Solders)

	% of Components Failed During Vibration Testing				
	"Manufactured" Test Vehicles			"Rework" Test Vehicles	
	SnPb Paste	SAC305 Paste	SN100C Paste	SnPb Paste	Pb-Free Paste
Component					
BGA-225	84	98	100	100	100
CLCC-20	32	43	90	35	68
CSP-100	62	73	70	62	80
PDIP-20	98	92	100	88	96
QFN-20	0	21	20	8	10
TQFP-144	60	63	64	70	70
TSOP-50	62	73	86	77	80

Vibration Testing

	Relative Ranking (Solder Alloy / Component Finish)												
BGA-225	Sn37Pb/ Sn37Pb	SAC305/ SAC405	Sn37Pb/ SAC405	SAC305/ Sn37Pb	Rwk Flux Only/ Sn37Pb	Rwk Flux Only/ SAC405	Rwk Sn37Pb/SAC405 (SnPb Profile)	Rwk Sn37Pb/SAC405 (Pb-Free Profile)	SN100C/ SAC405				
	1	3	3	3	3	3	3	3	3				
CLCC-20	Sn37Pb/ Sn37Pb	SAC305/ SAC305	Sn37Pb/ SAC305	SAC305/ Sn37Pb	SN100C/ SAC305								
	1	3	2	3	3								
CSP-100	Sn37Pb/ Sn37Pb	SAC305/ SAC105	Sn37Pb/ SAC105	SAC305/ Sn37Pb	Rwk Flux Only/ Sn37Pb	Rwk Flux Only/ SAC105	Rwk Sn37Pb/SAC105 (SnPb Profile)	Rwk Sn37Pb/SAC105 (Pb-Free Profile)	SN100C/ SAC105				
	1	1	1	2	1	2	1	3	1				
PDIP-20	Sn37Pb/ SnPb	SN100C/ Sn	Sn37Pb/ NiPdAu	Rwk Sn37Pb/ Sn	Rwk Sn100C/ Sn	SN100C/ NiPdAu							
	1	3	2	3	3	3							
QFN-20	Sn37Pb/ Sn37Pb	SAC305/ Sn	Sn37Pb/ Sn	SAC305/ Sn37Pb	SN100C/ Sn								
	1	2	1	1	2								
QFP-144	Sn37Pb/ Sn	SAC305/ Sn	Sn37Pb/ NiPdAu	SAC305/ NiPdAu	Sn37Pb/ Sn37Pb Dip	SAC305/ SAC305 Dip	SN100C/ Sn						
	1	1	1	2	1	2	1						
TSOP-50	Sn37Pb/ SnPb	Sn37Pb/ Sn	Sn37Pb/ SnBi	SAC305/ Sn	SAC305/ SnBi	SAC305/ SnPb	Rwk Sn37Pb/ SnPb	Rwk Sn37Pb/Sn (SnPb Profile)	Rwk Sn37Pb/Sn (Pb-free Profile)	Rwk SAC305/ SnBi	SN100C/ Sn	SN100 SnBi	
	1	2*	2*	2*	2*	2	2	2*	2*	2	2	2	

*Performance relative to Sn37Pb control may depend on orientation of the TSOP

: as good as or better than Sn37Pb control

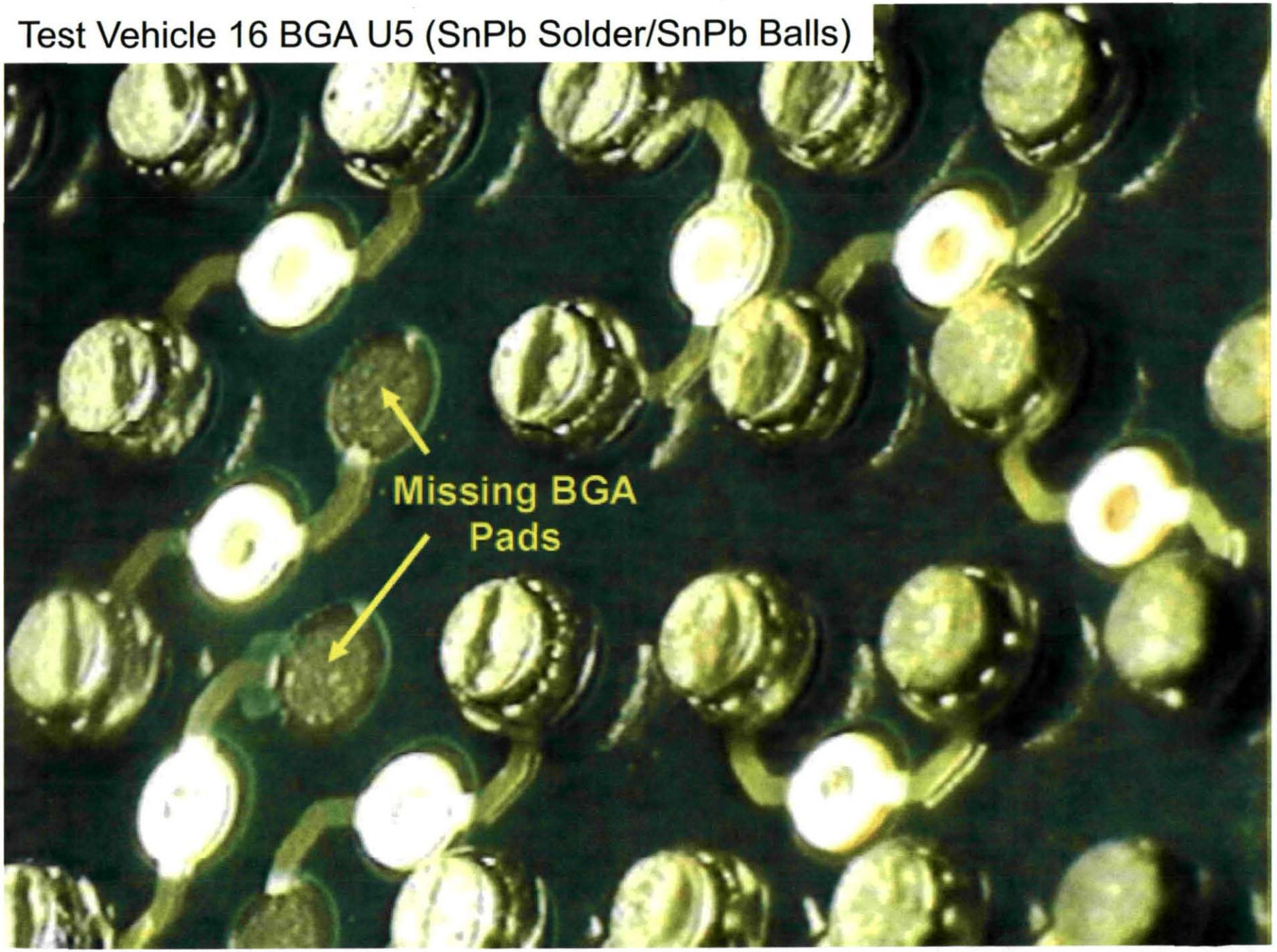
: worse than Sn37Pb control

: much worse than Sn37Pb control

Vibration Testing

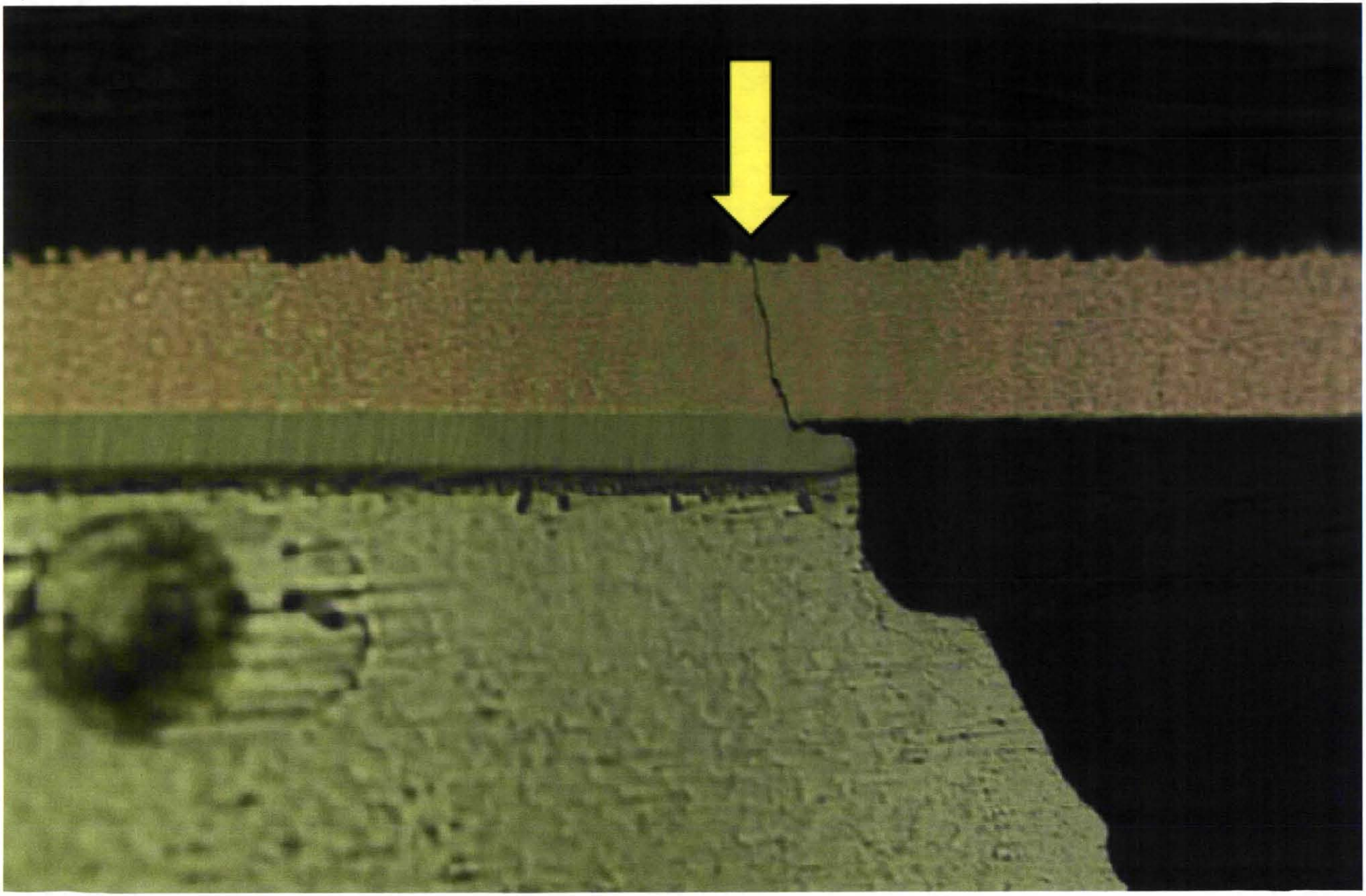
BOEING

Test Vehicle 16 BGA U5 (SnPb Solder/SnPb Balls)



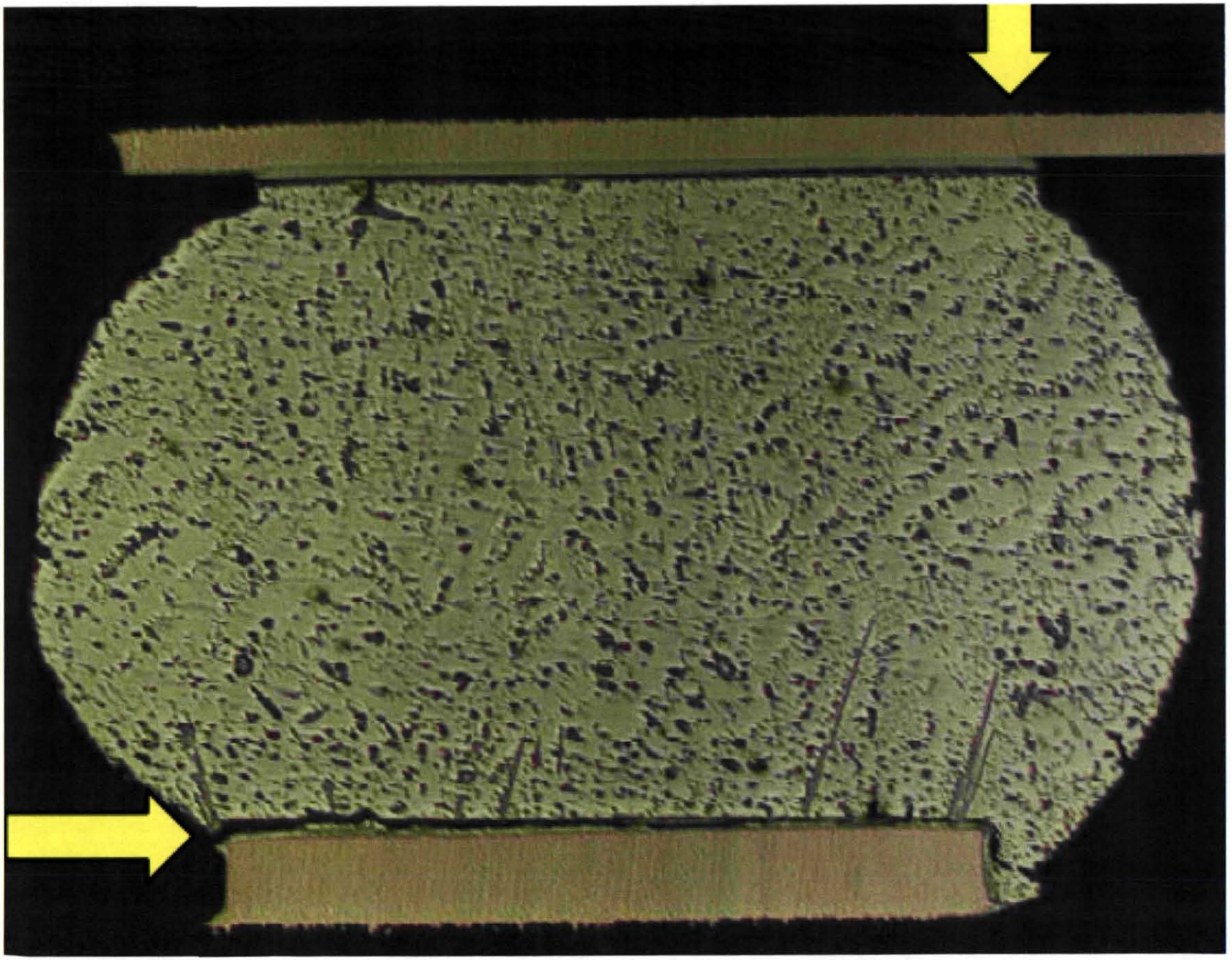
Vibration Testing

Test Vehicle 36 – Trace Crack on Component Side of BGA U21
(SAC305 Solder/SAC405 Balls)



Vibration Testing

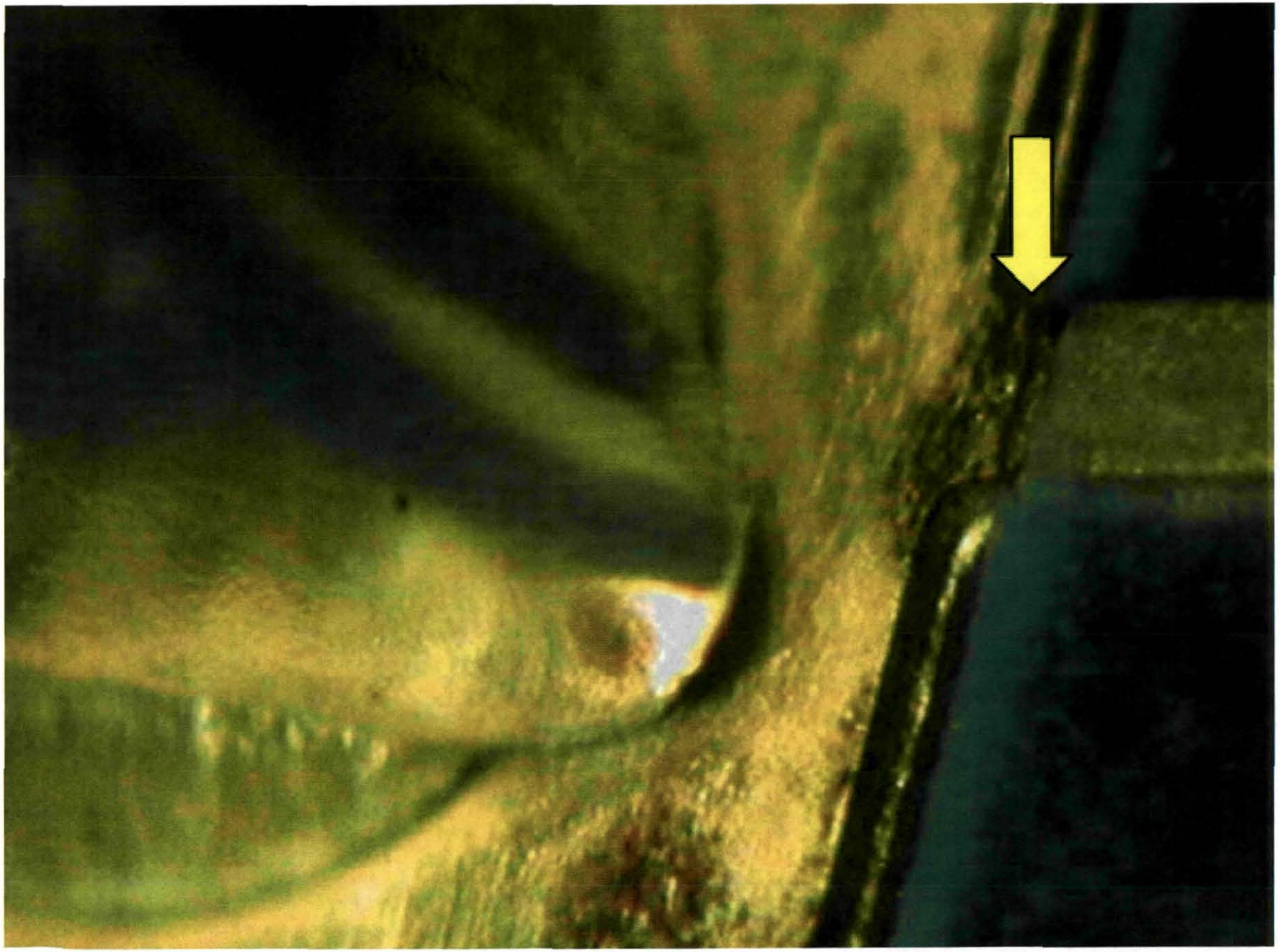
Test Vehicle 134 - Corner Ball of BGA U44 (SnPb Solder/SAC405 Balls)



Vibration Testing

BOEING

Test Vehicle 112 – Cracked Trace at Corner of PDIP U38 (SN100C/Sn)



On-Going Failure Analysis

Mechanical Shock Test Vehicles			
Failure Analysis Location	**Test Vehicle**	**Component Location**	**Selection Criteria**
Sandia	153	U43	Look for cause of open
	153	U18	Look for cause of early failure
	153	U6	Examine solder mixing
	153	U11	Look for cause of early failure with special focus on trace cracking
	153	U51	Look for cause of early failure with special focus on trace cracking
NSWC Crane	189	U11	Look for cause of early failure with special focus on trace cracking
	189	U51	See if trace cracking is absent
	190	U44	Examine solder mixing
	190	U56	Look for cause of early failure
Drop Test Vehicles			
Failure Analysis Location	**Test Vehicle**	**Component Location**	**Selection Criteria**
Celestica	144	U4	Early failure - Cycle 1
	25	U4	Early failure - Cycle 5
	27	U5	Early failure - Cycle 3
	29	U6	Early failure - Cycle 3
	26	U56	No failure - Comparison
	77	U5	Early failure - Cycle 5
	187	U4	Early failure - Cycle 2
	92	U5	Early failure - Cycle 3
	59	U6	Early failure - Cycle 3
	58	U56	No failure - Comparison
	159	U4	Early failure - Cycle 2
	159	U44	Early failure - Cycle 2
	159	U6	Early failure - Cycle 2
	159	U56	Early failure - Cycle 4

Upcoming Event

SMTAI 2010

- October 24 - 28, 2010
- Orlando, FL - Walt Disney World Swan and Dolphin Resort

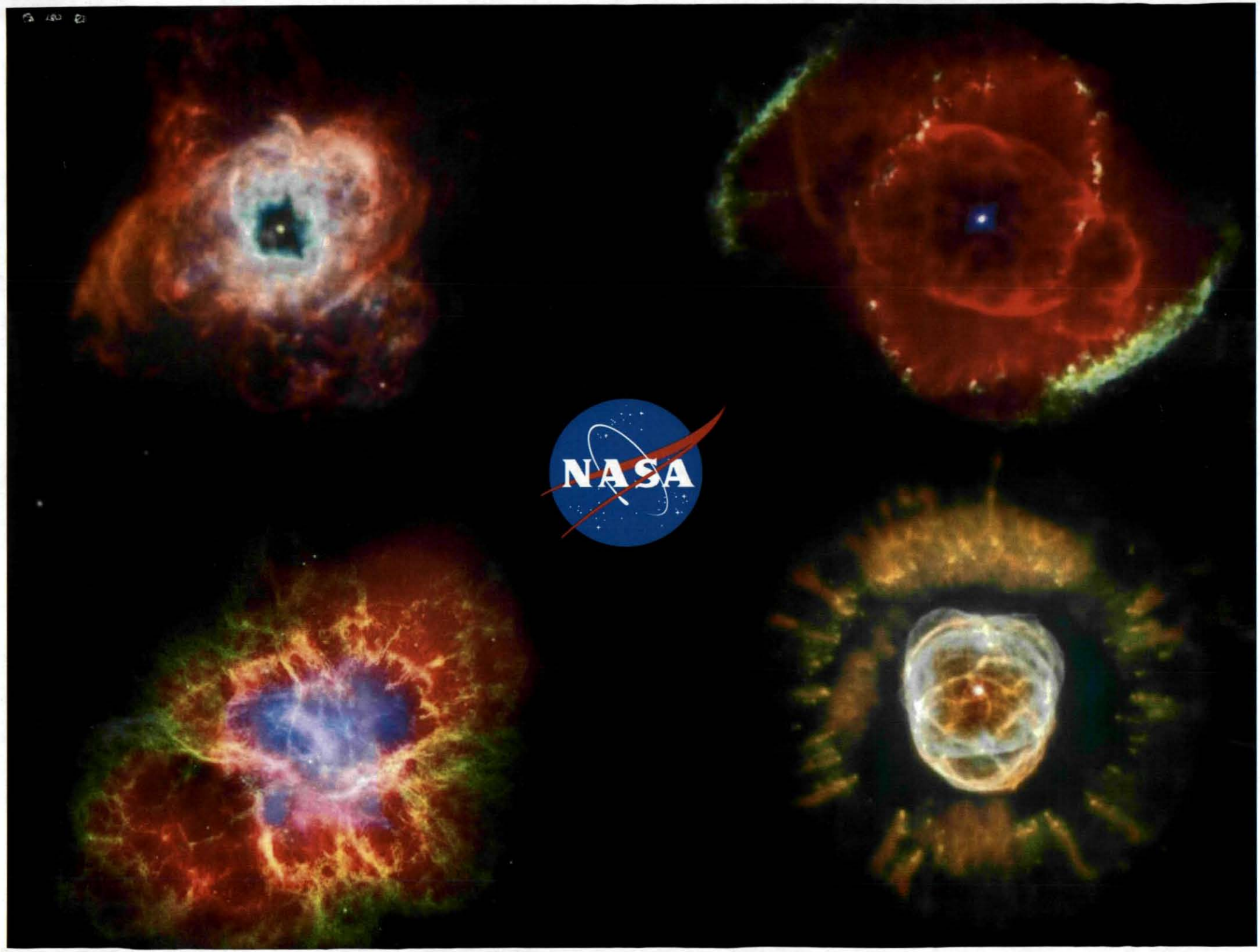
NASA-DoD Presentations - October 28

- NASA-DoD Lead-Free Electronics Project – Update
- Drop Test Assessment of a Medium Complexity Assembly for High Reliability Applications
- NASA/DoD Lead-Free Electronics Project: Mechanical Shock Testing
- NASA-DoD Combined Environments Testing Results
- NASA/DoD Lead-Free Electronics Project: Vibration Testing
- NASA DoD -55°C to +125°C Thermal Cycle Test Results

Kurt Kessel
ITB, Inc.
NASA Technology Evaluation for Environmental Risk Mitigation Principal Center (TEERM)
Kennedy Space Center, FL
Phone: 321-867-8480
E-Mail: kurt.r.kessel@nasa.gov
Website: www.teerm.nasa.gov

NASA-DoD Lead-Free Electronics Project:
http://www.teerm.nasa.gov/projects/NASA_DODLeadFreeElectronics_Proj2.html

JCAA/JGPP Lead-Free Solder Project
http://www.teerm.nasa.gov/projects/LeadFreeSolderTestingForHighReliability_Proj1.html


NASA