

RADIO-FREQUENCY INTERFERENCE (RFI) MITIGATION FOR THE SOIL MOISTURE ACTIVE/PASSIVE (SMAP) RADIOMETER

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ABSTRACT

The presence of anthropogenic RFI is expected to adversely impact soil moisture measurement by NASA's Soil Moisture Active Passive mission. The digital signal processing approach and preliminary design for detecting and mitigating this RFI is presented in this paper. This approach is largely based upon the work of Johnson [1] and Ruf [2].

Index Terms— SMAP, Soil Moisture Active Passive, Digital Radiometer, Filterbank, Kurtosis

1. INTRODUCTION

Radio-frequency interference (RFI) has detrimentally affected soil moisture remote sensing data since 1978 when it was first observed at 6.6 GHz with SMMR on SeaSat [3]. Over the last several years it has started to seriously impact remote sensing science products and is expected to continue. This is primarily because the frequency requirements of remote sensing have begun to overlap active radio service allocations. Until recently, soil moisture was being sensed in the C-band, for which there is no passive service allocation. The launch of the European Space Agency's Soil Moisture Ocean Salinity (SMOS) mission [4] begins a new era of L-band remote sensing from space, which has been long desired for remote sensing of soil moisture through vegetation. The L-band record from space will be continued with NASA's Aquarius [5] and SMAP [6] missions.

Although there is a primary exclusive allocation to passive use in the L-band, it is still highly susceptible to RFI because of the proliferation of the active services in bordering frequency allocations. Thus, RFI detection and mitigation strategies are needed so SMAP can meet its requirements.

The chosen approach for SMAP is to use a digital processing backend in lieu of microwave power detectors. Johnson produced the first RFI-mitigating digital radiometer [1] and Ruf, et al., introduced the kurtosis statistic as an RFI detector and classifier [2]. Using their previous research plus work

done for the Hydros mission [7] as its basis, the SMAP digital backend will provide both time and frequency diversity data at each footprint to enable the ground processing algorithms to detect and remove RFI. To do so, it will use digital signal processing (DSP) techniques to measure 1200 samples in time and frequency for each SMAP footprint. This paper summarizes the DSP algorithms and electronics implementation using field-programmable gate arrays (FPGAs) in the SMAP preliminary design.

2. SMAP HARDWARE IMPLEMENTATION

2.1. Radiometer Front End (RFE) Analog Subsystem

The SMAP mission uses a single feed polarimetric radiometer that operates in the protected L-band radio frequency range from 1400 to 1427 MHz. The received radiometer signal, $x(t)$, is branched into horizontal and vertical polarizations, denoted by $E_H(t)$ and $E_V(t)$, respectively. In each branch, the polarized signals are bandlimited, amplified, and down-converted to a 120 MHz intermediate frequency (IF). The Radiometer Digital Electronics (RDE) subsystem digitizes $E_H(t)$ and $E_V(t)$, forming digital signals $E_H(n)$ and $E_V(n)$ respectively. At the core of the RDE is a FPGA-based DSP system that computes time-frequency diversity data used for subsequent ground processing, removal of RFI, and geophysical parameter retrieval.

2.2. Digital Signal Processing Approach

SMAP will be the first spaceborne mission to use on-board DSP for RFI mitigation using state-of-the-art algorithms developed by Ruf [1] and Johnson [2]. In prior spaceborne radiometers, the IF signal power is measured by an analog square-law detector followed by a lowpass filter. The resulting power measurement is digitized and transmitted to the ground. The SMAP radiometer digitizes the IF signal directly and uses DSP to compute IF signal power, as well as additional data products useful for RFI time-frequency localization and statistical detection using kurtosis.

The SMAP DSP computes the first four raw sample moments of the fullband signals, $E_H(n)$ and $E_V(n)$. In addition, the fullband signal is split into 16 adjacent and overlapping subband signals $e_H^{[k]}(n)$ and $e_V^{[k]}(n)$. The first four raw sample moments are computed by the DSP for each subband signal as well. Finally, the cross-correlation of the fullband and subband signals are computed. The integration times used for each fullband and subband data product are programmable, but are initialized to a minimum of 280 and 1120 μ s, respectively. All of these statistics are transmitted to the ground and are used as inputs to the RFI detection algorithm. The system functional block diagram is shown in Figure 1.

2.3. Radiometer Digital Electronics Subsystem

The SMAP RDE consists of three processor boards. The first two identical boards are called Analog Processing Units (APU)s. These boards, named APU-H and APU-V, digitize the input signals with 14 bits at a sample rate of 96 MHz. The third processor board is called the Digital Processing Unit (DPU). The DPU collects and prepares data products from each APU card for ground transmission. The DPU also computes cross correlation between horizontal and vertical polarized fullband and subband signals.

2.4. FPGA-based DSP

On-board radiometer DSP is performed using a total of seven antifuse-based Actel RTAX2000 FPGAs - three on each APU board and one on the DPU board. If SRAM-based FPGAs with significantly more logic gates are used, the total number of FPGAs can be reduced to about 1 or 2 devices. However, factors such as flight qualification, radiation hardness and flight heritage deemed these kinds of FPGAs too risky for spaceborne application.

Actel RTAX4000 FPGAs, which have about twice the number of logic gates as the RTAX2000, offered a radiation hardened solution, but the risk of using these parts was also determined to be unacceptably high. This is because they had no prior flight heritage; had no easy and low-cost prototyping solution; and were too early in the flight qualification stage to be considered viable.

With the constraint of using Actel RTAX2000 devices to do the signal processing, several algorithm optimizations were employed that allowed for a logic-area efficient implementation of the RFI mitigation algorithm.

A number of DSP techniques [8, 9, 10] commonly found in digital communication receivers and radar are applied to the radiometer DSP algorithm to minimize FPGA logic area. Algorithms amenable to FPGA multiplier sharing and signal sample interleaving were deliberately sought out and are used

extensively throughout the entire processing chain to minimize FPGA logic.

3. PROCESSING SUBSYSTEMS

The DSP is divided into five modules: Signal Pre-Processor (SPP), Digital Down Converter (DDC), Polyphase Filter Bank (PFB), Statistics Calculation Unit (SCU) and Cross Correlator (XCORR). Each module discussed in the following sub-sections. In the following discussion, denote the fullband signal (from APU-H or APU-V) by $E(n)$ and the subband signal by $e^{[k]}(n)$. Subscripts H and V are used only when making a distinction between the polarized signals.

3.1. Precision and numeric representation

All FPGA computations are preformed using signed, 2's-complement fixed-point arithmetic. Full-precision fixed point is maintained in each processing module, but the word length is limited to 20 bits between modules. A finite-precision rounding system similar to block floating point is employed throughout the DSP, where a variable-start, contiguous range of 20 bits is selected from the full precision bus with the aid of in-orbit programmable starting pointers. Due to limited transmit bandwidth to the ground, each data product generated by the RDE is restricted to 12 bits.

3.2. Signal Preprocessor

It is desirable to have robust diagnostic capabilities for the RDE once in orbit. Two diagnostic capabilities in the DSP are managed by the SPP. First, the SPP allows the user to bypass the radiometer signal and inject test signals instead. The SPP also permits the user to add a programmable DC-offset value to the input signal to compensate for DC bias. A third diagnostic feature of the RDE bypasses processing all together, allowing short time records of $E(n)$ to be saved directly and transmitted to the ground for analysis.

3.3. Digital Downconverter

The RDE receives a 24 MHz bandlimited analog signal centered at 120 MHz IF. The signal is subsampled at 96 MHz, allowing the alias in first Nyquist zone to be digitized. The DDC downconverts $E(n)$, reducing its sample rate to 24 MHz. The mixer stage, image rejection filter, and down-sampler are all combined into an efficient periodically time-varying (PTV) [11] multirate FIR filter using an approach similar to Ellingson [12]. This architecture minimizes FPGA logic utilization by reducing the number of required multipliers from 130 to 16. The output of the DDC is referred to as the fullband signal denoted by $\tilde{E}(n)$.

Although the RFE aggressively bandlimits the L-band signal to 24 MHz using two 8-pole filters, it is important to have

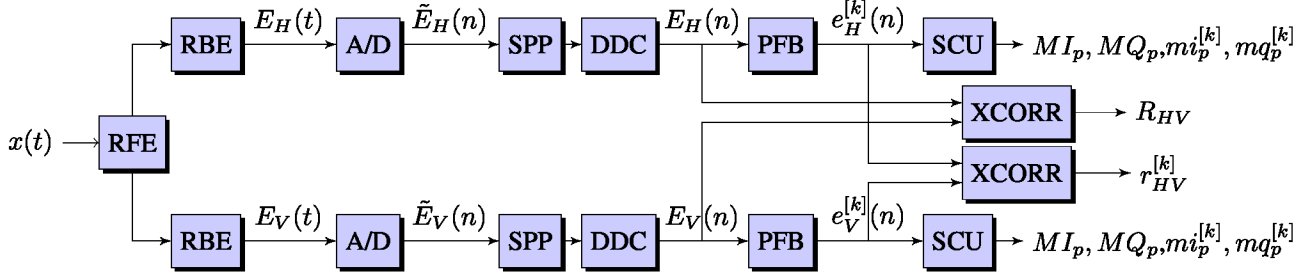


Fig. 1. SMAP-RDE signal processing flow. Output data consists of fullband and subband moments for each polarization and each I/Q component, as well as fullband and subband cross correlation.

high quality image rejection in the DDC. The image rejection filter for the DDC is a 64-tap 12-bit coefficient FIR low-pass filter based on a Blackman window with -3dB point at 12MHz. This filter suppresses the mixer image and out-of-band interference down to -60dB.

3.4. Critically-Sampled Polyphase Filter Bank

The PFB splits $\tilde{E}(n)$ into 16 uniformly spaced, equal-bandwidth subband signals $e^{[k]}(n)$, $k = 0, \dots, 15$. The filter bank requirements are listed in Table 1, leading to the response in Figure 2. The PFB design requirements are met

Table 1. SMAP Filter Bank Specifications

Channels	16
Total bandwidth	24MHz
Bandwidth/channel	1.5 MHz
k to $k + 2^{th}$ stopband attenuation	32 dB

with a prototype 64th-order unity gain FIR filter based on a Kaiser window with $\beta = 4$ and -2.8dB overlap point of 750 kHz. The coefficients are quantized to 12-bits to achieve about 60 dB stopband attenuation.

The filter bank is comprised of two units. The first is a PTV FIR filter that cycles through the coefficients of each polyphase sub-filter. The second is a standard 16-point, pipelined FFT. Compared with a uniform filterbank and a parallel-branch implementation of a polyphase filter bank [9], this filter bank architecture minimizes FPGA logic.

Much like the DDC, the desired side effect of this architecture is the interleaving of subband signals. Every block of 16 serialized samples represents a time sample from each of the 16 subbands. The output of the filter bank is denoted as $e^{[k]}(n) = i^{[k]}(n) + jq^{[k]}(n)$, $k = 0, \dots, 15$.

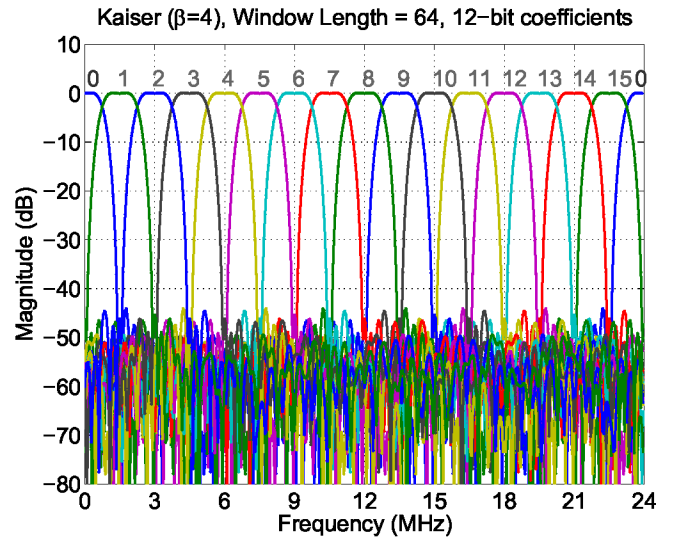


Fig. 2. Frequency response of polyphase filter bank

3.5. Statistics Calculation Unit

The role of the SCU is to compute the first four raw sample moments of $E(n)$ and $e^{[k]}(n)$. The r^{th} moment, $m_r^{[k]}$, $r = 1, \dots, 4$ for the in-phase and quadrature component signals for each subband are computed in Equation 1,

$$m_r^{[k]} = \alpha_{r,k} \sum_{n=0}^{T_2-1} \left(i^{[k]}(n) \right)^r \quad (1)$$

where α accounts for scaling the full-precision moment computations down to fit within a 12-bit bus subset. Similarly, the moments M_r of the $E(n)$ are computed using an equation of the same form as above by dropping the superscript $[k]$ and using capital notation.

3.6. Cross Correlator

The last DSP module in the SMAP-RDE signal processing chain is the cross-correlator. Cross-correlation necessarily

takes place on the DPU board. The subband cross correlation between $e_H^{[k]}(n)$ and $e_V^{[k]}(n)$ is given by,

$$\begin{aligned} r_{HV}^{[k]} &= \left\langle e_H^{[k]}(n) \left(e_V^{[k]}(n) \right)^* \right\rangle \\ &= \gamma \sum_{n=0}^{N-1} \left(i_H^{[k]}(n) i_V^{[k]}(n) + q_H^{[k]}(n) q_V^{[k]}(n) \right) \\ &\quad + j\gamma \sum_{n=0}^{N-1} \left(i_V^{[k]}(n) q_H^{[k]}(n) - i_H^{[k]}(n) q_V^{[k]}(n) \right), \quad (2) \end{aligned}$$

where $k = 0, \dots, 15$, and γ represents a scaling factor introduced by selecting a 12-bit subset of the full precision fixed point result. The complex cross-correlation of the fullband signals $\tilde{E}_H(n)$ and $\tilde{E}_V(n)$ are computed with an expression similar to Equation 2 by dropping the superscript $[k]$ and using upper-case notation for the signals.

4. GROUND ALGORITHMS

Using the detailed information provided by the SMAP instrument, the ground processing algorithms will detect RFI in the raw data, remove it, and output calibrated nearly RFI-free brightness temperature estimates. The diversity of the SMAP data product allows several different detectors to be utilized. A time domain pulse detector can be used on the full band product for removing radar interference. A cross-frequency detector can be used to remove persistent narrow band sources. It is envisioned the kurtosis products will aid in classifying RFI, if not in detecting less-well-behaved sources. A maximum likelihood decision process will be used to combine the detector outputs and produce a single estimate of antenna temperature with RFI removed.

5. SUMMARY

The development of the SMAP RFI-mitigating radiometer is based on the ground work of Johnson and Ruf. Application of fundamental DSP tools, novel algorithm simplifications and FPGA architecture tricks make this digital radiometer possible for space implementation. The preliminary design prototype is being tested currently using an Altera Stratix III DSP kit in preparation for a preliminary design review in September 2010. The spaceflight engineering test unit, currently being designed, is scheduled for delivery in 2011.

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