

Next-generation A/D Sampler ADS3000+ for VLBI2010

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Abstract

A high-speed A/D sampler, called ADS3000+, has been developed in 2008, which can sample one analog signal up to 4 Gbps to versatile Linux PC. After A/D conversion, the ADS3000+ can perform digital signal processing such as real-time DBBC (Digital Base Band Conversion) and FIR filtering such as simple CW RFI filtering using the installed FPGAs. A 4 Gbps fringe test with the ADS3000+ has been successfully performed. The ADS3000+ will not exclusively be used for VLBI but will also be employed in other applications.

1. Introduction

The National Institute of Information and Communications Technology (NICT) has been developing VLBI observation systems and data processing systems since the 1970s. The K5 VLBI system is designed with the commodity products such as personal computers, hard disks, and network components. This strategy has been quite successful for developing highly flexible and high-performance observation systems and data processing systems for VLBI. K5/VSI series are realized by high-speed AD sampler units and a commodity Linux PC system to record data according to the VSI-H (VLBI Standard Interface - Hardware) specifications. VSI-H was proposed to define a standard interface for the high-speed data transfer between data input modules, data transfer modules, and data output modules to improve the compatibility between next generation VLBI observing systems and the correlator systems. Three high-speed AD sampler units, ADS1000, ADS2000, and ADS3000, have been developed to date to support various sampling modes. ADS1000 can sample one baseband channel at a sampling rate of 1024 Msps/2bit. ADS2000 can sample 16 baseband channels at the sampling rate of 64 Msps suitable for geodetic VLBI observations with the bandwidth synthesis method. ADS3000 can sample a wide range of the baseband frequency band up to 1024 MHz with a sampling rate of 2048 Msps [2]. Currently, ADS3000+ is under development to support 4 Gbps x 1 ch, 2 Gbps x 2 ch, and 1 Gbps x 4 ch sampling modes by using a faster AD sampler chip [1]. ADS3000 and ADS3000+ are equipped with FPGA chips to realize digital baseband converter (DBBC) with user-selectable bandwidth of 4–32 MHz. We will present more details about the newly designed ADS3000+ system in this article.

2. The Next-generation A/D Sampler ADS3000+

The ADS3000+¹ is a newly-extended A/D sampler from the ADS3000 system that supports various sampling modes. A faster A/D sampler chip and two new FPGA chips replace a simple

¹More information is available in <http://www2.nict.go.jp/w/w114/stsi/K5/>



Figure 1. Front view of the ADS3000+ unit. Many status settings can be displayed and monitored.

Size	EIA 2U (480mm x 88mm x 430mm)
Reference	10MHz 0dBm+-3dBm, 1PPS (50ohm)
IF input	+/-250m Vp-p (50ohm)
Output	VSI-H compliance
Control	RS232-C (D-sub 9pin male),100Base-Tx
Power supply	AC100-240V
A/D chip	e2V EV8AQ160
FPGA chip 1	Xilinx Virtex5 XC5VLX110
FPGA chip 2	Xilinx Virtex5 XC5VLX220
Sampling Modes	4096 Msps x 1 ch 2048 Msps x 2 ch 1024 Msps x 4 ch (DBBC mode)

Figure 2. Specifications of the ADS3000+ unit. The FPGA chip can be replaced by a larger one (e.g., XC5VLX330).

FPGA chip. It has the capability of sampling analog data up to 5 GHz at the highest speed. However, one VSI-H (VLBI Standard Interface) interface is connected to a PC up to 2 Gbps (Giga bit per second). The maximum sampling speed via two VSI-H connections becomes 4 Gbps. ADS3000+ has four VSI-H output ports, so 8 Gbps recording is possible, if a PC is connected to every port.

The ADS3000+ digitizes analog signal 4 Gsps x 1 ch, 2 Gsps x 2 ch, and 1 Gsps x 4 ch. Moreover, various signal processing steps such as DBBC (Digital Base-Band Converter) can be performed with the FPGA chips inside the ADS3000+. Figure 2 shows the major specifications of the ADS3000+ system. Standard sampling modes up to 4 GHz have already been evaluated [3].

3. First Fringe Detection at 4 Gsps

Before doing a 4 Gsps fringe experiment, the VSI-H limitation (connection between ADS3000+ and PC) has to be considered. The VSI-H data rate at one channel is 2 Gbps at maximum, so that a 4Gsps@1bit experiment is not possible with one port output. A workaround of simulating two VSI-H ports has been applied to ADS3000+. Specifically, the digitized data is sequentially divided into one-byte or four-byte samples and allocated to the two VSI-H outputs. The two digital data streams are assembled by a software program to obtain 4 Gsps data. It is an adaptation of a high-performance look-up-table method.

A fringe test was carried out on 27 April 2009. The Kashima 34m antenna and 11m antenna were used with ADS3000+ units at the two stations. The phase calibration signal was shut off to detect fringes correctly. After sampling at 4 Gsps speed with 1bit quantization, the whole bandwidth spectrum of X-band is fully shown in Figure 3. A first fringe of 3C273B at 4 Gsps could be successfully detected after correlation. This is shown in Figure 4. A signal-to-noise-ratio (SNR) of the 3C273B fringe is estimated to be about 8.6 at 8 ms integration. The speed of the 4 Gsps fringe is a world record [3].

4. Real-time FIR Filtering, RFF Mode

With FPGA, a real-time FIR filtering signal process, called RFF mode, can be realized with 2 Gsps x 2 ch at maximum. We adapted the RFF mode to the radio signal environment of Kashima

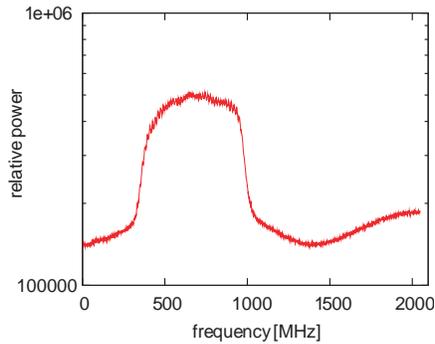


Figure 3. X-band spectrum of Kashima 11m antenna. The bandwidth is 500 MHz; however, the 4 Gbps mode detects up to Nyquist-rate 2 GHz. The whole X-band bandwidth spectrum can be obtained at one time.

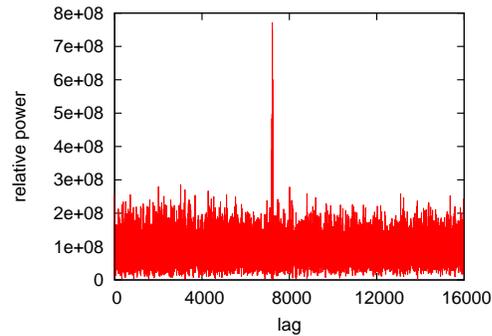


Figure 4. First fringe of 3C273B at 4 Gbps speed with ADS3000+ in 8 ms integration time between Kashima 34m and 11m antennas on 27 April 2009. The 4 Gbps fringe is a world speed record.

Space Research Center. This is shown in Figure 5. In this case, we designed a band elimination filter (BEF) for suppressing strong signals. In RFF mode, the filter coefficient is limited to 65taps 8bit range. However, any filter can be designed for these conditions. The RFF is also used for VLBI purposes. For example, a real-time Hilbert transform can be used, which makes 90 degree shift like 90 degree hybrid. One channel of RFF is Hilbert-transformed, and another channel is used for delay synchronization. We plan to use this RFF mode to convert linear polarization to circular polarization.

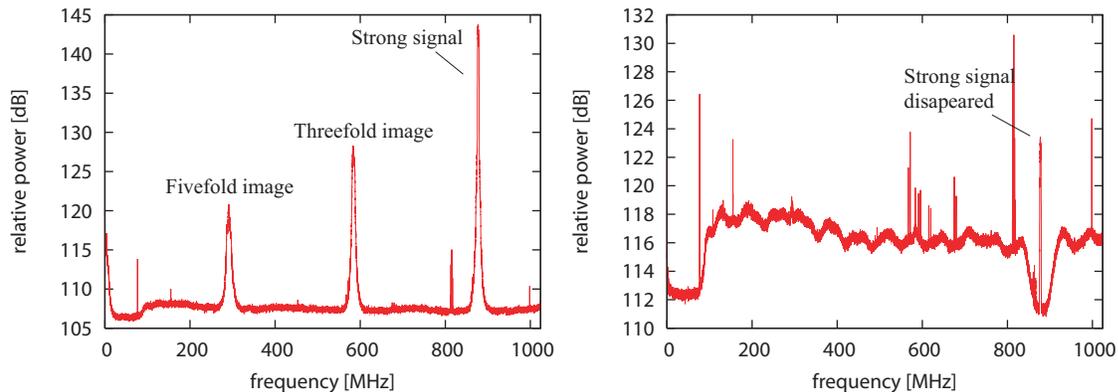


Figure 5. (left) With an omni-directional antenna and a wide-band receiver of 100–1024 MHz, the radio conditions around Kashima Space Research Center were determined. At 880 MHz, a strong radio signal from the base station can be seen. The base station signal is too strong to obtain a proper dynamic range. (right) With BEF, the strong base station signal weakens, and it is possible to measure other radio signals with an improved dynamic range.

5. DBBC on the ADS3000+

Digital sampling DSP with ADS3000+ is realized via DBBCs. There are 16-ch DBBCs inside ADS3000+. The DBBC specifications are shown in Table 1. The output formats of 16-ch DBBCs at 2 bit or 8-ch DBBCs at 4 bit can be selected. Figure 6 shows a DBBC flow chart. First digital data comes from A/D, and it is multiplied by NCO (numerical controlled oscillator), which makes it possible to tune the frequency by 1Hz resolution and angular acceleration. After frequency shift, filtered CIC and FIR follow. CIC (Cascade Integrator Comb) is not only a small circuit but also a useful LPF. Finally, complex or real (USB or LSB) signal is generated. A delay between 16-ch DBBCs is calibrated to zero in all modes. The user does not need to care about delay inside DBBCs. Following the final check of the DBBC, we will perform a fringe test between analog BBC and DBBC systems. The bandwidth of the analog BBC has a slope characteristic due to image rejection mixer. It will be more meaningful to compare analog-analog BBC and DBBC-DBBC.

Table 1. Specifications of the ADS3000+ DBBC mode. One VSI-H of DBBC generates 16 ch x 2 bit or 8 ch x 4 bit. The VSI clock speed can be fixed or variable. So far, only 1024 Msps x 4 ch is supported in DBBC mode.

Sample speed	Quantization	VSI clock
8 Msps	4 bit	Fixed: 64 MHz, Variable 8 MHz
16 Msps	4 bit	Fixed: 64 MHz, Variable 16 MHz
32 Msps	4 bit	Fixed: 64 MHz, Variable 32 MHz
64 Msps	4 bit	Fixed: 64 MHz, Variable 64 MHz
1024 Msps	1 bit, 2 bit	Fixed: 64 MHz

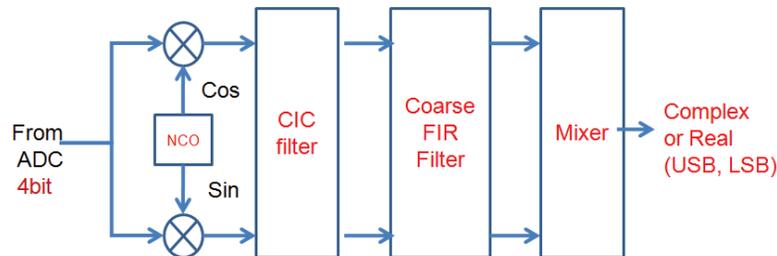


Figure 6. ADS3000+ DBBC flowchart. The DBBC follows a modified Weaver method which is multiplied by NCO and filtered out. To suit the FPGA capacity, a CIC filter (Cascade Integrator Comb) is applied. There are 16 DBBCs in ADS3000+. Each DBBC can generate Complex or Real (USB or LSB) with 4, 8, 16, or 32 MHz bandwidth.

6. Discussion

The National Astronomical Observatory of Japan (NAOJ) currently checks the connection between ADS3000+ and Mark 5B recording system. The compliance of ADS3000+ with VSI-H

output is kept; hence, a good result is expected. Currently ADS3000+ has a VSI-H output interface which connects PC with 2-Gbps speed at maximum. Four VSI-H output ports on ADS3000+ yield an 8-Gbps speed. However, to divide data inside ADS3000+ and to assemble data after recording to PC could be useless. By A/D chip specification of ADS3000+, it is possible to convert to digital signal up to 5 Gsps and 8bit quantization. Total 40 Gsps data is impossible to record via VSI-H and 10GbE interfaces. Currently 40GbE, 100GbE, and USB3.0 is more familiar. When considering 40GbE and 100GbE for the future equipment, it will be necessary to further develop not only the recorder system but also the e-VLBI network transfer. USB3.0, on the other hand, tends toward greater use at 5 Gbps. In case of using USB3.0, it is more convenient and cheaper. USB3.0 has the potential to create K5/VSI3.0 system with ADS3000+.

7. Summary and Outlook

We were able to obtain the speed record for 4 Gsps fringe in 2009. ADS3000+ will not only be a powerful converter for the current receiver system, but it is also suitable for a wide-band receiver of the next-generation VLBI (VLBI2010). The SNR is proportional to the bandwidth, and finer phenomena can be captured with high-speed sampling, so that the ADS3000+ will hopefully break new ground in VLBI, astronomy, and science.

Development of the ADS3000+ system is a cooperative effort between NICT, JAXA/ISAS, and COSMO RESEARCH Corp². The authors would like to thank the Kashima VLBI team for their cooperation.

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²<http://www.cosmoresearch.co.jp>