SpaceCube 2.0: An Advanced Hybrid Onboard Data Processor

Two FPGAs maximize data and computing performance while minimizing physical size.

Goddard Space Flight Center, Greenbelt, Maryland

The SpaceCube 2.0 is a compact, high-performance, low-power onboard processing system that takes advantage of cutting-edge hybrid (CPU/FPGA/DSP) processing elements. The SpaceCube 2.0 design concept includes two commercial Virtex-5 field-programmable gate array (FPGA) parts protected by "radiation hardened by software" technology, and possesses exceptional size, weight, and power characteristics [5×5×7 in., 3.5 lb (≈12.7×12.7×17.8 cm, 1.6 kg) 5–25 W, depending on the application's required clock rate]. The two Virtex-5 FPGA parts are implemented in a unique back-to-back configuration to maximize data transfer and computing performance.

Draft computing power specifications for the SpaceCube 2.0 unit include four PowerPC 440s (1100 DMIPS each), 500+ DSP48Es (2×580 GMACS), 100+ LVDS high-speed serial I/Os (1.25 Gbps each), and 2×190 GFLOPS single-precision (65 GFLOPS double-precision) floating point performance. The SpaceCube 2.0 includes PROM memory for CPU boot, health and safety, and basic command and telemetry functionality; RAM memory for program execution; and FLASH/EEPROM memory to store algorithms and application code for the CPU, FPGA, and DSP processing elements. Program execution can be reconfigured in real time and algorithms can be updated, modified, and/or replaced at any point during the mission. Gigabit Ethernet, Spacewire, SATA and high-speed LVDS serial/parallel I/O channels are available for instrument/sensor data ingest, and mission-unique instrument interfaces can be accommodated using a compact PCI (cPCI) expansion card interface.

The SpaceCube 2.0 can be utilized in NASA Earth Science, Helio/Astrophysics and Exploration missions, and Department of Defense satellites for onboard data processing. It can also be used in commercial communication and mapping satellites.

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CMOS Imager Has Better Cross-Talk and Full-Well Performance

Electrically isolated areas containing imaging and readout structures are optimized separately.

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A complementary metal oxide/semiconductor (CMOS) image detector now undergoing development is designed to exhibit less cross-talk and greater full-well capacity than do prior CMOS image detectors of the same type. Imagers of the type in question are designed to operate from low-voltage power supplies and are fabricated by processes that yield device features having dimensions in the deep submicron range.

Because of the use of low supply potentials, maximum internal electric fields and depletion widths are correspondingly limited. In turn, these limitations are responsible for increases in cross-talk and decreases in charge-handling capacities. Moreover, for small pixels, lateral depletion cannot be extended. These adverse effects are even more accentuated in a back-illuminated CMOS imager, in which photogenerated charge carriers must travel across the entire thickness of the device.

The figure shows a partial cross section of the structure in the device layer of the present developmental CMOS imager. (In a practical imager, the device layer would sit atop either a heavily doped silicon substrate or a thin silicon oxide layer on a silicon substrate, not shown here.) The imager chip is divided into two areas: area C, which contains readout circuits and other electronic circuits; and area I, which contains the imaging (photodetector and photogenerated-charge-collecting) pixel structures. Areas C and I are electrically isolated from each other by means of a trench filled with silicon oxide.

The electrical isolation between areas C and I makes it possible to apply different supply potentials to these areas, thereby enabling optimization of the supply potential and associated design features for each area. More specifically, metal oxide semiconductor field-effect transistors (MOSFETs) that are typically included in CMOS imagers now reside in area C and can remain unchanged from established designs and operated at supply potentials prescribed for those designs, while the dopings and the lower supply potentials in area I can be tailored to optimize imager performance.

In area I, the device layer includes an n^+-doped silicon layer on which is grown an n^--doped silicon layer. A p^--doped silicon layer is grown on top of the n^--doped layer. The total imaging device thickness is the sum of the thickness of the n^+, n, and p^- layers. A pixel photodiode is formed between a surface n^+ implant, a p implant underneath it, the aforementioned p^- layer, and the n and n^+ layers. Adjacent to the diode is a gate for transferring photogenerated charges out of the photodiode and into a floating diffusion formed by an implanted p^+ layer on an implanted n-doped region. Metal contact pads are added to the back-side for providing back-side bias.