



SpaceCube 2.0: An Advanced Hybrid Onboard Data Processor

Two FPGAs maximize data and computing performance while minimizing physical size.

Goddard Space Flight Center, Greenbelt, Maryland

The SpaceCube 2.0 is a compact, high-performance, low-power onboard processing system that takes advantage of cutting-edge hybrid (CPU/FPGA/DSP) processing elements. The SpaceCube 2.0 design concept includes two commercial Virtex-5 field-programmable gate array (FPGA) parts protected by “radiation hardened by software” technology, and possesses exceptional size, weight, and power characteristics [5×5×7 in., 3.5 lb (=12.7×12.7×17.8 cm, 1.6 kg) 5–25 W, depending on the application’s required clock rate]. The two Virtex-5 FPGA parts are implemented in a unique back-to-back configuration to maximize data transfer and computing performance.

Draft computing power specifications for the SpaceCube 2.0 unit include four

PowerPC 440s (1100 DMIPS each), 500+ DSP48Es (2×580 GMACS), 100+ LVDS high-speed serial I/Os (1.25 Gbps each), and 2×190 GFLOPS single-precision (65 GFLOPS double-precision) floating point performance. The SpaceCube 2.0 includes PROM memory for CPU boot, health and safety, and basic command and telemetry functionality; RAM memory for program execution; and FLASH/EEPROM memory to store algorithms and application code for the CPU, FPGA, and DSP processing elements. Program execution can be reconfigured in real time and algorithms can be updated, modified, and/or replaced at any point during the mission. Gigabit Ethernet, Spacewire, SATA and high-speed LVDS serial/parallel I/O chan-

nels are available for instrument/sensor data ingest, and mission-unique instrument interfaces can be accommodated using a compact PCI (cPCI) expansion card interface.

The SpaceCube 2.0 can be utilized in NASA Earth Science, Helio/Astro-physics and Exploration missions, and Department of Defense satellites for onboard data processing. It can also be used in commercial communication and mapping satellites.

This work was done by Michael Lin, Thomas Flatley, John Godfrey, Alessandro Geist, Daniel Espinosa, and David Petrick of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15760-1

CMOS Imager Has Better Cross-Talk and Full-Well Performance

Electrically isolated areas containing imaging and readout structures are optimized separately.

NASA’s Jet Propulsion Laboratory, Pasadena, California

A complementary metal oxide/semiconductor (CMOS) image detector now undergoing development is designed to exhibit less cross-talk and greater full-well capacity than do prior CMOS image detectors of the same type. Imagers of the type in question are designed to operate from low-voltage power supplies and are fabricated by processes that yield device features having dimensions in the deep submicron range.

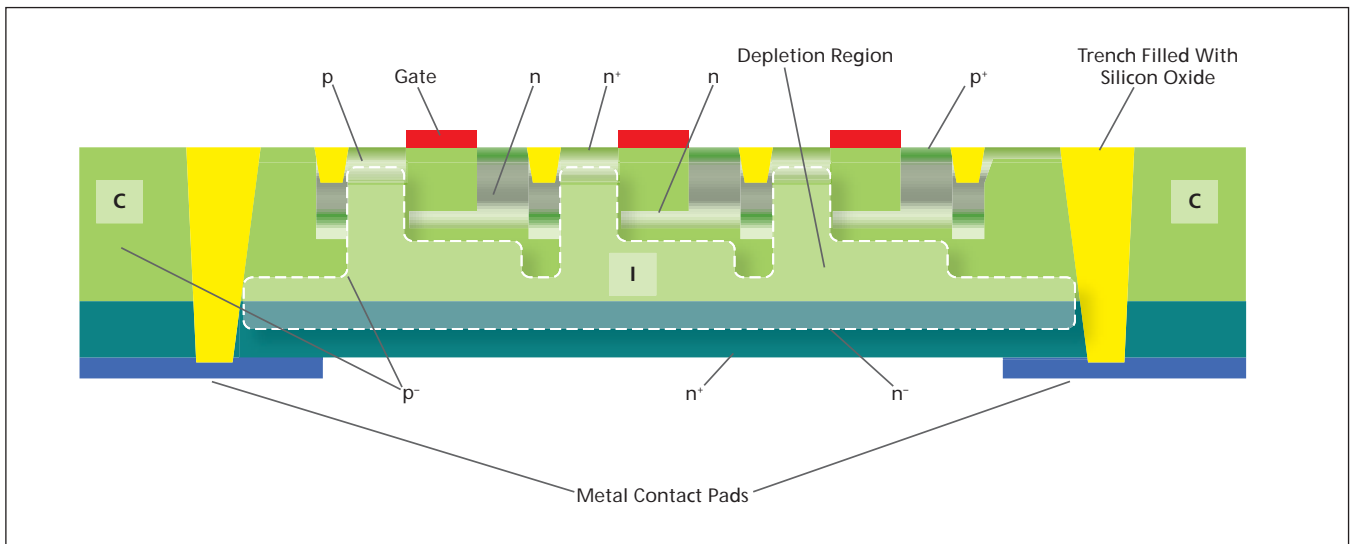
Because of the use of low supply potentials, maximum internal electric fields and depletion widths are correspondingly limited. In turn, these limitations are responsible for increases in cross-talk and decreases in charge-handling capacities. Moreover, for small pixels, lateral depletion cannot be extended. These adverse effects are even more accentuated in a back-illuminated CMOS imager, in which photogenerated charge carriers must travel across the entire thickness of the device.

The figure shows a partial cross section of the structure in the device layer of the present developmental CMOS imager. (In a practical imager, the device layer would sit atop either a heavily doped silicon substrate or a thin silicon oxide layer on a silicon substrate, not shown here.) The imager chip is divided into two areas: area C, which contains readout circuits and other electronic circuits; and area I, which contains the imaging (photodetector and photogenerated-charge-collecting) pixel structures. Areas C and I are electrically isolated from each other by means of a trench filled with silicon oxide.

The electrical isolation between areas C and I makes it possible to apply different supply potentials to these areas, thereby enabling optimization of the supply potential and associated design features for each area. More specifically, metal oxide semiconductor field-effect transistors (MOSFETs) that are typically included in CMOS imagers

now reside in area C and can remain unchanged from established designs and operated at supply potentials prescribed for those designs, while the dopings and the lower supply potentials in area I can be tailored to optimize imager performance.

In area I, the device layer includes an n⁺-doped silicon layer on which is grown an n⁻-doped silicon layer. A p⁻-doped silicon layer is grown on top of the n⁻-doped layer. The total imaging device thickness is the sum of the thickness of the n⁺, n, and p⁻ layers. A pixel photodiode is formed between a surface n⁺ implant, a p implant underneath it, the aforementioned p⁻ layer, and the n⁻ and n⁺ layers. Adjacent to the diode is a gate for transferring photogenerated charges out of the photodiode and into a floating diffusion formed by an implanted p⁺ layer on an implanted n-doped region. Metal contact pads are added to the back-side for providing back-side bias.



This **Simplified Cross Section** (not to scale) shows essential features of the developmental device structure. A key feature of the structure is the depletion region (indicated by the dashed outline) along the entire n^-/p^- junction.

The n^- and p^- doping concentrations are chosen such that everywhere in area I, a depletion region exists between the n^- and p^- layers. This depletion region enables electrical isolation between the several front (top) doped regions and the back (bottom) n and n^+ layers. Consequently, the bias potentials applied to the top of the diode and the adjacent transfer gate can be different from the bias applied to the bottom. Thus, while CMOS-compatible potentials (e.g., 3 V) are applied at the top, the bottom of the structure can be biased to greater potential (e.g., 5 V) via the back-side metal contact pads to completely deplete the photodiode. The re-

sulting depletion region is indicated in the figure as the area enclosed by the dashed outline. Complete depletion of the photodiode results in collection of charge carriers (holes in this case) under the influence of an electric field, and hence, a significant reduction of cross-talk. Complete depletion also increases the charge-storage volume, and, hence, the charge-handling capacity. Thus, the structure described here provides for large depletion width around each photodiode, independent of the CMOS power-supply voltage and pixel size.

This work was done by Bedabrata Pain and Thomas J. Cunningham of Caltech for NASA's

Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-45964, volume and number of this NASA Tech Briefs issue, and the page number.

High-Performance Wireless Telemetry

This technology is applicable to any kind of aviation or power-plant turbine testing.

John H. Glenn Research Center, Cleveland, Ohio

Prior technology for machinery data acquisition used slip rings, FM radio communication, or non-real-time digital communication. Slip rings are often noisy, require much space that may not be available, and require access to the shaft, which may not be possible. FM radio is not accurate or stable, and is limited in the number of channels, often with channel crosstalk, and intermittent as the shaft rotates. Non-real-time digital communication is very popular, but complex, with long development time, and objections from users who need continuous waveforms from many channels.

This innovation extends the amount of information conveyed from a rotating machine to a data acquisition system

while keeping the development time short and keeping the rotating electronics simple, compact, stable, and rugged. The data are all real time. The product of the number of channels, times the bit resolution, times the update rate, gives a data rate higher than available by older methods. The telemetry system consists of a data-receiving rack that supplies magnetically coupled power to a rotating instrument amplifier ring in the machine being monitored. The ring digitizes the data and magnetically couples the data back to the rack, where it is made available.

The transformer is generally a ring positioned around the axis of rotation with one side of the transformer free to

rotate and the other side held stationary. The windings are laid in the ring; this gives the data immunity to any rotation that may occur.

A medium-frequency sine-wave power source in a rack supplies power through a cable to a rotating ring transformer that passes the power on to a rotating set of electronics. The electronics power a set of up to 40 sensors and provides instrument amplifiers for the sensors. The outputs from the amplifiers are filtered and multiplexed into a serial ADC. The output from the ADC is connected to another rotating ring transformer that conveys the serial data from the rotating section to the stationary section. From there, a cable conveys the serial data to