The **Half Cell** on the left contains a graphite cathode pellet behind a solid-electrolyte film. The half cell on the right contains a graphite/iodine pellet behind a solid-electrolyte film; the darkening of this cell was caused by diffusion of iodine through the solid electrolyte.

Four-Quadrant Analog Multipliers Using G^4-FETs

Devices with independently biased multiple inputs are exploited to simplify multiplier circuits.

NASA's Jet Propulsion Laboratory, Pasadena, California

Theoretical analysis and some experiments have shown that the silicon-on-insulator (SOI) 4-gate transistors known as G^4-FETs can be used as building blocks of four-quadrant analog voltage multiplier circuits. Whereas a typical prior analog voltage multiplier contains between six and 10 transistors, it is possible to construct a superior voltage multiplier using only four G^4-FETs.

A G^4-FET is a combination of a junction field-effect transistor (JFET) and a metal oxide/semiconductor field-effect transistor (MOSFET). It can be regarded as a single transistor having four gates, which are parts of a structure that affords high functionality by enabling the utilization of independently biased multiple inputs. The structure of a G^4-FET of the type of interest here (see Figure 1) is that of a partially-depleted SOI MOSFET with two independent body contacts, one on each side of the channel. The drain current comprises of majority charge carriers flowing from one body contact to the other — that is, what would otherwise be the side body contacts of the SOI MOSFET are used here as the end contacts [the drain (D) and the source (S)] of the G^4-FET. What would otherwise be the
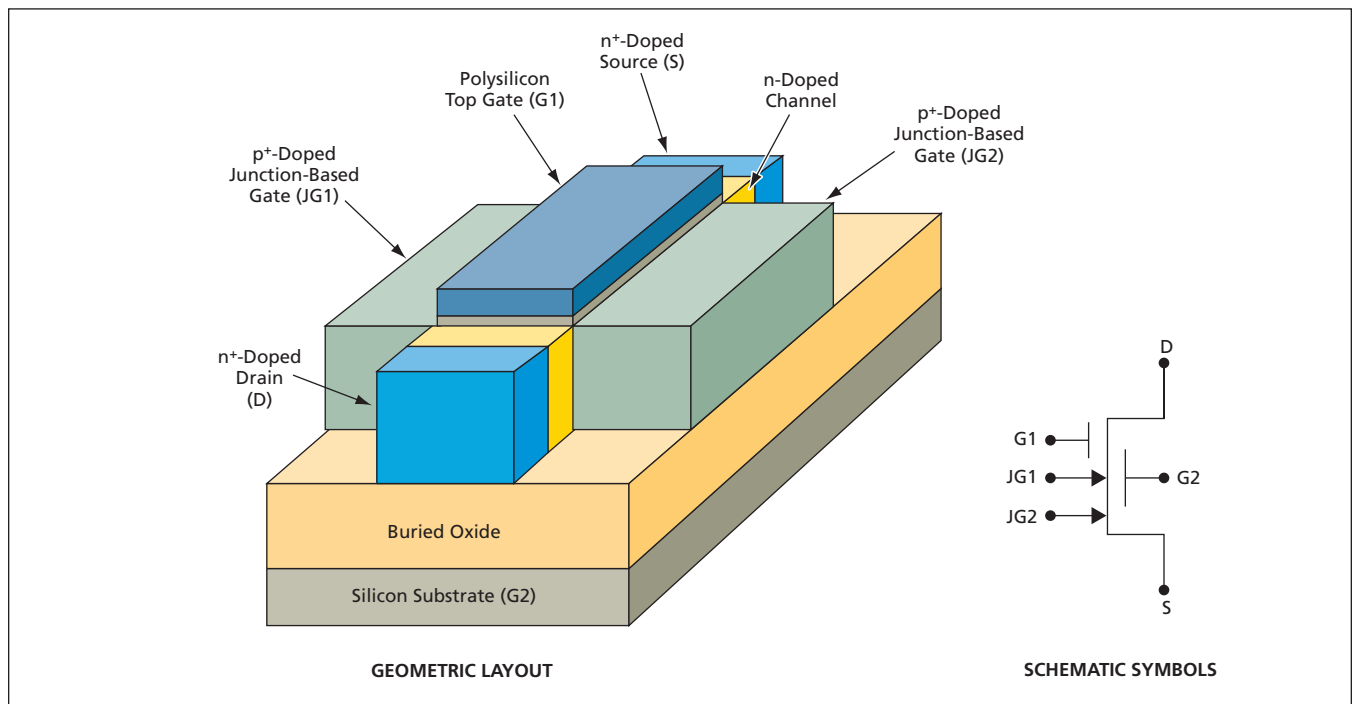

Figure 1. In this **G^4-FET**, the top gate plays the same role as does the sole gate in a conventional accumulation-mode MOSFET. The side gates (JG1 and JG2) provide additional degrees of freedom for design and operation, beyond those of a conventional MOSFET.
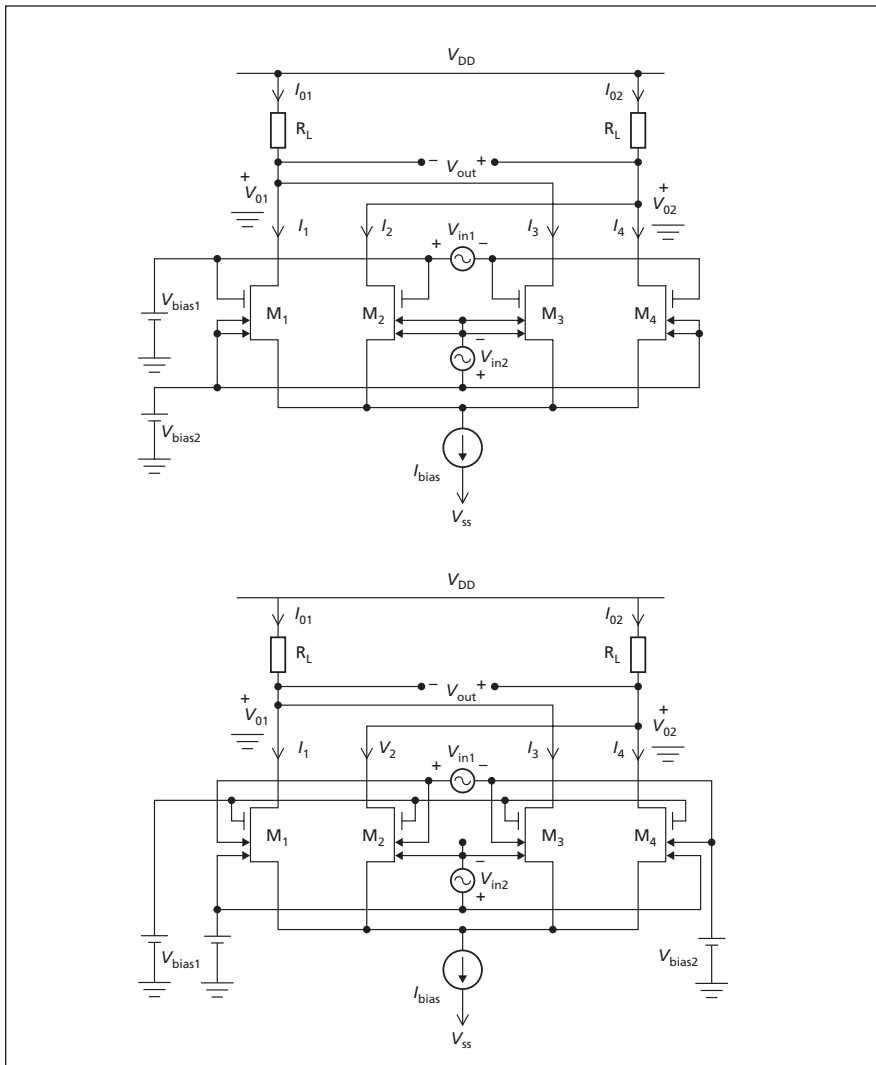
Figure 2. These **Two G⁴-FET Analog Multiplier Circuits** are examples of implementation of four-quadrant multipliers using fewer transistors than were previously required for such multipliers.

- The multiplier core consists of four G^4-FETs (M1 through M4) biased by a constant current sink (I_{bias}), and
- The G^4-FETs in two pairs are loaded by two identical resistors (R_L), which convert a differential output current to a differential output voltage.

The difference between the two circuits stems from their input and bias configurations. In each case, provided that the input voltages remain within their design ranges as determined by considerations of bias, saturation, and cutoff, then the output voltage is nominally given by $V_{out} = kV_{in1}V_{in2}$, where k is a constant gain factor that depends on the design parameters and is different for the two circuits.

In experimental versions of these circuits constructed using discrete G^4-FETs and resistors, multiplication of voltages in all four quadrants (that is, in all four combinations of input polarities) was demonstrated, and deviations of the output voltages from linear dependence on the input voltages were found to amount to no more than a few percent. It is anticipated that in fully integrated versions of these circuits, the deviations from linearity will be made considerably smaller through better matching of devices.

source and drain of the SOI MOSFET serve, in the G⁴-FET, as two junction-based extra gates (JG1 and JG2), which are used to squeeze the channel via reverse-biased junctions as in a JFET. The G⁴-FET also includes a polysilicon top gate (G1), which plays the same role as does the gate in an accumulation-mode MOSFET. The substrate emulates a fourth MOS gate (G2).

By making proper choices of G⁴-FET device parameters in conjunction with bias voltages and currents, one can design a circuit in which two input gate voltages (V_{in1}, V_{in2}) control the conduction characteristics of G⁴-FETs such that the output voltage (V_{out}) closely approximates a value proportional to the product of the input voltages. Figure 2 depicts two such analog multiplier circuits. In each circuit, there is the following:

- The input and output voltages are differential,

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