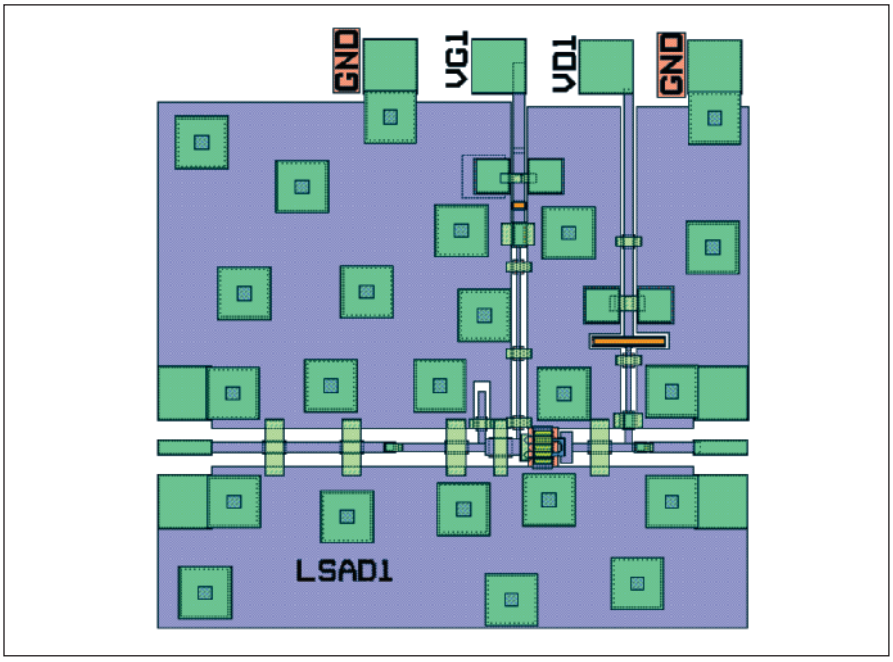



Figure 1. This **MMIC** embodies an active frequency doubler rated for a nominal output frequency of about 300 GHz.

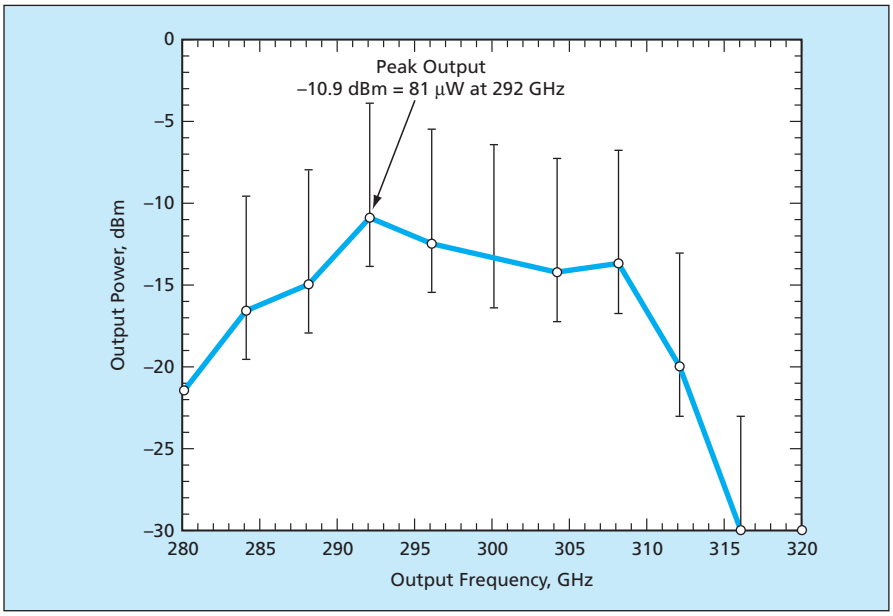



Figure 2. The **Output Power** of the MMIC of Figure 1 was measured at several output frequencies from 280 to 316 GHz.

blers lies in the fact that they can be integrated with amplifiers, oscillators, and other circuitry on MMIC chips.

The circuitry of the doubler MMIC (see Figure 1) features grounded coplanar waveguides. Air bridges and vias are used to make contact with the ground plane. The HEMT is biased for Class-A operation (in which current is conducted throughout each cycle of oscillation), which would ordinarily be better suited to linear amplification than to frequency doubling. Ordinarily, class-B operation (in which current is conducted during about half of each cycle of oscillation) would be more suitable for frequency doubling because of the essential nonlinearity of partial-cycle conduction. The reason for the unusual choice of class A was that computational simulations had shown that in this case, the efficiency in class B would be less than in class A.

The input matching circuit of this doubler includes transmission lines that afford a good impedance match at the fundamental frequency, plus an open stub to prevent leakage of the second harmonic through the input terminals. The output circuit was designed to suppress the fundamental while providing a good match for the second harmonic.

In a test, this doubler was driven by an input signal at frequencies from 140 to 158 GHz and its output at the corresponding second-harmonic frequencies of 280 to 316 GHz was measured by means of a power meter connected to the MMIC via waveguide wafer probes and a high-pass (fundamental-suppressing) waveguide. The results of this test are summarized in Figure 2.

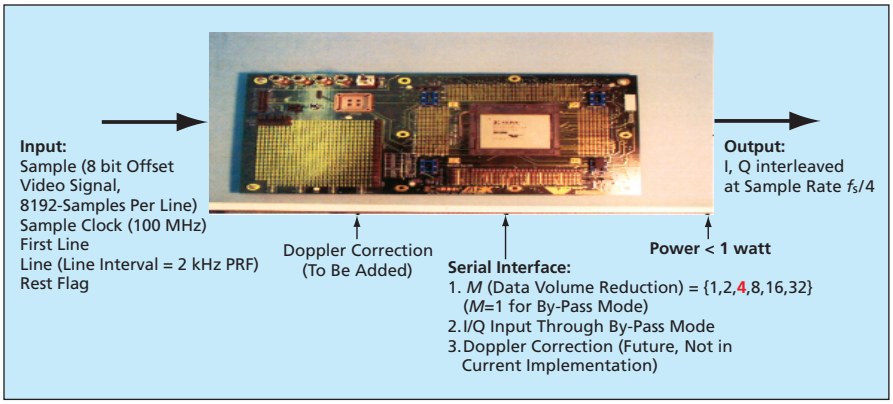
*This work was done by Lorene Samoska and Jean Bruston of Caltech for* **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*
*NPO-30581*

# Single-Chip FPGA Azimuth Pre-Filter for SAR

## Range resolution is reduced by a selectable factor to reduce the volume of data.

*NASA's Jet Propulsion Laboratory, Pasadena, California*

A field-programmable gate array (FPGA) on a single lightweight, low-power integrated-circuit chip has been developed to implement an azimuth pre-filter (AzPF) for a synthetic-aperture radar (SAR) system. The AzPF is needed to enable more efficient use of data-transmission and data-processing resources: In broad terms, the AzPF reduces the volume of SAR data by effectively reducing the azimuth resolution, without loss of range resolution, during times when end users are willing to accept lower azimuth resolution as the price of rapid access to SAR imagery. The data-reduction factor is selectable at a decimation factor, *M*, of 2, 4, 8, 16, or 32 so that users can trade




The **Prototype Circuit Board** measures 6 by 10 in. (15.2 by 25.4 cm). The AzPF integrated circuit mounted on the board measures only about 2.5 in. (≈6.4 cm) square and consumes a power <1 W. The performance requirements are as follows: (1) Range resolution: No degradation in range resolution; (2) Azimuth resolution: 1/*M* of original resolution for a single look; (3) Peak to side-lobe ratio (PSLR) after Hamming window: -25 dB; and (4) Integrated side-lobe ratio (ISLR) after Hamming window: -15 dB.

resolution against processing and transmission delays.

In principle, azimuth filtering could be performed in the frequency domain by use of fast-Fourier-transform processors. However, in the AzPF, azimuth filtering is performed in the time domain by use of finite-impulse-response filters. The reason for choosing the time-domain approach over the frequency-domain approach is that the time-domain approach demands less memory and a lower memory-access rate.

The AzPF operates on the raw digitized SAR data. The AzPF includes a digital in-phase/quadrature (I/Q) demodulator. In general, an I/Q demodulator effects a complex down-conversion of its input signal followed by low-pass filtering, which eliminates undesired sidebands. In the AzPF case, the I/Q demodulator takes offset video range echo data to the complex baseband domain, ensuring preservation of signal phase through the azimuth pre-filtering process. In general, in an SAR I/Q demodulator, the intermediate frequency ($f_I$) is chosen to be a quarter of the range-sampling frequency and the pulse-repetition frequency ($f_{PR}$) is chosen to be a multiple of $f_I$.

The AzPF also includes a polyphase spatial-domain pre-filter comprising four weighted integrate-and-dump filters with programmable decimation factors and overlapping phases. To prevent aliasing of signals, the bandwidth of the AzPF is made 80 percent of $f_{PR}/M$. The choice of four as the number of overlapping phases is justified by prior research in which it was shown that a filter of length $4M$ can effect an acceptable transfer function.

The figure depicts prototype hardware comprising the AzPF and ancillary electronic circuits. The hardware was found to satisfy performance requirements in real-time tests at a sampling rate of 100 MHz.

*This work was done by Mimi Gudim, Tsan-Huei Cheng, Soren Madsen, Robert Johnson, Charles T-C Le, Mahta Moghaddam, and Miguel Marina of Caltech for* **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*
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