



Parylene C as a Sacrificial Material for Microfabrication

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Parylene C has been investigated for use as a sacrificial material in microfabrication. Although Parylene C cannot be patterned lithographically like photoresists, it nevertheless extends the range of processing options by offering a set of properties that are suitable for microfabrication and are complementary to those of photoresists. The compatibility of Parylene C with several microfabrication processes was demonstrated in experiments in which a thin film of Parylene C was deposited on a silicon wafer, then several thin metal films were deposited and successfully patterned, utilizing the Parylene C pads as a sacrificial layer.

The term "parylene" — a contraction of "poly(para-xylene)" — denotes a family of vapor-deposited polymers. In Parylene C (the most common form of parylene), a chlorine atom is substituted for one of the hydrogen atoms on the benzene ring of each para-xylene moiety. Heretofore, parylenes have been used as conformal coating materials in diverse applications.

The unique combinations of processing properties of Parylene C that make it suitable for use in microfabrication are the following:

- It can be deposited to uniform sub-micron thickness.
- It is highly resistant to solvents and, therefore, able to survive wet processing.

- It can easily be patterned or removed by use of oxygen plasma.
- Because it cannot be easily patterned or removed by means other than oxygen plasma, it can withstand many dry etching processes.
- It has little or no outgassing and is fully functional at cryogenic temperatures.

This work was done by Michael Beamesderfer of Goddard Space Flight Center.

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, Goddard Space Flight Center, (301) 286-7351. Refer to GSC-14803-1.

In Situ Electrochemical Deposition of Microscopic Wires

Tedious, expensive post-growth assembly is no longer necessary.

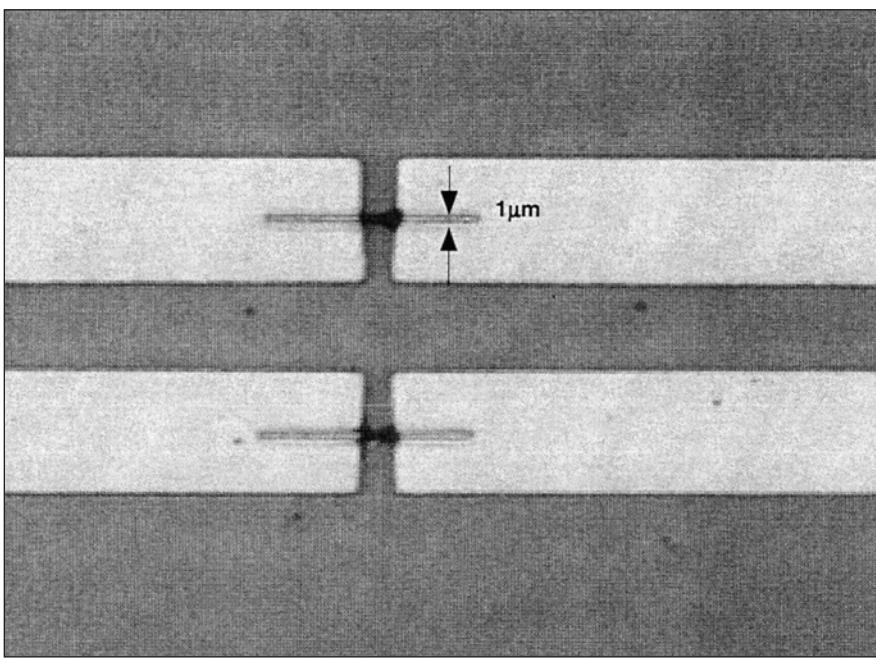
NASA's Jet Propulsion Laboratory, Pasadena, California

A method of fabrication of wires having micron and submicron dimensions is built around electrochemical deposition of the wires in their final positions be-

tween electrodes in integrated circuits or other devices in which the wires are to be used. Heretofore, nanowires have been fabricated by a variety of techniques char-

acterized by low degrees of controllability and low throughput rates, and it has been necessary to align and electrically connect the wires in their final positions by use of sophisticated equipment in expensive and tedious post-growth assembly processes. The present method is more economical, offers higher yields, enables control of wire widths, and eliminates the need for post-growth assembly. The wires fabricated by this method could be used as simple electrical conductors or as transducers in sensors. Depending upon electrodeposition conditions and the compositions of the electroplating solutions in specific applications, the wires could be made of metals, alloys, metal oxides, semiconductors, or electrically conductive polymers.

In this method, one uses fabrication processes that are standard in the semiconductor industry. These include cleaning, dry etching, low-pressure chemical vapor deposition, lithography, dielectric deposition, electron-beam lithography, and metallization processes as well as the electrochemical deposition process used to form the wires. In a typical case of fabrication of a circuit that includes electrodes between which microscopic wires are to be formed on a silicon substrate,



Palladium Wires 1 μm wide and 5 μm long were formed in contact with gold electrodes by electrodeposition into 1- μm -wide channels from a solution of $\text{Pd}(\text{NH}_2)_2(\text{NO}_2)_2$ at a concentration of 10 g/L and ammonium sulfamate at a concentration of 100 g/L.

the fabrication processes follow a standard sequence until just before the fabrication of the microscopic wires.

Then, by use of a thermal SiO-deposition technique, the electrodes and the substrate surface areas in the gaps between them are covered with SiO. Next, the SiO is electron-beam patterned, then reactive-ion etched to form channels having specified widths (typically about 1 μm or less) that define the widths of the wires to be formed. Drops of an electroplating solution are placed on the substrate in the regions containing the channels thus

formed, then the wires are electrodeposited from the solution onto the exposed portions of the electrodes and into the channels. The electrodeposition is a room-temperature, atmospheric-pressure process. The figure shows an example of palladium wires that were electrodeposited into 1-mm-wide channels between gold electrodes.

This work was done by Minhee Yun, Nosang Myung, and Richard Vasquez of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-40221, volume and number of this NASA Tech Briefs issue, and the page number.

E Improved Method of Manufacturing SiC Devices

Several improvements promise to make manufacture of SiC devices more economical.

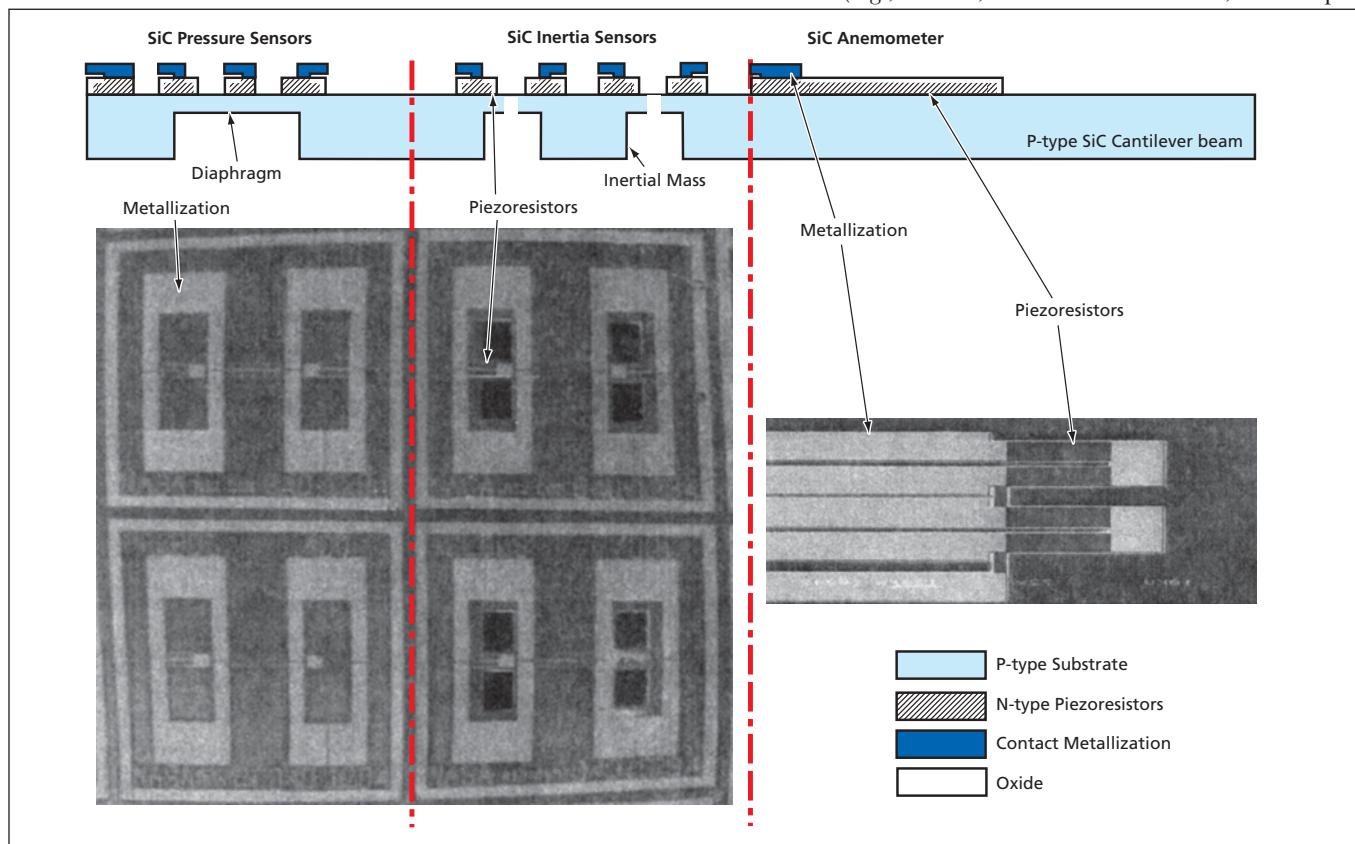
John H. Glenn Research Center, Cleveland, Ohio

The phrase, "common-layered architecture for semiconductor silicon carbide" ("CLASSiC") denotes a method of batch fabrication of microelectromechanical and semiconductor devices from bulk silicon carbide. CLASSiC is the latest in a series of related methods developed in recent years in continuing efforts to standardize SiC-fabrication

processes. CLASSiC encompasses both institutional and technological innovations that can be exploited separately or in combination to make the manufacture of SiC devices more economical. Examples of such devices are piezoresistive pressure sensors, strain gauges, vibration sensors, and turbulence-intensity sensors for use in harsh environments (e.g.,

high-temperature, high-pressure, corrosive atmospheres).

The institutional innovation is to manufacture devices for different customers (individuals, companies, and/or other entities) simultaneously in the same batch. This innovation is based on utilization of the capability for fabrication, on the same substrate, of multiple



Two Pressure Sensors, Two Accelerometers, and an Anemometer were fabricated on the same SiC substrate to demonstrate the capability for simultaneous batch fabrication of devices that perform different functions. Cross-sectional views of devices are also shown.