Investigation of Current Spike Phenomena During Heavy Ion Irradiation of NAND Flash Memories

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***Abstract*—A series of heavy ion and laser irradiations were performed to investigate previously reported current spikes in flash memories. High current events were observed, however, none matches the previously reported spikes. Plausible mechanisms are discussed.**

I. Introduction

We report the results of a heavy ion and laser experiments intended to reproduce the destructive current spikes reported in [1, 2], but not observed in other studies [3]. We used the same part types, and duplicated the beam conditions. Although a total of 52 high current events were observed, none matched the 300-400 ms pulses described in [1, 2]. Our results seem to be explained nicely by the mechanisms proposed by Shindou et al, [4], and we will discuss our results in light of these mechanisms. To shed more light on the mechanisms underlying high current events, pulsed laser experiments were conducted, using the Naval Research Laboratory (NRL) laser [5], to identify regions on the chip where high currents can be induced. We have also conducted heavy ion experiments using the Micro-RDC Milli-Beam™ system [6], which collimates the beam, so that only a small part of the die is exposed at any one time. The Micro-RDC Milli-Beam™ experiment serves as a novel method to confirm both the laser experiments and broad beam heavy ion exposures reported previously [1-3].

II. Description of Devices Under Test (DUT)

The samples used in the various tests are described in Table I. The parts all have a single power supply, 2.7-3.6 V full range, and 3.3 V nominal, which means there is an on-chip charge pump to produce the higher voltages needed to write and erase. The parts have 4096 blocks, of which up to 80 can be "bad" initially (not fully functional)—the manufacturer identifies the bad blocks, so that they can be screened out. In our samples, most had only a few bad blocks, but none came close to 80. Maximum operating frequency is 40 MHz., in all cases.

III. Experimental Procedure

In Single Event Effects (SEE) testing, all exposures were with stored logical checkerboard. For single bit upsets, zero-to-one errors are normally observed, but errors of the opposite polarity are often observed if they originate in the control logic. For example, one of the common Single Event Functional Interrupt (SEFI) modes is for an entire block, 128Kx8 bits, to be read as all zeroes. If the block had had all zeroes stored, no error would have been detected. The testing was performed at Texas A&M University (TAMU) Cyclotron [7] and at Lawrence Berkeley National Laboratory (LBNL) [8] using the ions indicated in Table II.

Table I. Parts used in testing.

Mfr	Part No.	LDC	Package	Blocks	Pages/Block	Page Size (bits)	Feature Size (nm)	Tests Performed
Micron	MT29F4G08AAA	748	TSOP-48	4096	64	2Kx8	73	HI-TAMU
Micron	MT29F4G08ABADA	0M*	BGA-63	4096	64	2Kx8	73	Laser, HI-LBNL
Samsung	K9F8G08U0M	807	TSOP-48	4096	64	4Kx8	60	HI-TAMU

*Abbreviated Lot Date Code (LDC) used on Ball Grid Array (BGA) parts: 0 indicates 2010, M indicates 26th workweek.

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TABLE II: IONS/ENERGIES AND LINEAR ENERGY TRANSFER (MEV•CM^2) (LETS) FOR THE TAMU AND LBNL TESTS.

TAMU Ions					
Ion	**Energy/ AMU**	**Energy (MeV)**	**Approx. LET (MeV•cm^2/g)**	**Angle**	**Eff. LET**
Xe	15	1935	53.9	0, 50	53.9, 84
Au	15	2955	87.5	0, 50	87.5, 138
LBNL Ions					
Xe	10	1290	59	0	59

For SEE testing, bias and operating conditions included:

1) Static/biased irradiation, in which a pattern was written and verified, and then irradiated. Once the desired fluence was reached, the run was stopped. The memory contents were read and errors tallied.
2) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.
3) Dynamic Read/Erase/Write (R/E/W), which again was similar to the Dynamic Read, except that a word in error was first erased and then rewritten. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these high voltage operations.

In this set of experiments, we have included an initial attempt to look at angular effects, which may include multiple bits grazed by the same ion, and other effects due to charge sharing by multiple nodes in the control logic. This test was done at 50 degrees, which was the highest angle we could use, without the DUT socket shadowing the beam.

In all cases, the power supply current was monitored, and recorded. The electronic recording system had better than 1 ms resolution. Current was also displayed on a digital oscilloscope trace, so that current level changes could be observed in real time.

In the laser test, we used only the Dynamic Read mode, because we knew the laser would not upset the storage cells.

In the Milli-Beam® test at LBNL [8], we used only Xe ions in their 10 MeV/amu cocktail. We exposed all the peripheral control circuits in Dynamic Read mode, and started through the circuit again in Dynamic R/E/W mode, but did not have time to finish the entire circuit.

IV. RESULTS

Though the same parts were used for comparison with previous results, the NASA Low Cost Digital Tester (LCDT) system, rather than the test system described in [1, 2], was used. The LCDT [9] is a reconfigurable Field Programmable Gate Array (FPGA) controlled tester. The responsibility of the LCDT is to control the DUT inputs and to process the DUTs outputs during testing. Although the LCDT's board components do not change from DUT to DUT, the DUT controls and processing does change via FPGA reconfiguration.

Common approaches to FPGA-based testers use processors such as Power-PCs or other micro-processors contained within the FPGA device to control and process DUT Input/Output (I/O). The issue with these approaches is that a processor based controller loses fine grain control and visibility of the DUT during testing. The power behind the REAG LCDT test process is that DUT control and processing is custom designed per DUT. No microprocessor is used within the LCDT FPGA; however, the FPGA is able to have the finest grain control and visibility. The advantages of this approach are:

- High speed testing capability – the tester is not limited by fetch/execute cycles and memory latency
- Fine grained control and visibility of the DUT I/O
  - No hidden command (such as No-ops)
  - All clock cycles are account for
  - DUT outputs can be monitored with a custom approach
  - At speed Single Event Upset (SEU) determination

The previously reported current spikes were described as having a typical pulse width of 300-400 ms. For the new broad beam experiment, a total of 52 high current events were observed. These events varied in period, however, none appeared as short as previously reported [1, 2]. The shortest newly observed events were nearly an order of magnitude longer. Forty-eight of the 52 events are rectangular, stair step waveforms which were identified in [4] as being caused by localized Single Event Latchup (SELs), where a small part of the circuit latches up. They observed that rest of the circuit remains fully functional, however, because sufficient bias voltage is maintained. The stair step structure occurs because one localized region undergoes SEL, then another, and perhaps then yet another, each changing the power supply current level. These events have duration ranging from a few seconds to several minutes. In fact, many of them ended only because of operator intervention. An example from our new data is shown in Fig. 1. The power supply current limit on this run was 100 mA, so the shape of the waveform is not due to current limiting.

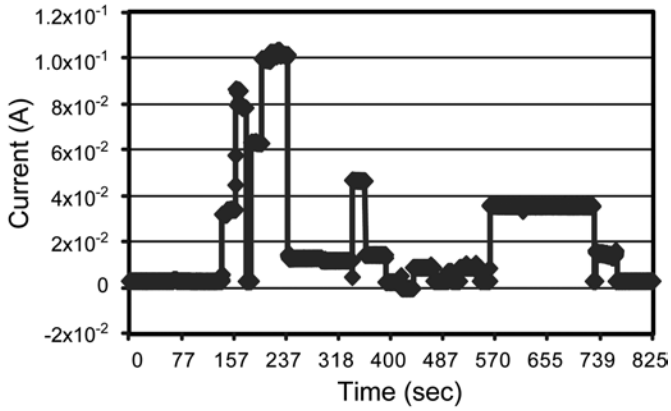

Fig. 1. Samsung DUT 1, Run 1, Static mode, Xe ions. Current history versus time.

In Fig. 1, two high current events were observed, with stair-step structure characteristic of Localized Single Event Latchup (LSEL) [4]. The beam was turned off after the second high current event, at about t=300 sec. Current level changes after the beam was off are due to actions performed to reset the part for the next exposure. Interval baseline-to-baseline was 37 sec for the first event, 57 sec for the second. In this instance, the DUT failed, losing both Erase and Program (write) functions. In all, eight parts (four Micron and four Samsung) failed on a total of 38 beam runs.

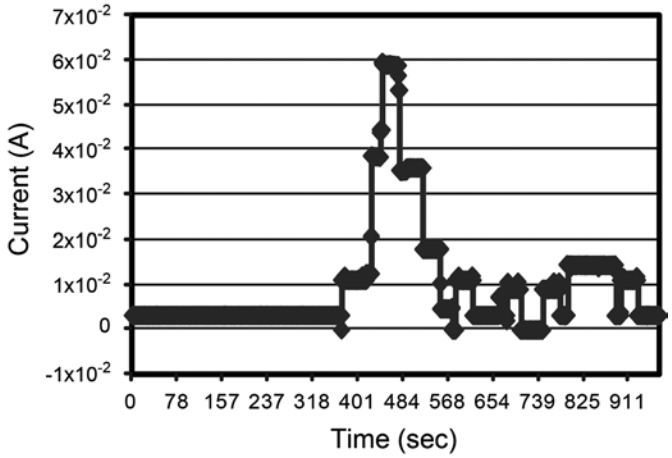

Fig. 2. Samsung DUT 3, Run 2, Xe ions, Dynamic Read mode. Current history versus time.

In Fig. 2, there is one high current event, with stair-step structure, with duration from baseline-to-baseline about three minutes. In this case, no failure occurred, an example of a high current event without failure.

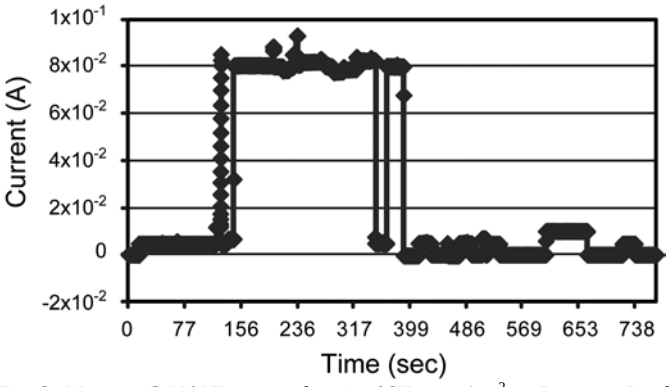

Fig. 3. Micron 4G NAND exposed to 2x106Xe ions/cm^2 in Dynamic Read mode. DUT survived, and was used on the next shot. Current history versus time.

In Fig. 3, there are two events shown here with rectangular waveforms, both of which reach a current of 80 mA in one step. A total of 48 rectangular waveforms were observed on all runs, however, several runs had multiple stair steps, such as in Figs. 1 and 2, before reaching their peak current. Here, in Fig. 3, the duration of these events is more than three minutes for the longer one, and about 25 seconds for the shorter one. Again these are attributed to LSELs in Shindou et al. [4]. The first high current event from Fig. 3 is the very shortest duration event of all 52 events. It is shown on an expanded time scale in Fig. 4, with baseline-to-baseline duration about 1 second.

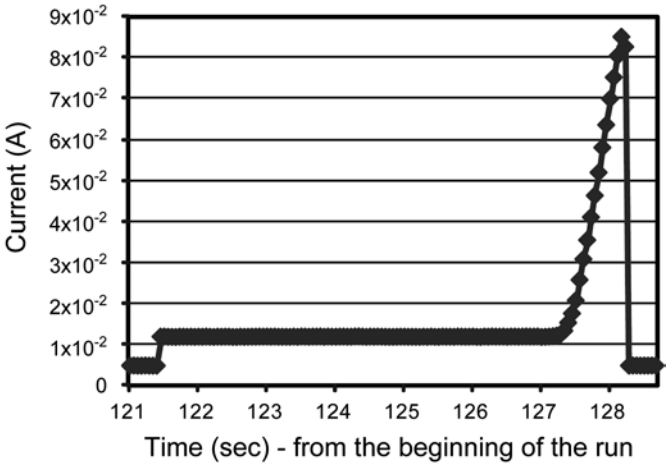

Fig. 4. Transient from Fig. 1 on an expanded time scale. Current versus time.

In Shindou et al. [4] events similar to this are referred to as "pseudo-SELs", meaning the current increases rapidly, as in a true SEL, but the mechanism is contention on the data bus lines, rather than SEL. Bus contention results when two or more portions of the control logic are on at the same time, when they are not both supposed to be on, and they end up fighting for control. This makes intuitive sense: if a heavy ion strike occurs in a control register, changes in operating modes can take place, i.e., SEFIs [10]. In this case, the DUT is receiving continuous commands to Read, and initially the current is at about 5 mA, which is the nominal Read current for this part. But there comes a point where the current jumps to about 10 mA, which is the nominal Write current for this

part. It is not really clear whether the part is really trying to Write, or not. A watchdog timer error occurred, which meant the DUT had stopped responding to Read commands. A few seconds after the event began, and Read command response had stopped, contention took place, and the current increased rapidly. The contention was resolved when another Read command was received, and the current dropped back to the nominal Read current level, and the DUT started to operate properly, again.

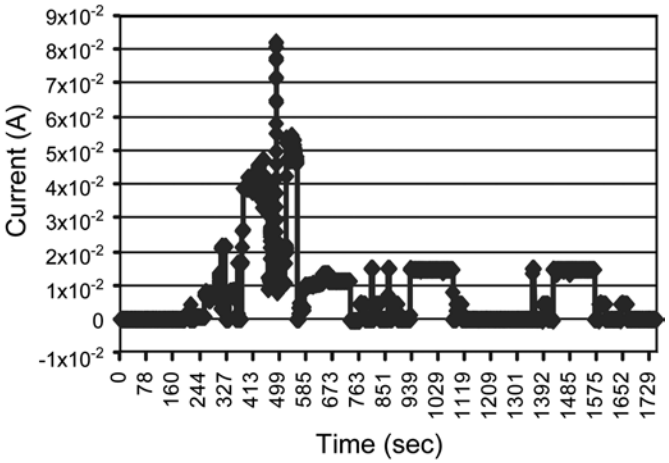

Fig. 5. Micron DUT 21, Run 5, Xe ions, Static mode. Erase and Write functions both failed. Current versus time.

In Fig. 5, we show another three high current events, the first lasting about two minutes, and the last lasting 37 sec. The second event, which is much shorter, is an apparent example of bus contention, and is shown on an expanded time scale in Fig. 6. However, it differs from the example in Fig. 4 because the DUT was in Static mode. This means the sample was not receiving any commands during the exposure. In Fig. 6, the baseline current initially is about 17 mA, compared to nominal current in Static mode for this part of <1 mA, which clearly indicates that there is activity not driven by commands from the test system. In this case, after the high current ends, the baseline current drops to about 12 mA. Since this value is lower than the current before the contention, it suggests that some activity stopped, or changed modes, as a result of the contention. Contention duration is about 1.7 seconds.

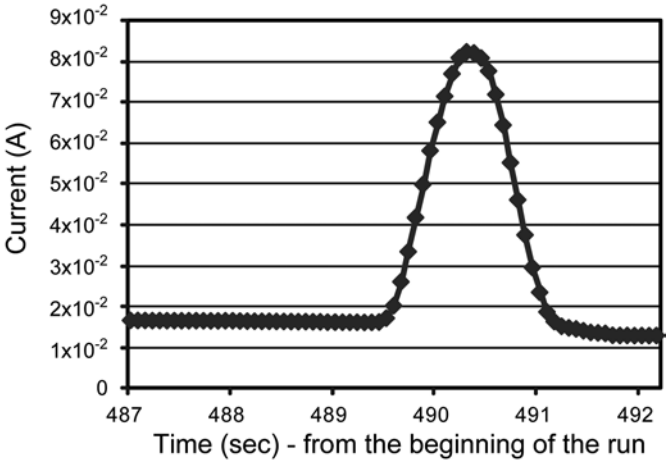

Fig. 6 Micron DUT 21, Run 5, Xe ions, Static mode. Second high current event, shown on an expanded scale. Current versus time.

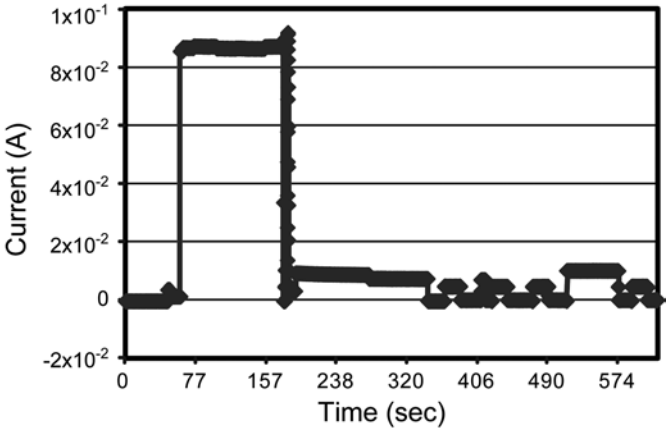

Fig. 7. Micron DUT 20—Run 9. Static mode, with fluence 1x106 Xe ions/cm^2. There are two high current events on this Run, although they appear to run together on this scale. Current versus time.

In Fig. 7, we show another current trace with two high current events, one lasting about two minutes, and a much shorter event which is difficult to resolve on this scale. It is shown on an expanded time scale in Fig. 8. In Fig. 8, the baseline current is about 10 mA, initially, compared to normal Static mode current less than 1 mA. The higher than expected initial current suggests activity driven by Single Event Transients (SETs). Then an apparent bus contention occurs, presumably because there are parts of the circuit on that are not supposed to be on at the same time. After the contention is resolved, the current drops to about 3 mA, suggesting that some of the SET-driven activity stops, consistent with the discussion of Figs. 5 and 6. Duration of this contention event is about 1.3 seconds.

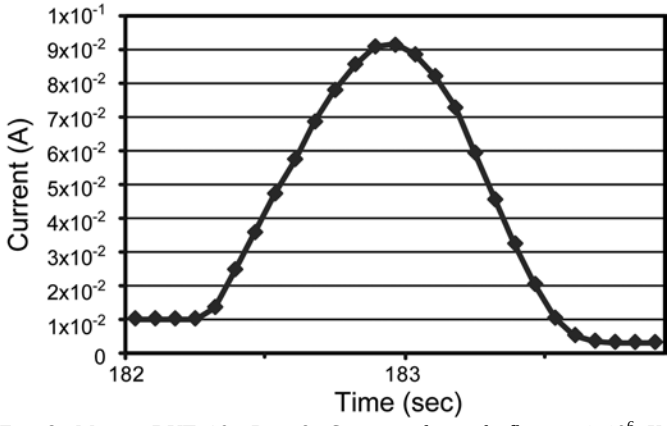

Fig. 8. Micron DUT 20—Run 9. Static mode, with fluence $1x10^6$ Xe ions/cm2. High current transient with an expanded time scale. Current versus time.

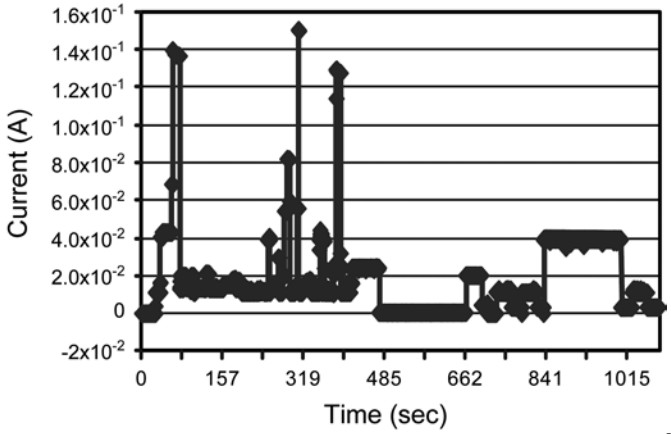

Fig. 9. Samsung DUT 4—Run 18. Dynamic Read mode, with fluence $3x10^6$ Au ions/cm2. Watchdog timer error, and DUT failed, losing both erase and write functions. Current versus time.

In Fig. 9, we show a current trace with five events where the current exceeds 40 mA. The event with the shortest duration, and also the highest current level is shown on an expanded scale in Fig. 10. The current is above 60 mA for about 1.4 seconds, but the trace has the stair-step structure and square corners characteristic of LSEL.

In Fig. 11, we present a histogram of the 52 high current events that we observed in the TAMU heavy ion experiment. The duration, baseline-to-baseline, for each high current event is tabulated, and the results are shown in Fig. 11. None of the events lasts less than 1 second, and most last tens of seconds or minutes. Although it is not indicated in the Figure, many ended when they did because of operator intervention, and not spontaneously. None was in the range of 300-400 ms, although the shortest one was within about a factor of 3.

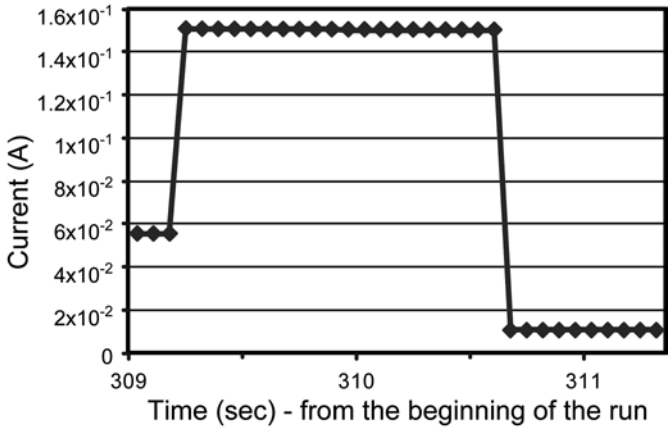

Fig. 10. Highest peak current event in Fig. 9, shown on an expanded time scale. Total duration of the entire trace is about 2 seconds. Current versus time.

Note: Vertical axis should say “Number of events”.

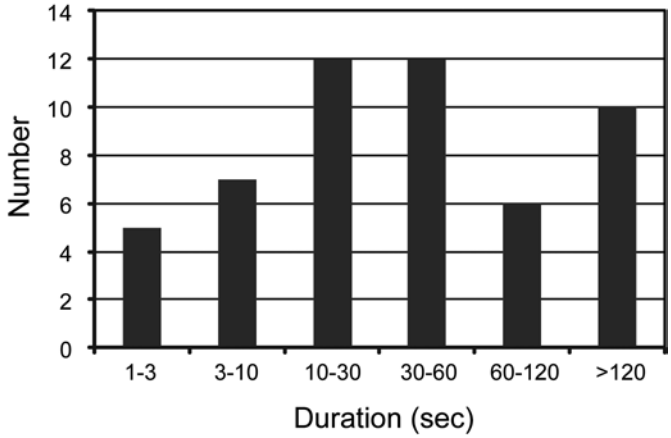

Fig. 11. Duration in seconds of all 52 high current events observed in this experiment.

In Fig. 12, we show the results of the pulsed laser test at NRL. Darks spots indicate locations where high current, 80 mA or more, was observed. Light spots indicate locations where SEFIs, without high current, were observed. There are 38 locations where high currents were triggered by the laser, including almost anywhere in the peripheral control logic. Note that there are no high current events in the regions believed to be the charge pumps (white rectangles). This result is very difficult to reconcile with the conclusion in [1, 2], that the high currents are coming from the charge pumps.

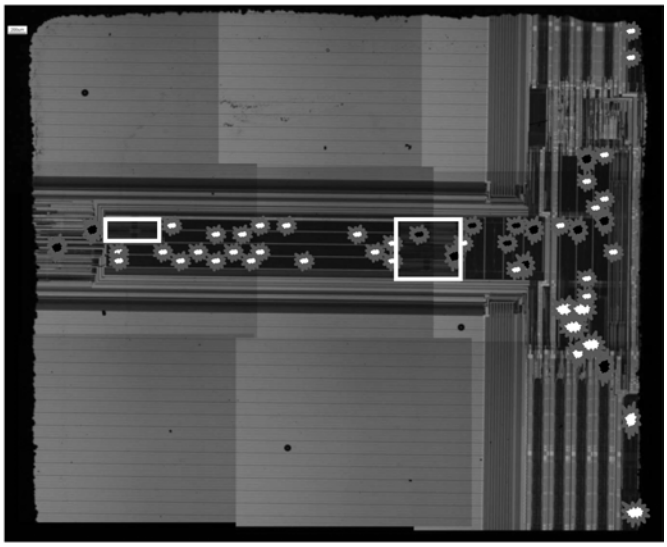

Fig. 12. Results of the pulsed laser test on the Micron 4G NAND. Red (dark) spots indicate the location of high current events, while light spots indicate locations where SEFIs without high current were observed. White rectangles indicate regions believed to be charge pumps.

In Fig. 13, we show the results of the Micro-RDC Milli-Beam™ experiment. In this test we collimated the beam so that only an area of 100 μm by 100 μm was exposed on each beam run. We used Xe ions at a fluence of 10^7 ions/cm^2 on each exposure. That is, we exposed the entire chip to a fluence of 10^7 Xe ions/cm^2 over the course of the entire run, but only a small portion of the die was exposed at one time. Locations of the numbers indicate the locations where SEFIs, requiring a DUT reset, or power cycle, or both, were observed. The numbers refer to the beam run on which the SEFI occurred. In all, there were 820 beam runs, and about 125 SEFIs in the entire run. The SEFI locations correlate very well with the locations where high currents or other SEFIs were observed in the laser test. The striking difference from the laser test, and also from the broad beam TAMU results, was that no current above 20 mA was observed at any point in the entire run. We will discuss the implications of this result later.

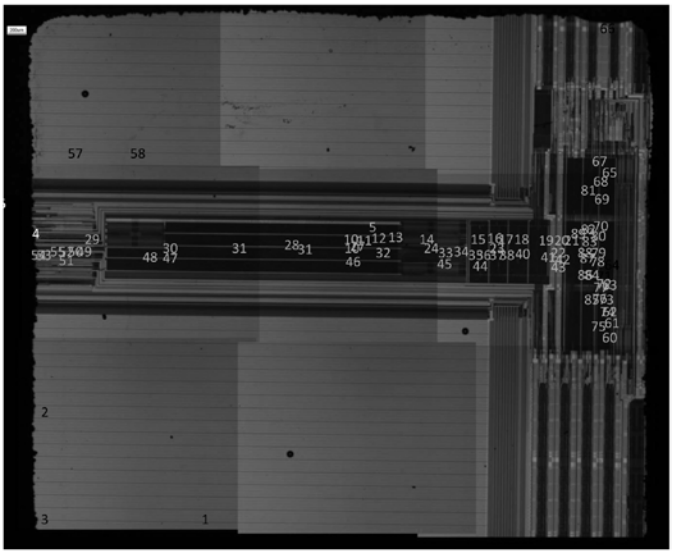

Fig. 13. Results of the Milli-Beam test. Locations of the number indicate where the Milli-Beam caused SEFIs; numbers refer to the beam run on which the SEFI was observed.

V. Discussion

None of the high current events match exactly those described in [1, 2]. Furthermore, Fig. 14 from Irom and Nguyen [1] shows a trace with ten such high current spikes in one run. When we tried to duplicate their results in Fig. 14, the closest agreement was shown in Figs. 3 and 4. That is, nine of the ten spikes were not observed at all, and one that was observed had a different pulse width. On most other runs, all ten spikes disappeared. Therefore, we believe the mechanism in our experiment was different than that observed in [1, 2].

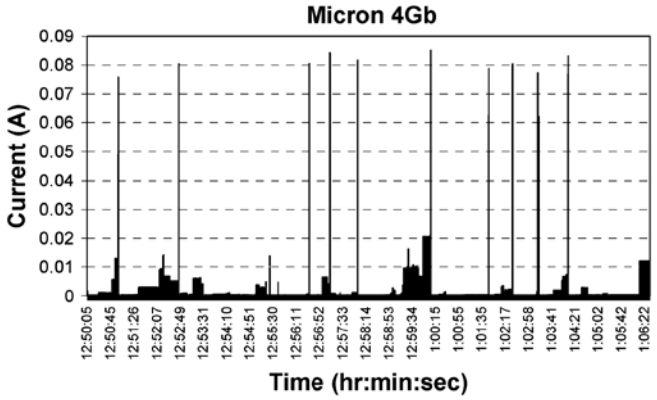

Fig. 14. Current spectrum for Micron Technology 4 Gb NAND flash. Data is taken with 181Ta ion at LET 77.3 MeV - cm^2/mg at the TAMU facility, figure from Irom and Nguyen [1].

We also note that the beam conditions used in [1] were 10^7 Ta ions/cm^2, with an LET of about 77 MeV/mg/cm^2. The flux at this LET in geosynchronous orbit is about one particle/cm^2 every 2000 years. Under present conditions, a fluence of 10^7 particles/cm^2 corresponds to an interval of $2x10^{10}$ years, which is greater than the age of the universe. In Fig. 14 from [1], there are ten current spikes, which means the mean time between events would be on the order of two billion years. Therefore, we conclude that even if we had duplicated the current spikes in a ground test, it would not make them a threat in space systems.

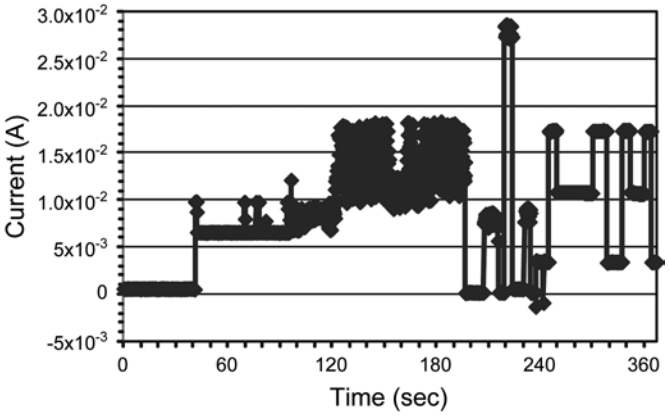

Fig. 15. Micron 4G, Xe ions, Dynamic Read/Erase/Write mode. DUT failed, losing the Erase function. Current versus time.

In [1, 2], it is asserted that the current spikes are destructive, implying that they cause functional failures. In Figs. 2 and 3, we have already shown two examples of high currents that were not destructive. In Fig. 15, we show an example where a Micron 4G, in R/E/W mode failed, losing the ability to Erase. But there was no current level higher than the normal Write current when the beam was on, so this failure is not associated with any high current. In Fig. 16, we show results for the Samsung 4G NAND, irradiated with Xe ions. The test mode is R/E/W, where the part is read, and, if an error is detected, the block is erased and rewritten. In Fig 15 (a), the part is reading (10 mA is the normal Read current), until errors are detected. The current then returns to nominal levels between the Read (10 mA), and the Write current, which is about 18 mA. In Fig. 16 (a), the ions were incident at high angle (45°), and no failure occurred—this current trace is an example of how the current should look. In Fig. 16 (b), on the other hand, the trace looks similar initially, but after Reading for a short time, the current increases to nearly 60 mA, and stays at nearly that level. Afterwards, the Write operation had failed, but normal current levels could be restored by telling the DUT to do something other than Write. In this case, the ions were normally incident, and similar failures were observed in a small fraction of the shots, but only if the ions were normally incident. The clear angular dependence is the signature of Single Event Gate Rupture (SEGR). Basically, the ion blows a hole in the gate oxide of a transistor, which creates a short circuit, and the short circuit causes high current. That is, the high current is the result of the oxide failure, and not the cause of it. There are examples, where high currents and functional failures are correlated, meaning they occur on the same shot. With all these counter-examples, where high currents do not cause functional failures, it is important to remember that correlation does not prove cause-and-effect. Functional failures in flash memory occur when the DUT can no longer Erase, or Write, which is usually assumed to be because the charge pump no longer puts out the voltage necessary for those operations. The results in Fig. 12 suggest the high currents do not come from the charge pump. Therefore, there is no clear evidence that the high currents actually cause functional failures, even when they are correlated.

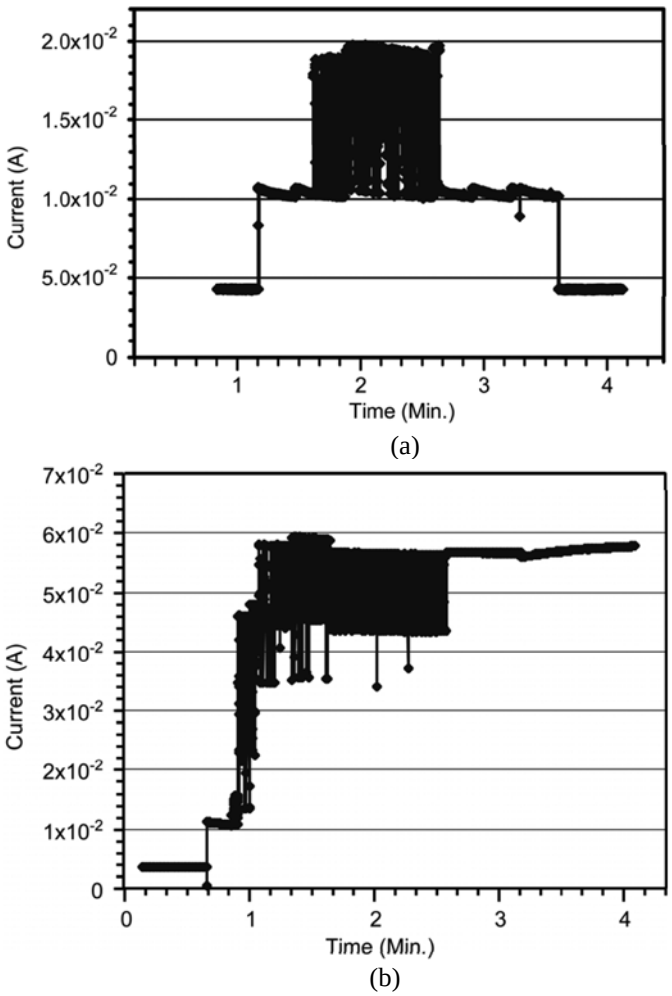

Fig. 16. Samsung 4G NAND irradiated with Xe ions in Read/Erase/Write mode: (a) 45 degree incidence, without failure; and (b) normal incidence with Write mode failure.

High current events, similar to what we observed in the TAMU experiments reported here, have been observed in a number of experiments by others [4, 11, 12]. None of these results were obtained on flash memories, which suggests that the effects reported here are not unique to flash memories. Shindou et al. [4] reported two kinds of high current events, one of which they call localized single event latchup (LSEL). An example is shown in Fig. 17, with the same stair-step

structure that we observed, and have shown in several examples. The other kind of high current event they called "Pseudo-SEL", and they attributed it to contention on the data signal lines. In [4], the authors were testing a test chip designed to check out a standard cell library, so they had every kind of combinational logic standard cell, but apparently, no charge pump. But the two kinds of high current events they discuss seem to account for all 52 of the high current events observed in our TAMU experiments.

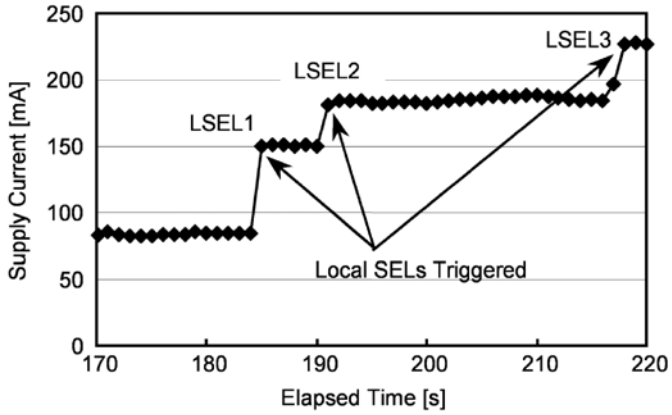

Fig.17. Stair-step increase in current, from LSEL current paths turning on, one after another, after Shindou et al. [4].

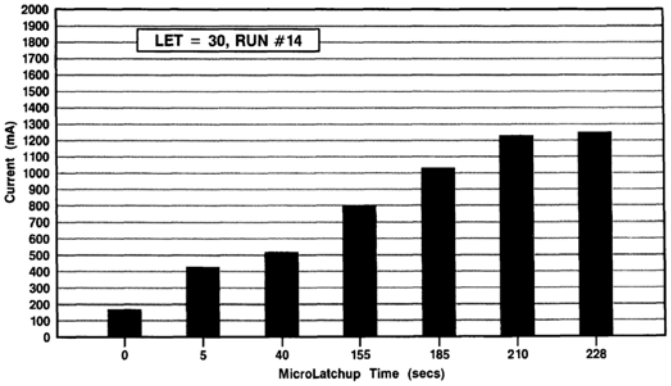

Fig. 18. Micro-latchups (or LSEL) observed in Intel 386 processor [5].

In Fig. 18, we show another example of stair-step current increases from LSELs in the Intel 80386 processor [11]. This paper was the very first paper ever published in the IEEE Radiation Effects Data Workshop, in 1992. Like Shindou et al [4], it was on a logic chip, with no charge pump. In Fig. 19, we show another example, on a Synchronous Dynamic Random Access Memory (SDRAM) [12]. Fig. 19 shows a series of clock pulses, but the baseline current increases in a stair-step manner from LSELs. SDRAMs, like flash memories, are complex circuits, with large amounts of combinational logic, embedded in the form of an on-chip controller. It appears that LSEL and bus contention can be expected in SEE testing of anything containing combinational logic. This means that the effects observed in our TAMU experiments are not unique to flash memories.

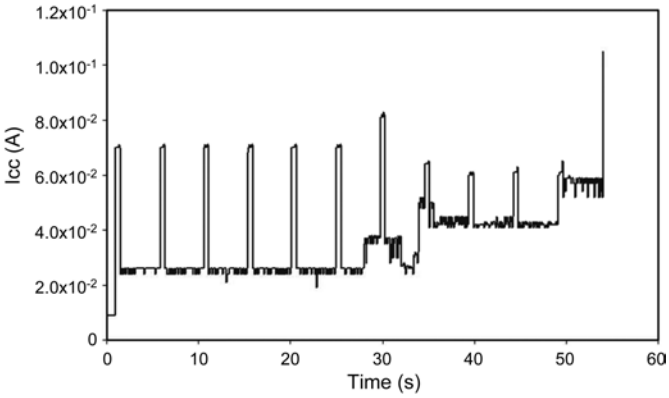

Fig. 19. Results from Poivey, et al. [6] in SEE testing of an SDRAM. Spikes here are clock pulses, but the baseline current increases in a stair-step manner from LSELs.

We noted that the results of the experiment with the Micro-RDC Milli-Beam correlated well with the NRL pulsed laser results, in the locations where SEFIs occurred, but not in the current values at those locations. In the laser test, we ran the beam at full power, to make sure we saw some effect. But equating laser power to effective LET is very difficult. We plan further testing where we will vary the laser power, and also the lens used to focus the beam. We expect that, with more careful control, the laser will come closer to matching the Milli-Beam results. The Milli-Beam results also call into question broad beam heavy ion results in [1, 2]. In those tests, the die was typically hit in about 10^4 location/sec, with results qualitatively far different than when the die was only hit in one location at a time. In space, the flux of ions is so low, the die will never be hit in more than one location at a time. The lesson is to be very wary of multiple particle strikes during ground testing and correlating to space applications.

VI. Conclusion

We attempted to replicate the current spike results in [1, 2], and did observe high current events, but the waveforms and pulse widths were generally much different. Only 4 of 52 events had a pulse width within 10x of that reported in [1, 2], but the frequency of occurrence is also much different. There were only four events that did not have rectangular waveforms in 38 shots in this experiment, and never more than one on a given shot. In [1], the authors observed ten spikes or more in one shot, multiple times. It is also true that the mechanisms described by Shindou et al. [4] were observed in combinational logic, but they seem to explain very nicely all 52 of our high current events. Similar things have also been observed in other kinds of circuits [11, 12], without charge pumps. Therefore, there is no reason to believe that the kinds of high current events reported here are unique to flash memories.

We have also presented laser test results and Milli-Beam test results, and compared them to broad beam heavy ion results. The differences have significant implications for future testing procedures.

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