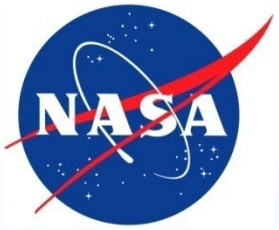
NEPP Electronic Technology Workshop
June 28-30, 2011

National Aeronautics
and Space Administration



Radiation Status of Sub-65 nm Electronics

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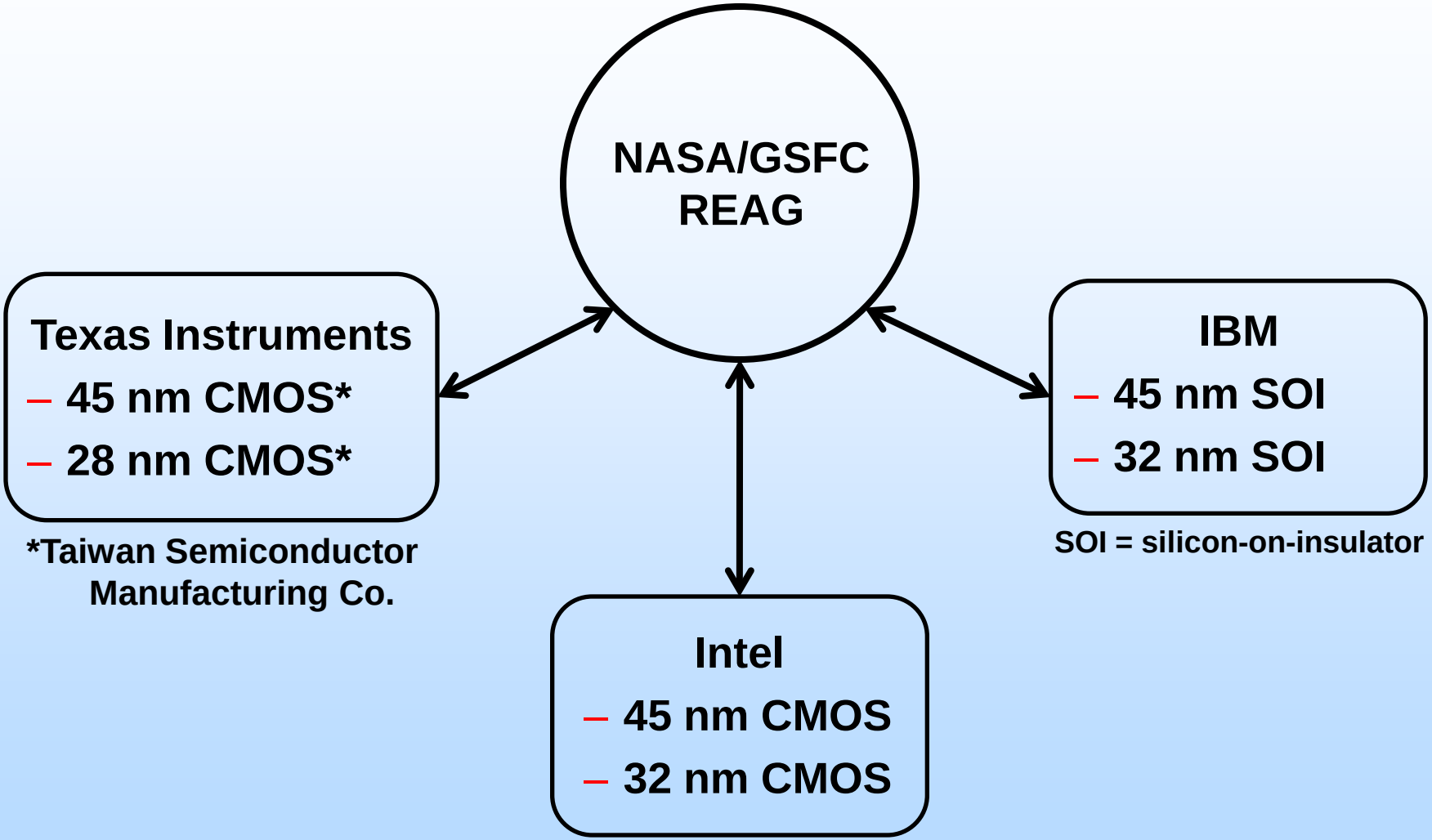
Introduction

- Ultra-scaled complementary metal oxide semiconductor (CMOS) includes commercial foundry capabilities at and below the 65 nm technology node
- Radiation evaluations take place using standard products and test characterization vehicles (memories, logic/latch chains, etc.)
- NEPP focus is two-fold:
  - Conduct early radiation evaluations to ascertain viability for future NASA missions – leverage commercial technology development
  - Uncover gaps in current testing methodologies and mechanism comprehension – early risk mitigation

Introduction

- **Large source of collaboration with external partners (not all ≤ 65 nm):**
  - **Corporate**
    - **Cypress Semiconductor**
    - **IBM Corporation (presented here)**
    - **Intel Corporation (presented here)**
    - **Texas Instruments (presented here)**
    - **TowerJazz**
    - **STMicroelectronics**
  - **Government**
    - **Naval Research Laboratory**
    - **Sandia National Laboratories**
  - **University**
    - **Vanderbilt University**
    - **The Georgia Institute of Technology**
    - **Auburn University**
    - **Arizona State University**

Introduction



Sub-65 nm CMOS

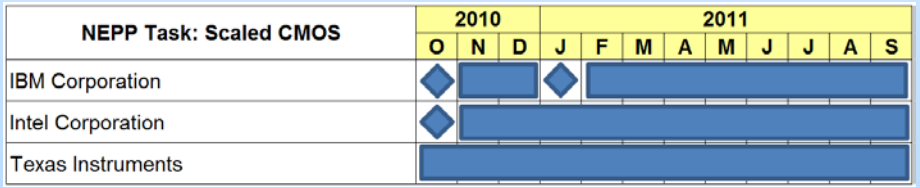
Description:

- Continue task to evaluate scaled CMOS technologies (< 65 nm) from IBM, Intel, and Texas Instruments,
- Determine inherent single-event effects (SEE) tolerance of Trusted Access Program Office (TAPO) product flows,
- Identify challenges for future SEE hardening efforts
- Investigate new SEE failure mechanisms and effects, and
- Provide data to NASA and DTRA modeling programs.
- Testing covers mostly non-destructive SEE using heavy ion and protons.
- Recent emphasis has been on low-energy proton soft errors induced by direct ionization.

FY11 Plans:

- IBM: continue analysis of FY10 45 nm SOI static random access memory (SRAM) data to assess role of proton direct ionization soft errors (both single and multi-bit); extend accelerated ground tests to 45 nm and 32 nm SOI latches; employ cold laser ablation and XeF_2 to yield advanced flip-chip sample preparation for low-energy protons and pulsed laser testing; extend studies to single-event transients pending test vehicle availability.
- Intel: continue FY10 evaluation of 45 and 32 nm test vehicles as available; make plans for evaluation of future technology nodes.
- TI: continue analysis of 45 nm data; support Vanderbilt efforts to gather single-event latchup (SEL) and exotic particle single-event upset (SEU) data; support modeling efforts; tapeout and complete test set design for 28 nm hardware.

Schedule:



- All tasks are currently ongoing
- Diamonds indicate completed or scheduled tests

Deliverables:

- Quarterly status reports to NEPP and DTRA
- Test reports
- Updates to lessons learned
- Presentations at leading technical conferences
- Publications in journals and NEPP website

Goals

- **IBM Corporation**
  - Gather first heavy ion and proton data sets on 32 nm SOI latches
  - Analyze low-energy proton data for latches and SRAM
  - Use low-energy proton data to develop a testing guideline
- **Intel Corporation**
  - Gather electron dose rate and gamma total ionizing dose data on 32 nm processors
  - Gather low-energy proton data on 45 and 32 nm test vehicles
- **Texas Instruments**
  - Continue investigation of layout dependence on heavy ion SEL in 45 nm CMOS
  - Support tapeout and subsequent testing of 28 nm test vehicles

Expected Impact to Community

- **Encourage early-adoption of advanced technologies**
  - **Promote technology development and leverage non-recurring engineering**
- **Identify new failure mechanisms**
  - **Reduce risk**
  - **Refine test methodologies and standards**
- **Strengthen existing and foster new relationships with industry**
  - **Maintain proactive (not reactive) stance for the radiation community**
- **Support Department of Defense foundry roadmaps for future rad-hard/tolerant devices**

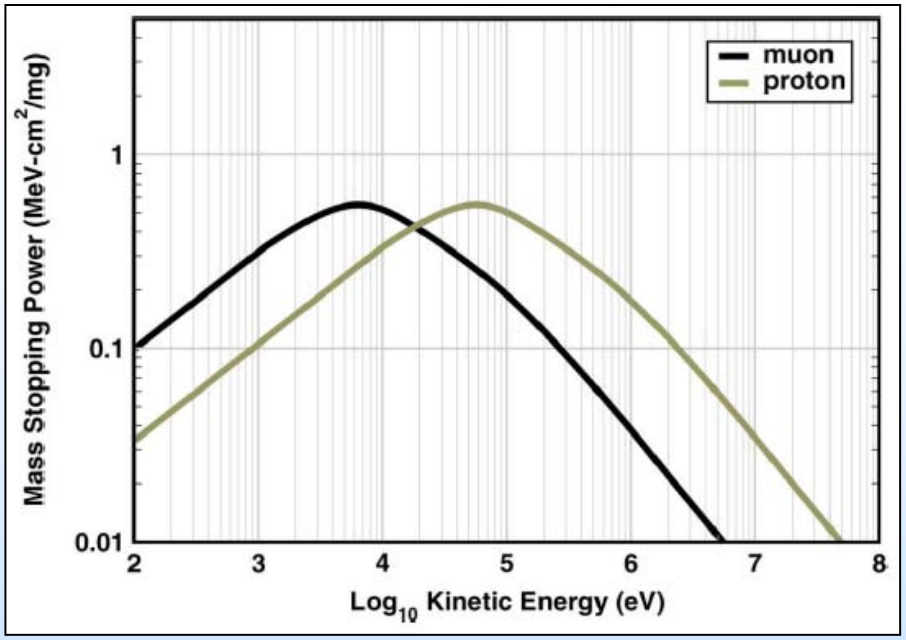
Status/Schedule

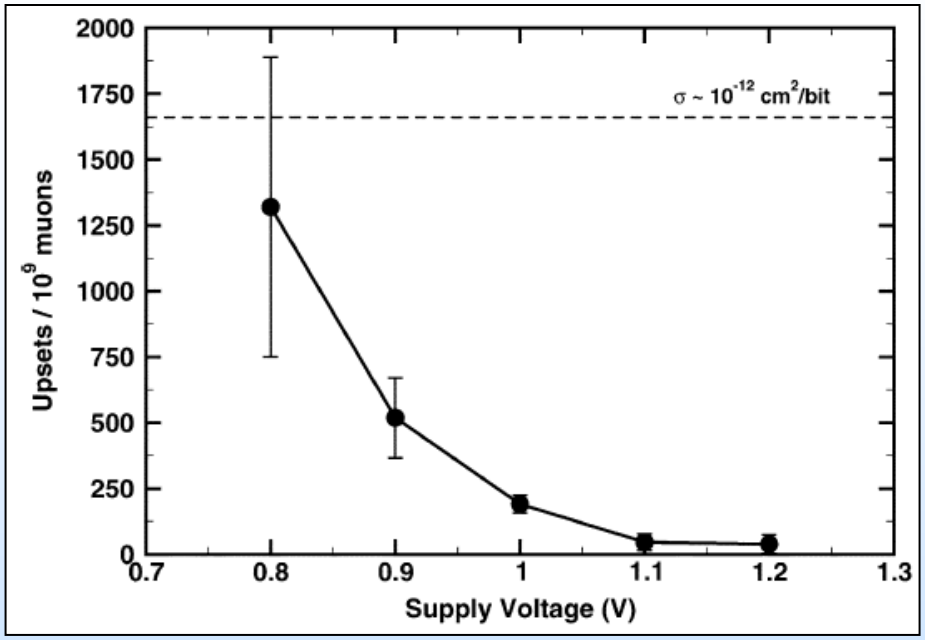
Acronyms Defined in Appendix if not Already Used

- **IBM Corporation**
  - Completed 32 nm SOI latch test set design
  - Completed initial 32 nm SOI latch heavy ion test (FY11 LBNL)
  - Completed initial 32 nm SOI low-energy proton test (FY11 UCD)
  - Completed additional low-energy proton and heavy ion testing of 45 nm SOI latches, including RHBD variant (FY11 UCD and LBNL)
- **Texas Instruments**
  - Supported additional SEL layout-dependence studies at the 45 nm node (FY11Q1-Q2)
  - Supported tapeout of 28 nm CMOS test vehicles (FY11Q3)
- **Intel Corporation**
  - Completed joint low-energy proton test of 32 and 45 nm CMOS test vehicles (FY11Q1 UCD)
  - Completed dose rate and total ionizing dose evaluation of 32 nm processor hardware (FY11Q2 NSWC/Crane & GSFC)
  - Continuing collaboration and look towards next technology node (FY11Q3-Q4, FY12)

Technical Highlights

65 nm Texas Instruments CMOS SRAM





B. D. Sierawski *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, Dec. 2011.

- **Muons shown to cause soft errors in 65 nm CMOS SRAM**
- **Simulations indicate no issue at nominal voltages for 65 and 45 nm technologies**

Potential implications for terrestrial SER in technologies below the 45 nm node – direct ionization, just like protons

SER = soft error rate

Technical Highlights

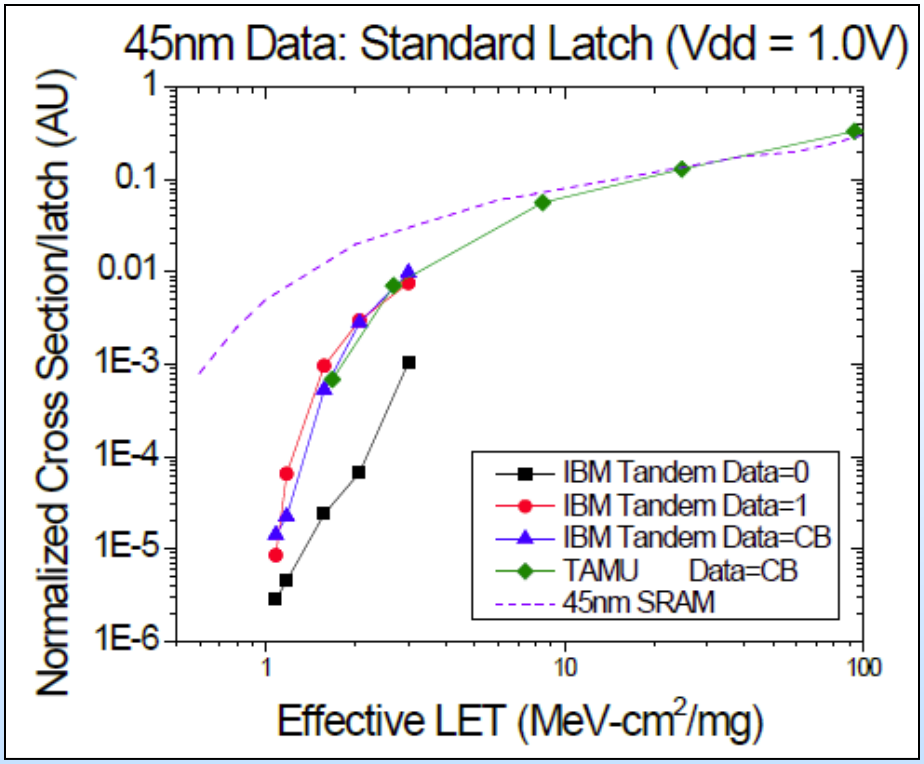
28 nm TSMC (via TI) CMOS

- Texas Instruments (TI) provided Vanderbilt University (VU) 20 “A” size modules on 28nm CMOS TSMC process
- Each “A” module is 151×833 *μ*m, twenty pads
- Vanderbilt team of four traveled to TI in Dallas April 3-11, 2011, to do layout with TI software
- All VU test modules will be relevant to understanding performance of advanced digital CMOS process in space
  - Heavy-ion testing for single event latchup
  - Characterization of two-photon laser beam area and intensity
  - Parasitic extraction for pulse capture of transistor currents from laser
  - Other modules related to space environment performance:
    - Transistor arrays for total dose characterization
    - Structures for measuring extent of potential collapse of n- and p-well
    - Latches designed to reduce vulnerability to well potential collapse
- Tape-out was late April, delivery estimated September 2011

Technical Highlights

45 nm IBM SOI CMOS Latches

- **Completed initial heavy ion characterization of 45 nm SOI latches**
  - **Size of latch stage and data pattern impact soft error cross section**
  - **Voltage dependence not shown**



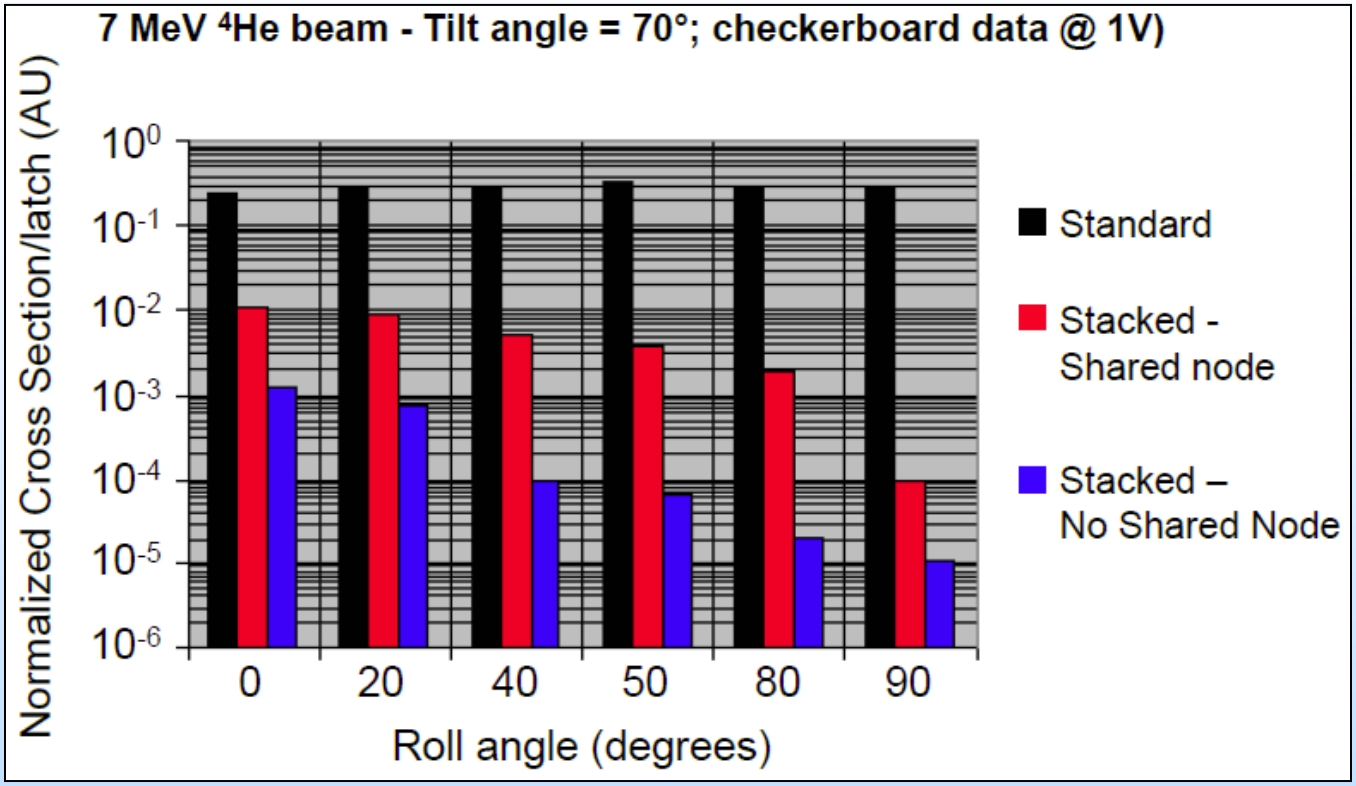
D. F. Heidel, *et al.*, *2011 Single-Event Effects Symposium*, La Jolla, CA.

LET = linear energy transfer

Confirmed sensitivity of 45 nm SOI latches relative to 45 nm SOI SRAM cells. What about the effects of roll and tilt angle?

Technical Highlights

45 nm IBM SOI CMOS Latches

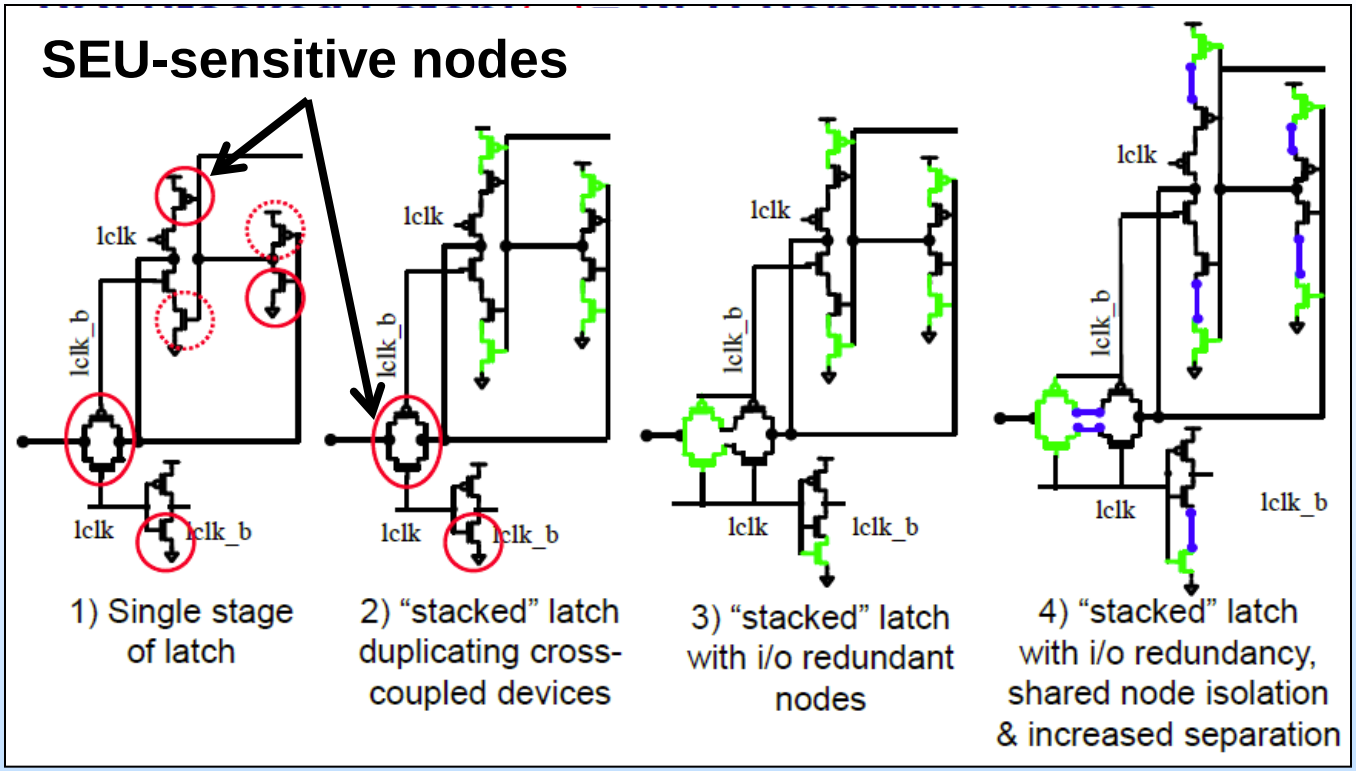


D. F. Heidel, *et al.*, *2011 Single-Event Effects Symposium*, La Jolla, CA.

Strong roll angle sensitivity to low-LET ion for radiation-tolerant designs suggests accelerated testing considerations
Highly dependent on nodal spacing

Technical Highlights

32 nm IBM SOI CMOS Latches



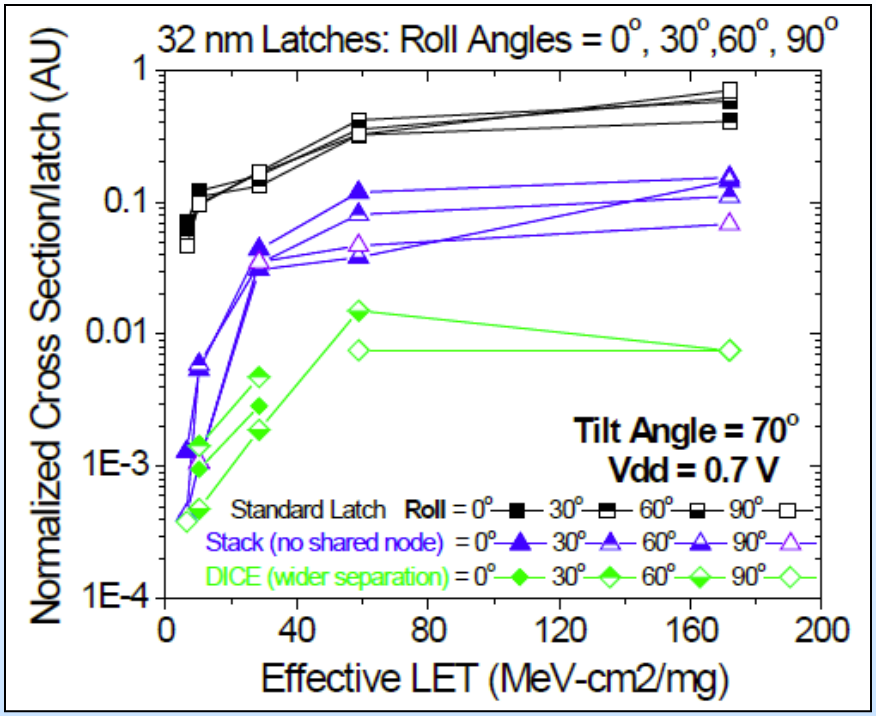
D. F. Heidel, *et al.*, *2011 Single-Event Effects Symposium*, La Jolla, CA.

Stacked latches increase SEU hardness with area penalties (similar to DICE latches) but lower power increase vs. DICE latches

DICE = dual-interlocked cell

Technical Highlights

32 nm IBM SOI CMOS Latches



Data at LBNL with a tilt of 70°

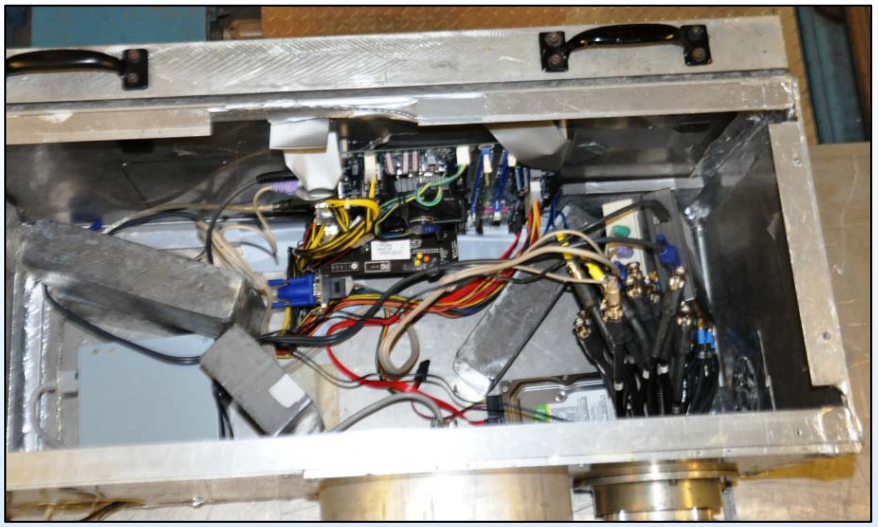
D. F. Heidel, *et al.*, *2011 Single-Event Effects Symposium*, La Jolla, CA.

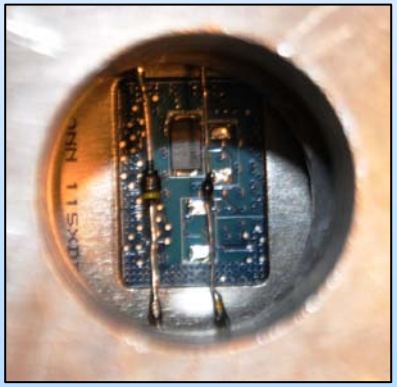
- **Redundant nodes increase SEU tolerance**
  - **Eliminate charge sharing and/or increase separation to increase tolerance**
- **Large tilt and roll angles can defeat hardening schemes; track radius effects become more significant for small geometries**

Technical Highlights

45 and 32 nm Intel CMOS

- Dual core i5 XEON microprocessor
  - Dose rate
  - Total ionizing dose
- 32 and 45 nm latch test structures
  - Low-energy proton testing
- Results from low-energy proton testing presented at 2011 Nuclear and Space Radiation Effects Conference



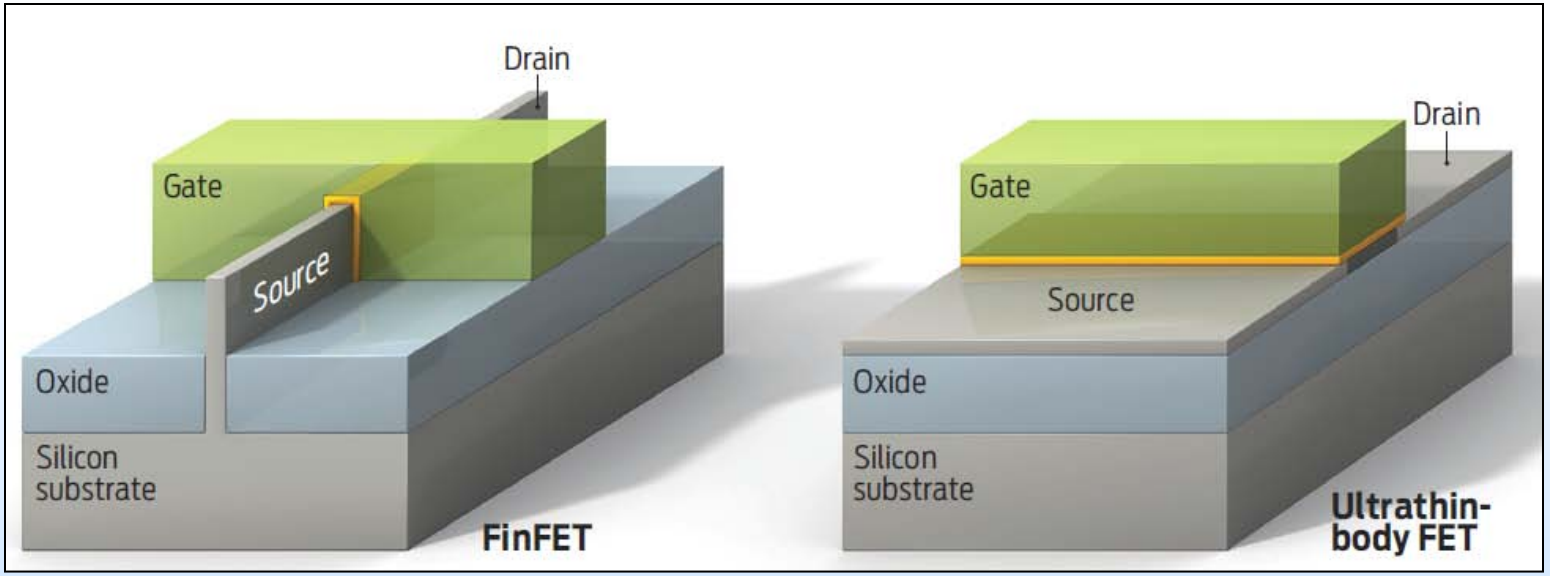


- Radiation shield/collimator
- P-i-N diodes used for dosimetry are positioned behind the device under test

Ongoing collaboration working towards evaluating the next technology node (22 nm CMOS).

Technical Highlights

22 nm Intel CMOS



"Transistors go 3-D," *IEEE Spectrum*, vol. 48, no. 6, pp. 12-12, 2011.

- Intel announced in May 2011 that they are going to FinFETs ("tri-gate") devices at 22 nm
- Processors with FinFETs roll out later this year according to IEEE Spectrum article

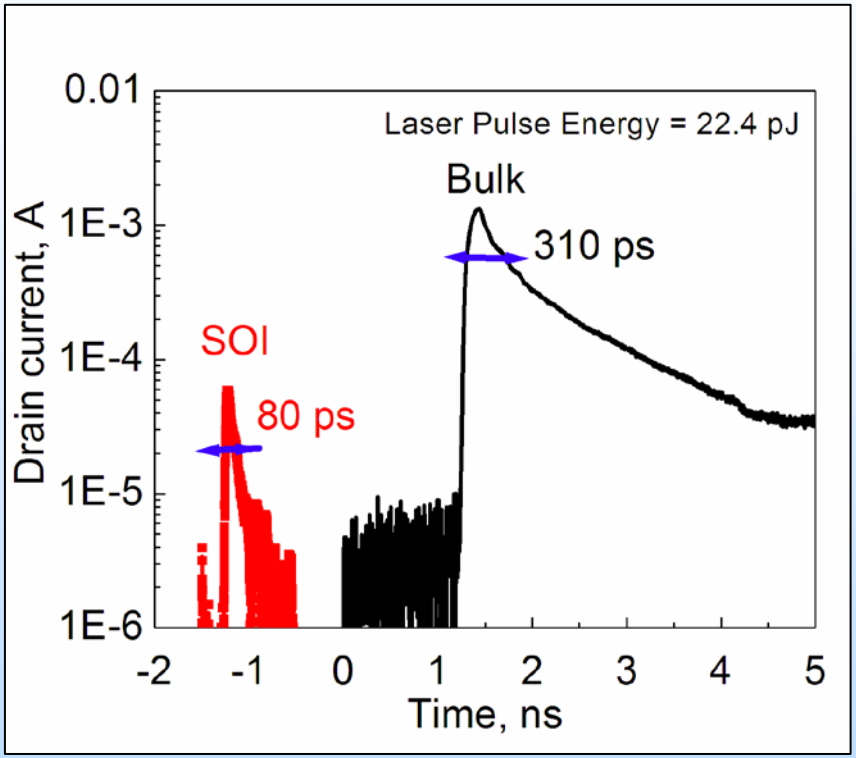
What are the implications for radiation effects on FinFETs with ultra large scale integration processor designs?

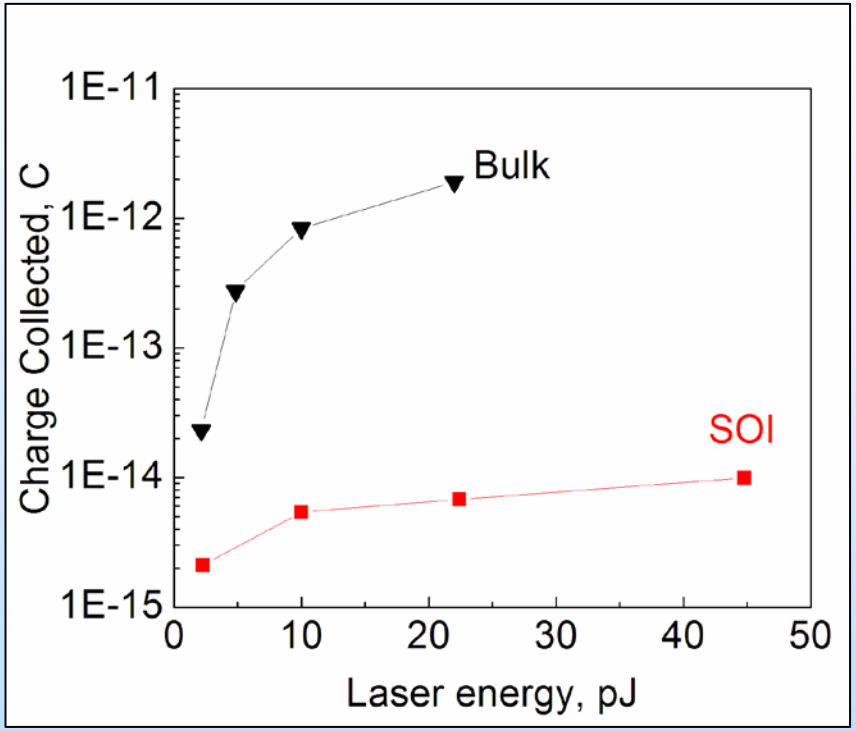
FinFET = fin field effect transistor

Technical Highlights

Bulk vs. SOI FinFET Pulsed Laser Data

Vanderbilt University





F. El-Mamouni, *et al.*, *2011 Int. Reliability Phys. Symp.*

SOI FinFETs may be more advantageous than their bulk counterparts due to isolating effects of the buried oxide

FY11 Publications

Selection of Well Contact Densities for Latchup-Immune Minimal-Area ICs

N. A. Dodds, J. M. Hutson, J. A. Pellish, R. A. Reed, H. S. Kim, M. D. Berg, M. R. Friendlich, A. M. Phan, C. M. Seidleck, M. A. Xapsos, X. Deng, R. C. Baumann, R. D. Schrimpf, M. P. King, L. W. Massengill, and R. A. Weller

IC = integrated circuit

Impact of Spacecraft Shielding on Direct Ionization Soft Error Rates for Sub-130 nm Technologies

Jonathan A. Pellish, *Member, IEEE*, Michael A. Xapsos, *Senior Member, IEEE*, Craig A. Stauffer, Thomas M. Jordan, *Member, IEEE*, Anthony B. Sanders, *Member, IEEE*, Raymond L. Ladbury, *Member, IEEE*, Timothy R. Oldham, *Fellow, IEEE*, Paul W. Marshall, *Member, IEEE*, David F. Heidel, *Senior Member, IEEE*, and Kenneth P. Rodbell, *Senior Member, IEEE*

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010

- **Layout guidelines for SEL immunity in scaled CMOS**
- **3-D ray trace/reverse Monte Carlo techniques for rate calculations**
  - **Includes work on low-energy protons for SRAM and NAND flash**

FY11 Publications

Muon-Induced Single Event Upsets in Deep-Submicron Technology

Brian D. Sierawski, *Member, IEEE*, Marcus H. Mendenhall, *Member, IEEE*, Robert A. Reed, *Senior Member, IEEE*, Michael A. Clemens, *Student Member, IEEE*, Robert A. Weller, *Senior Member, IEEE*, Ronald D. Schrimpf, *Fellow, IEEE*, Ewart W. Blackmore, *Member, IEEE*, Michael Trinczek, *Member, IEEE*, Bassam Hitti, Jonathan A. Pellish, *Member, IEEE*, Robert C. Baumann, *Fellow, IEEE*, Shi-Jie Wen, Rick Wong, and Nelson Tam

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010

- **1st experimental evidence that 65, 45, and 40 nm bulk CMOS SRAMs are susceptible to muon direct ionization – implications for ground-based systems as scaling continues**

FY11 Presentations

- F. El-Mamouni, *et al.*, "Pulsed laser-induced transient currents in bulk and silicon-on-insulator FinFETs," in *2011 Int. Reliability Physics Symp*., Monterey, CA.
- B. D. Sierawski, *et al.*, "Effects of scaling on muon-induced soft errors," in *2011 Int. Reliability Physics Symp*., Monterey, CA.
- J. R. Schwank, et al., "Comparison of single and two-photon absorption for laser characterization of single-event upsets in SOI SRAMs," to be presented at the *2011 IEEE Nuclear Space Radiation Effects Conf.*, Las Vegas, NV.
- J. A. Pellish, *et al.*, "Low-energy proton testing using cyclotron sources," to be presented at the *2011 IEEE Nuclear Space Radiation Effects Conf.*, Las Vegas, NV.

FY11 Presentations

- **K. P. Rodbell, et al., "32 and 45 nm Radiation Hardened by Design (RHBD) SOI Latches," to be presented at the *2011 IEEE Nuclear Space Radiation Effects Conf.*, Las Vegas, NV.**

- **N. Seifert, et al., "On the Susceptibility of Latches to Low-Energy Protons," to be presented at the *2011 IEEE Nuclear Space Radiation Effects Conf.*, Las Vegas, NV.**

Plans (FY11/FY12)

Acronyms Defined in Appendix if not Already Used

- **IBM Corp.**
  - **Continue 45 and 32 nm SOI SRAM and latch data analysis (FY11Q3-Q4, FY12)**
  - **Prepare test sets and experimental designs for 32 nm SOI transient measurement test vehicle (FY11Q3-Q4); commence testing in FY12**
- **Intel Corp.**
  - **Continue collaboration and make plans to evaluate additional processor hardware, test vehicles, and the next technology node**
- **Texas Instruments**
  - **Continue to support analysis of TAMU and LBNL SEL data on 45 nm CMOS test vehicles (FY11Q3-Q4)**
  - **Support additional testing and modeling efforts for 28 nm CMOS test vehicles (FY11Q3-Q4, FY12)**

Additional Acronym Definitions

- FY = fiscal year
- LBNL = Lawrence Berkeley National Laboratory
- NAND = “Not AND”
- NSWC/Crane = Naval Surface Warfare Center – Crane Division
- SEE = single-event effect
- SEL = single-event latchup
- SEU = single-event upset
- TAMU = Texas A&M University
- TI = Texas Instruments
- TSMC = Taiwan Semiconductor Manufacturing Co.
- UCD = University of California at Davis
- VU = Vanderbilt University