

# CHARACTERIZATION OF AN AUTONOMOUS NON-VOLATILE FERROELECTRIC MEMORY LATCH

**Caroline S. John<sup>1</sup>, Todd C. MacLeod<sup>2</sup>, Joe Evans<sup>2</sup> and Fat D. Ho<sup>1</sup>**

<sup>1</sup>The University of Alabama in Huntsville, Department of Electrical and Computer Engineering,  
Huntsville, Alabama, 35899, USA

<sup>2</sup>National Aeronautics and Space Administration, Marshall Space Flight Center, Huntsville,  
Alabama, 35812, USA

<sup>2</sup>Radiant Technologies Inc., Albuquerque, New Mexico, 87107, USA

## ABSTRACT

Non-volatile memory forms an integral part of computer systems and its applications. Non-volatile memory using ferroelectric components is more desirable over the other available memories due to its high endurance and high speed writing. The properties of the material to store an electric polarization in the absence of an electric field make the device non-volatile. In this paper we present an autonomous non-volatile ferroelectric memory latch using the principle that when an electric field is applied to a ferroelectric capacitor, the positive and negative remnant polarization charge states of the capacitor are denoted as either data '0' or data '1'. The latch holds the new data as long as power is applied and returns automatically to that state when the power is removed and reapplied ensuring non-volatility. Further the memory latch is autonomous as it operates with the ground, power and output node connections only. The unique quality of this latch circuit is that it can be written when powered off. The circuit was laid out using discrete components which was used to characterize the design. This paper analyses the electrical characterization and the data retention of the circuit.

**Keywords:** Ferroelectric capacitor; non-volatile; autonomous; memory latch

**Topic:** Non-Volatile Memories  
**Presenting Author:** Caroline S. John  
**Affiliation:** The University of Alabama in Huntsville  
**Email:** carolinesangeetha@gmail.com  
**Type:** Poster Presentation



CAROLINE S. JOHN<sup>1</sup>, TODD C. MACLEOD<sup>2</sup>, JOE EVANS<sup>2</sup> and FAT D. HO<sup>1</sup>

<sup>2</sup>National Aeronautics and Space Administration, Marshall Space Flight Center, Huntsville, Alabama, 35812, U.S.A.

<sup>2</sup>The Radiant Technologies Inc., Albuquerque, New Mexico, 87107, U.S.A.



We present the electrical characterization of an autonomous non-volatile ferroelectric memory latch using the principle that when an electric field is applied to a ferroelectric capacitor, the positive and negative remnant polarization charge states of the capacitor are denoted as either data '0' or data '1'. The properties of the ferroelectric material to store an electric polarization in the absence of an electric field make the device non-volatile. Further the memory latch is autonomous as it operates with the ground, power and output node connections, without any externally clocked control line. The unique quality of this latch circuit is that it can be written when powered off. The advantages of this latch over flash memories are: a) It offers unlimited reads/writes b) Works on symmetrical read/write cycles. C) The latch is asynchronous. The circuit was initially developed by Radiant Technologies Inc., Albuquerque, New Mexico.

Figure 1: Ferroelectric memory latch circuit

The NPN transistor acts as the data switch and PNP transistor is the feedback switch. The drop across the diode formed by the PNP base circuit provides the detection threshold necessary for the feedback switch to delay its activation. A Sawyer tower circuit is constructed at the base of the transistors. The sense capacitor collects charge from the ferroelectric capacitor  $C_{data}$  such that the voltage at the base of T1 is

$$V_{\text{base}} = Q_{\text{fe}} * C_{\text{sense}}.$$

The numerical value of  $C_{\text{sense}}$  is determined by how much charge is present in the ferroelectric capacitor  $C_{\text{data}}$ .

## Switching Capacitance of the Ferroelectric Capacitor<sup>[1]</sup>

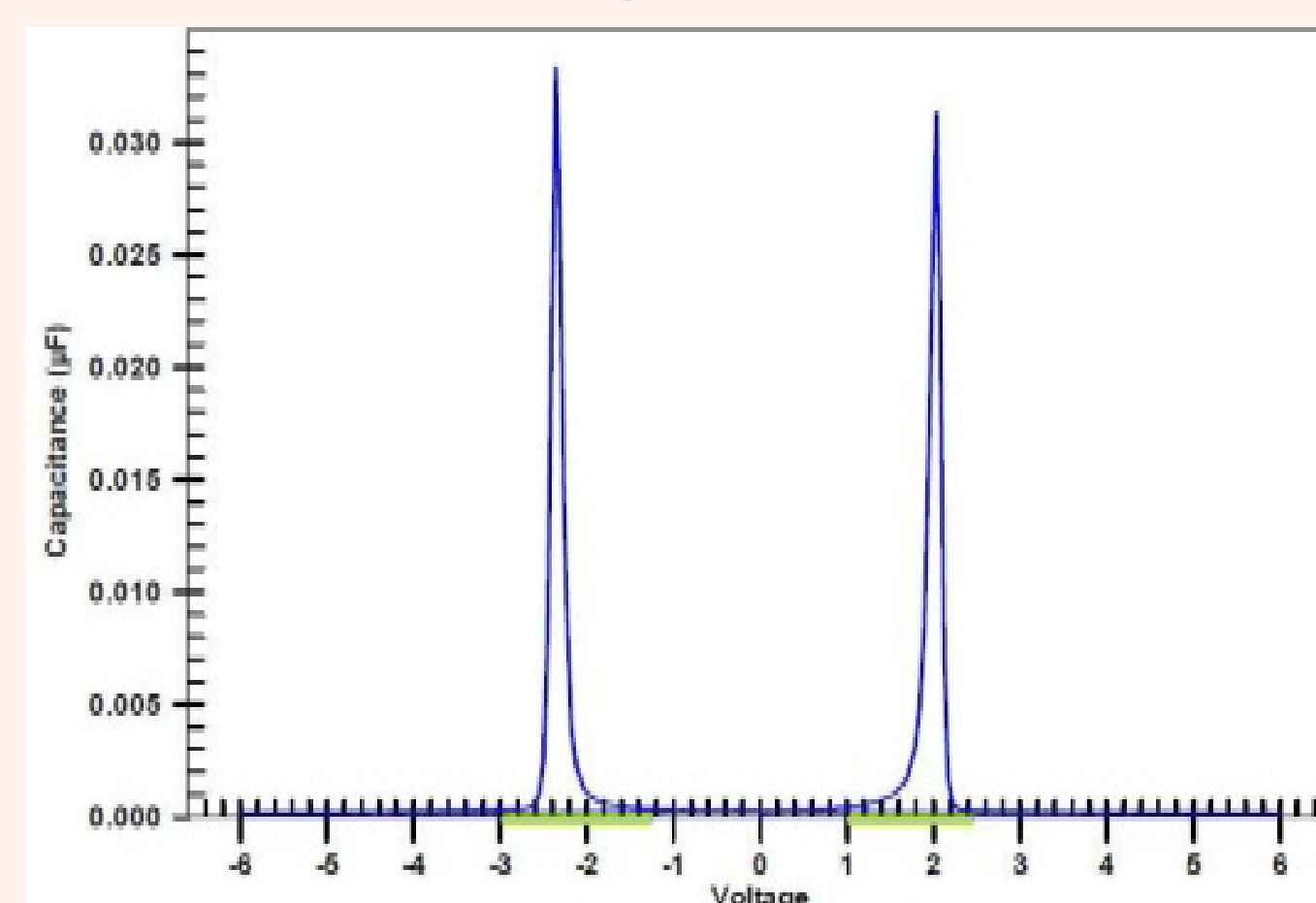


Figure 2: Instantaneous capacitance Vs voltage of the ferroelectric capacitance

The ferroelectric capacitance used is of type AB White from Radiant Technologies Inc. These capacitors possess an area of 0.0001 square centimeters and 2600 Å of 20/80 PZT between platinum electrodes.

The graph shows the capacitance switching in and around +2V and -2V of applied voltage for the ferroelectric capacitance.

## References

1. Comparison of remnant Polarization, IV and small signal CV for a PZT capacitor, Radiant Technologies Inc., ISAF- ECAPD '10
2. Design of a ferroelectric programmable logic gate array ,T. Macleod & F.D Ho, Integrated Ferroelectrics Volume 56,pp.1013-1021,'03.
3. An Autonomous nonvolatile memory Latch, J.T Evans, Radiant Technologies Inc., [www.ferrodevices.com/1/297](http://www.ferrodevices.com/1/297).

## Read / Write Operation

A '0' or one '1' can be written onto the latch by first ramping the voltage at the power supply node to 2Vpp. This causes a switch in the ferroelectric capacitance as shown in Fig:2. The power supply is now turned off and a 2v signal is applied at the input node which causes the state of the data stored in the latch to be reversed. Thus a '1' is written to the latch if its previous state was '0' and vice versa. The written data is indicated by the red line in the images below.

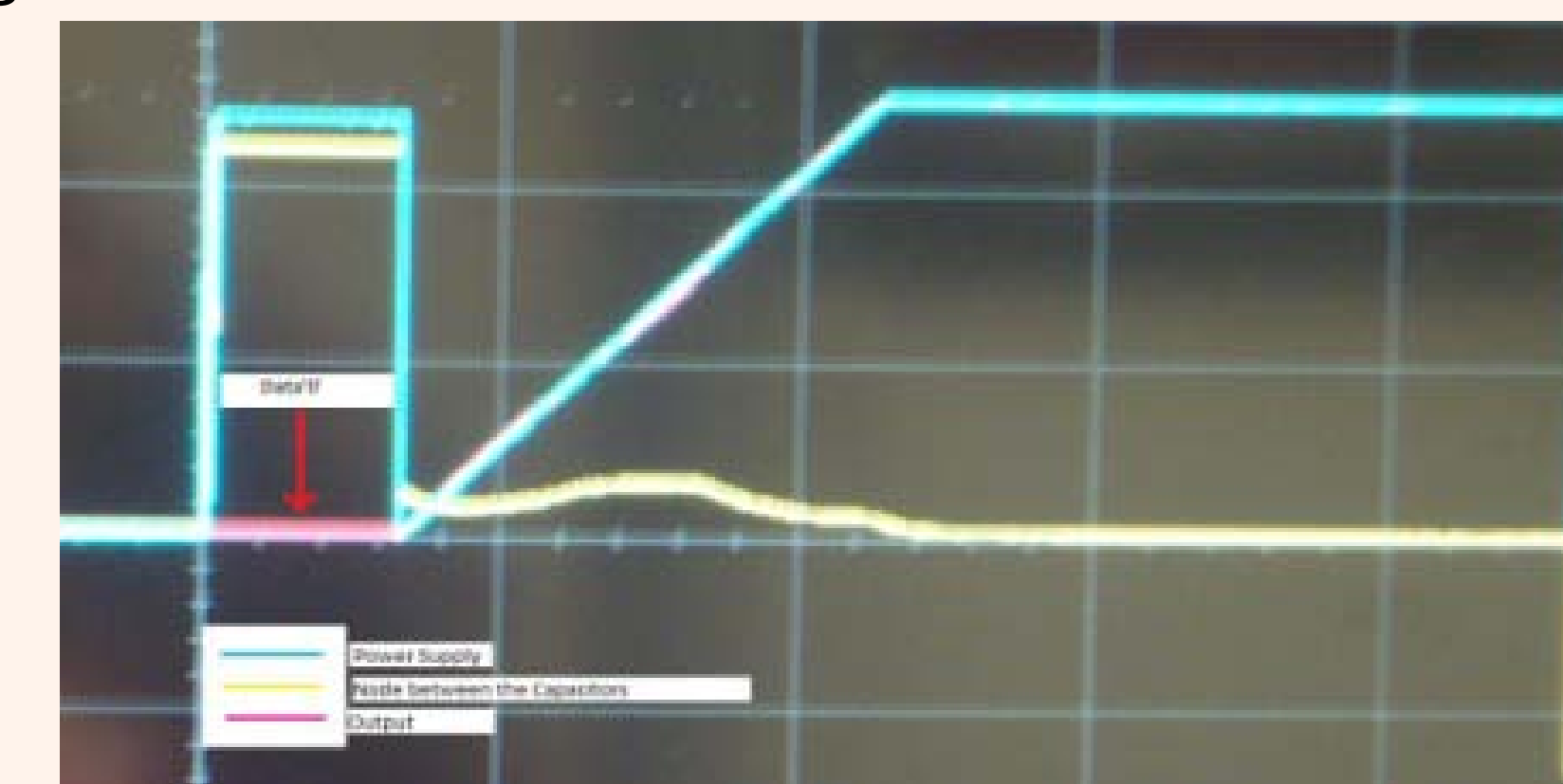


Figure 3: Writing a '0' to the latch

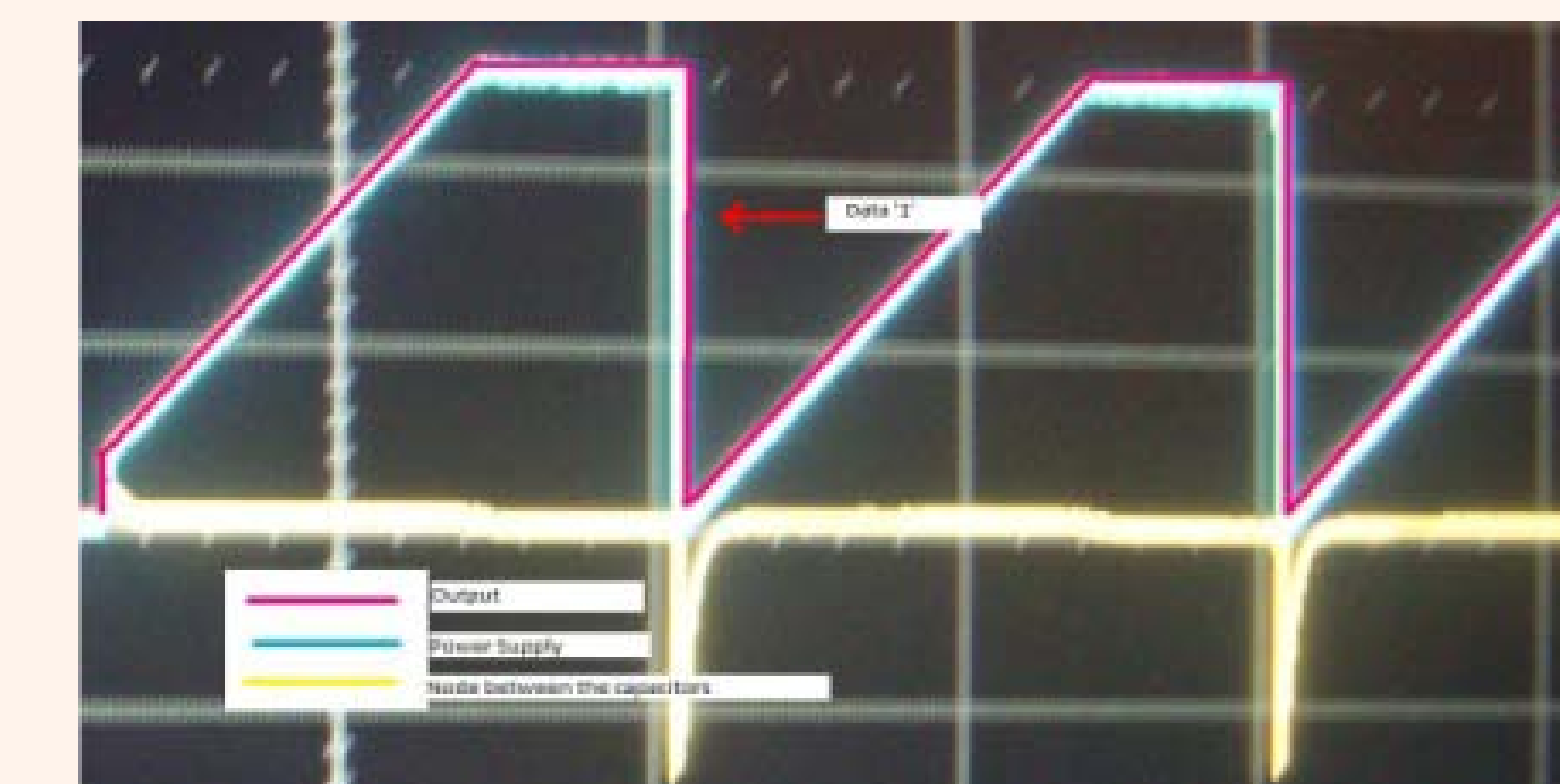


Figure 4: Writing a '1' to the latch

In order to read from the latch, the Ferroelectric Capacitance is switched by ramping the the voltage at the power supply node to 2Vpp and then switched off. The data stored on the latch is read by then ramping the power supply voltage to 5Vpp. The data that is read is indicated by the red line in the images below.



Figure 5: Reading a '0' from the latch

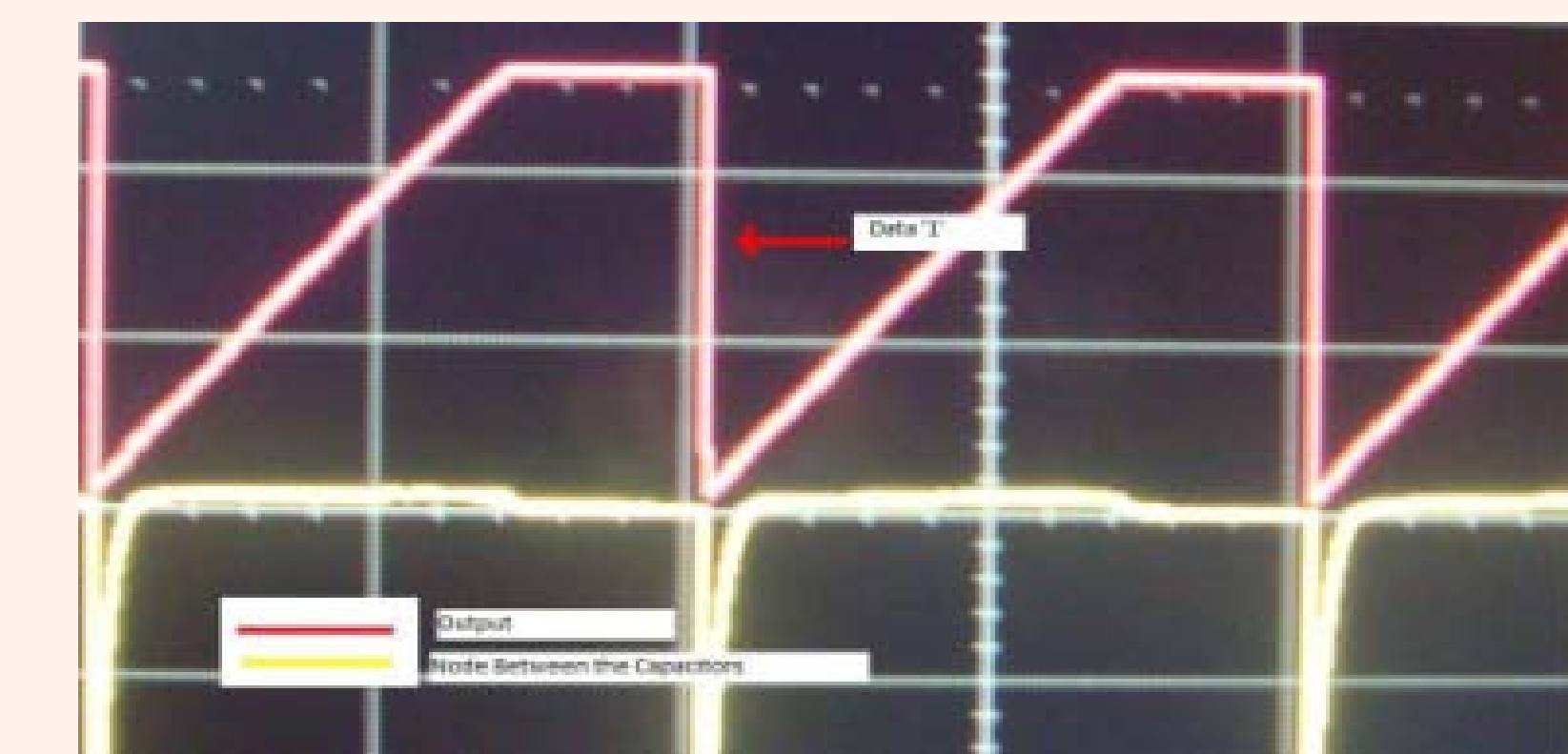


Figure 6: Reading a '1' from the latch

## Power Supply

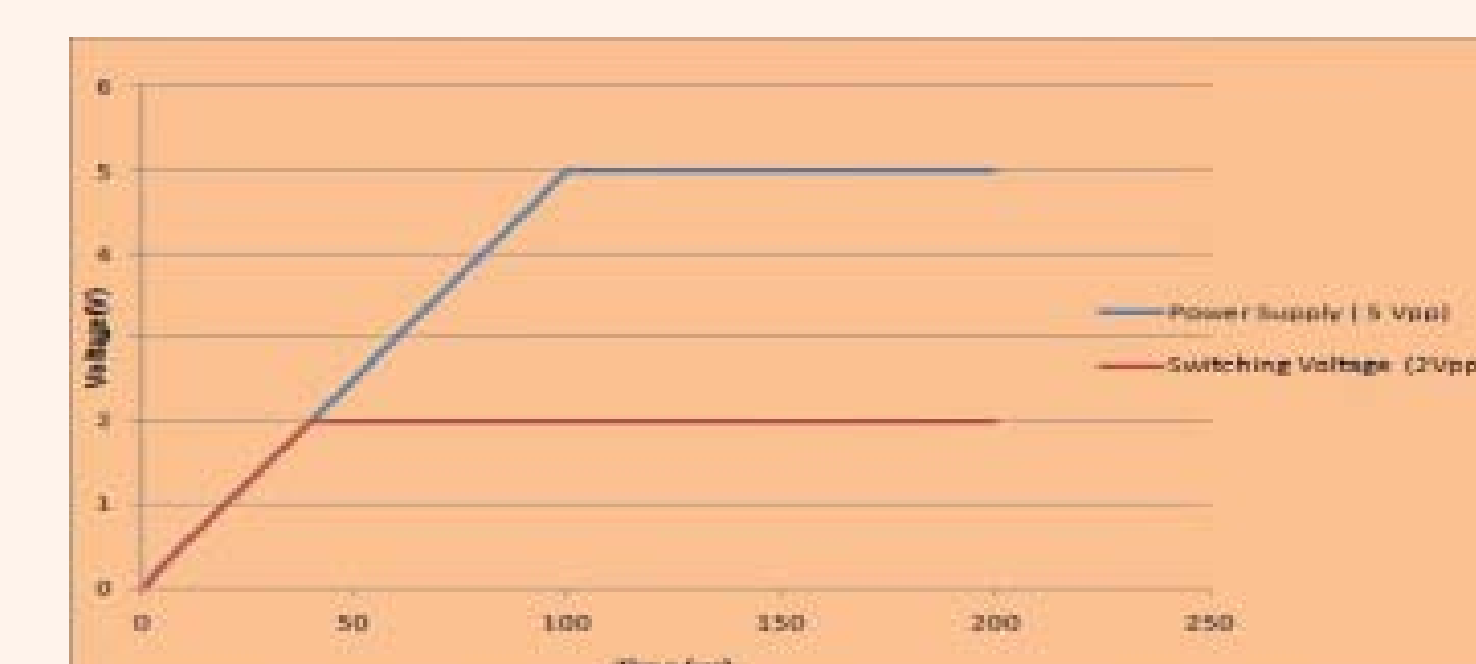


Figure 6: Voltage variations at the power supply node.

The key aspect during the read or write operation of this latch is to be able to switch the ferroelectric capacitance. This is done by changing the voltage at the power supply node as shown in Fig: 6.

## Applications

The applications of the studied memory latch may include:

- State Machine.
- Automotive and Aerospace Applications.
- Asynchronous Memory.
- FPGA configuration control.

## Conclusions

Initial characterization of the autonomous memory latch circuit were made. The circuit successfully stored data that could be set and reset. This circuit was also able to retrieve data even after power was removed.