MODELING OF SONOS MEMORY CELL ERASE CYCLE

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INTRODUCTION

- Utilization of Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile semiconductor memories as a flash memory has many advantages.
- These electrically erasable programmable read-only memories (EEPROMs) utilize low programming voltages, have a high erase/write cycle lifetime, are radiation hardened, and are compatible with high-density scaled CMOS for low power, portable electronics.
- In this paper, the SONOS memory cell erase cycle was investigated using a nonquasi-static (NQS) MOSFET model.
- Comparisons were made between the model predictions and experimental data.

SONOS Device

- The modeled SONOS device is shown in Figure 1.

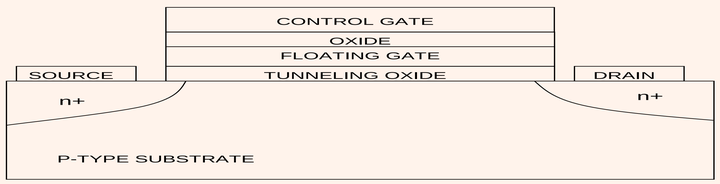

Figure 1: SONOS Device Layout

- SONOS device parameters
  - Tunneling oxide thickness (t_{oxtun}) – 6nm
  - Floating gate thickness – 6nm
  - Oxide thickness (t_{ox}) – 7nm
  - Channel length (l) – 0.35μm
  - Device width (w) – 0.25μm
  - Gate length (l')
  - Gate overlap over Drain/Source (x_j)
- Calculated Capacitances
  - $C_{oxg}= (\varepsilon_{ox}/t_{ox})\ w\ l'$
  - $C_{oxtun}= (\varepsilon_{ox}/t_{oxtun})\ A_{tun}$
  - $C_{oxgd}= (\varepsilon_{ox}/t_{oxtun})\ w\ x_j$
  - $C_{oxgs}= (\varepsilon_{ox}/t_{oxtun})\ w\ x_j$
  - $C_{total}= C_{oxg}+ C_{oxtun}+ C_{oxgd}+ C_{oxgs}$
  - $l' = l + 2x_j$
  - $A_{tun}= w\ l$

ERASE MODEL DEVELOPMENT

- Applying Gauss' Law to the floating gate provides

  $Q_{FG} = C_{oxg} (V_{FG} – V_{GB}) + C_{oxtun} (V_{FG}-\phi_S-\phi_{MS}) + C_{oxgs}(V_{FG}-V_{SB}) + C_{oxgs}(V_{FG}-V_{DB})$ (1)
- During Erase cycle device is in accumulation mode
  - ϕ_S should be on the order of a few hundredths of a volt and can be neglected
- Taking the time derivative of equation 1, and realizing that $dQ_{FG}/dt = -I_{tun}$ leads to

  $dQ_{FG}/dt = -I_{tun}=C_{total}(dV_{FG}/dt) - C_{oxg}(dV_{GB}/dt)$ (2)
- Rearranging equation 2 to solve for the floating gate voltage provides

  $(dV_{FG}/dt)=[C_{oxg}(dV_{GB}/dt) - I_{tun}]/C_{total}$ (3)
- Equation 3 can be solved for the floating gate voltage by numerical methods.
- Now the tunneling Electric Field can be calculated.

  $E_{tun}=(V_{FG}- \phi_S)/t_{oxtun}$ (4)
- Then the tunnel current can be calculated using the Fowler-Nordheim equation

  $I_{tun}=\alpha_{Fnerase} A_{tun} E^2_{tun} \exp(-\beta_{Fnerase}/E_{tun})$ $E_{tun} > 0$ (5.1)

  $I_{tun}=-\alpha_{Fnerase} A_{tun} E^2_{tun} \exp(-\beta_{Fnerase}/|E_{tun}|)$ $E_{tun} < 0$ (5.2)

  $I_{tun}= 0$ $E_{tun} = 0$ (5.3)
- Fowler-Nordheim constants

  $\alpha_{Fnerase}$ = 1.23e-6

  $\beta_{Fnerase}$ = 2.37e+8
- Now an updated value for the floating gate charge can be obtained from

  $dQ_{FG}/dt = -I_{tun}$
- Finally an updated value for the threshold voltage can be calculated using

  $V_{th}= V_{th0} - (Q_{FG}/C_{oxg})$ (7)
- A software flowchart is shown in Figure 2.
- A logarithmic series was implemented for time steps t.
- Each of the equations was solved for each time step.

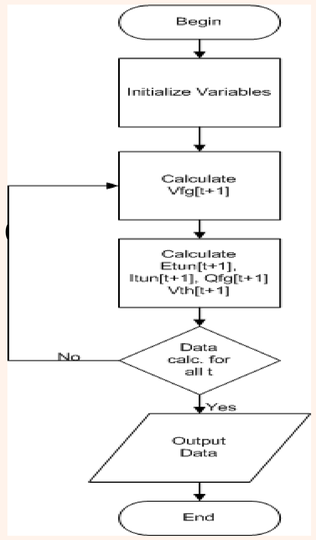

Figure 2: Software Flowchart

RESULTS

- For the SONOS erase operation V_{GB} was set to -8 VDC, V_{DB} and V_{SB} were set to 0 VDC.
- The calculated floating gate voltage is shown in Figure 3.

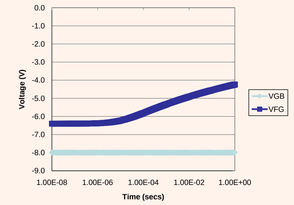

Figure 3: Gate Voltages

- The calculated tunnel current is shown in Figure 4. The calculated threshold voltage and the threshold voltage from the Cho & Kim device is shown in Figure 5.

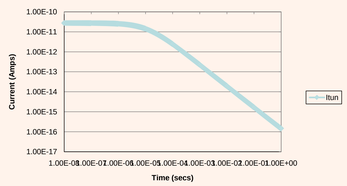

Figure 4: Tunnel Current

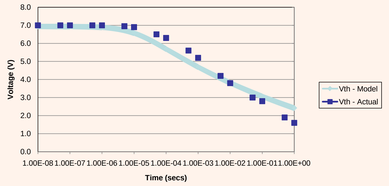

Figure 5: Threshold Voltage

CONCLUSION

- A nonquasi-static model was developed for the SONOS memory cell erase cycle.
- The floating gate voltage, tunnel current, and threshold voltages were calculated based on the SONOS device parameters.
- The calculated threshold voltage curve had a slightly different slope than the threshold voltage curve from the Cho & Kim device, but there was still fairly good agreement between the two curves.

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