entire image from the CCD, pixel by pixel. The exposure time must be long enough to obtain adequate signal-to-noise ratios in the code-bit marks. The requirement for pixel-by-pixel readout of the entire image arises from the use of vertical (as well as horizontal) position information to distinguish among code-bit marks in different rows.

In conventional pixel-by-pixel readout, during each row-readout clock cycle, the signal contents of all the pixels of each row are shifted down to the next row, except that the contents of the bottom row are shifted down to a serial register, which triggers analog-to-digital conversion of each pixel's signal. Then, before the beginning of the next row-readout clock cycle, the contents of the serial register are shifted out, one pixel at a time, in response to sequence of column-readout pulses.

In vertically binned readout, which is an established alternative to conventional pixel-by-pixel readout, the sequence of clock pulses is modified so that the contents of multiple rows are shifted down to the serial register before applying the column-readout pulses. As a result, vertical resolution is lost, but time needed for reading out the image charge from all the pixels is reduced by a factor equal to the number of rows shifted prior to shifting the column contents out of the serial register. Moreover, the image-data processes needed to extract the vertical spatial information to determine row locations of code-bit marks can be eliminated. Inasmuch as the consequent loss of vertical resolution does not adversely affect the desired measurement of horizontal position, vertical binning can thus be used to reduce readout time substantially, provided that the scale pattern is such that the horizontal spatial information in the code-bit marks suffices to uniquely identify the fiducial bars. A scale pattern that satisfies this requirement is said to be vertically binnable.

Figure 2 shows an example of a vertically binnable scale pattern. The vertical stripes spanning the entire field from top to bottom are the fiducial bars. The stripes that extend part way up from the bottom and part way down from the top are the code-bit marks. The code-bit marks at the top and bottom are identical, so that the image can be binned by the full height (that is, all the rows can be included in the bin for each column, enabling maximum speedup). Other patterns in which code bits at top and bottom differ but identify a greater number of fiducials dramatically increase range, while still greatly speeding up readout. Among the secondary advantages of such a vertically binnable pattern is that the vertical alignment of the CCD relative to the pattern is much less critical than is the alignment needed to utilize the vertical spatial information in a conventional pattern with pixel-by-pixel readout.

This work was done by Douglas B. Leviton of **Goddard Space Flight Center**. *Further information is contained in a TSP (see page 1).*

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, Goddard Space Flight Center, (301) 286-7351. Refer to GSC-14633-1.

Flexible, Carbon-Based Ohmic Contacts for Organic Transistors

These contacts are printed using an inexpensive, low-temperature process.

NASA's Jet Propulsion Laboratory, Pasadena, California

A low-temperature process for fabricating flexible, ohmic contacts for use in organic thin-film transistors (OTFTs) has been developed. Typical drain-source contact materials used previously for OTFTs include (1) vacuum-deposited noble-metal contacts and (2) solution-deposited intrinsically conducting molecular or polymeric contacts. Both of these approaches, however, have serious drawbacks.

Use of vacuum-deposited noble-metal contacts (such as gold or platinum) obviates one of the main benefits of organic electronics, which is low-cost processing based on solution or printing techniques. First, it requires the use of vacuum-deposition techniques (such as sputtering or evaporation) instead of the less expensive solution-based processes such as spin coating, casting, or printing. Second, the use of gold or platinum for coating large-area devices is potentially expensive (both from a standpoint of materials and processing equipment). Again, this approach runs counter to the perceived low-cost benefit of organic electronics. Furthermore, adhesion of gold to many organic materials is very poor. Some recent work has been carried out regarding intrinsically conducting molecular- or polymeric-based contacts such as polyaniline and TTF-TCNQ. Unfortunately, these materials tend to exhibit high resistivities and poor overall performance, are prone to reaction with the surrounding environment, and are potentially unstable with time.

To achieve an ohmic contact to the organic semiconductor, the work function of the contact should be well matched to that of the semiconductor. Due to the similar chemical nature of the graphite filler to the conjugated poly(3-hexylthiophene) (P3HT) polymer, it was surmised that a carbon paste may possess a similar work function and therefore behave as suitable ohmic contact in this application.

To demonstrate the effectiveness of this approach, bottom contact thin-film transistors were fabricated (Fig. 1). A highly doped silicon wafer was used as the substrate, with a thermally grown 300-nm oxide gate dielectric layer. In this case, a 5-mil (127-μm) thick laser-cut stainless-steel stencil was used to pattern the contacts.

The carbon-based conductor used was a paste comprising a stable, flexible polymer binder and a conducting graphite/carbon-based filler. The

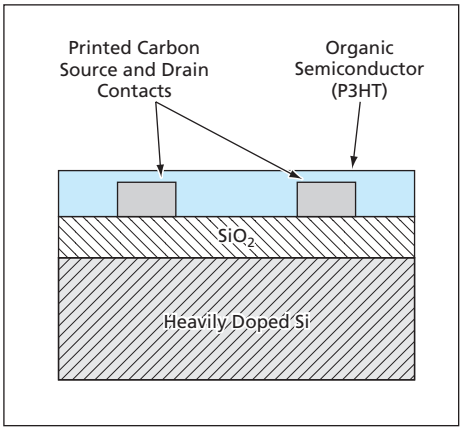

Figure 1. An **Organic Field-Effect Transistor** was fabricated in an inexpensive process, mostly at room temperature, with brief heating at 100 °C.

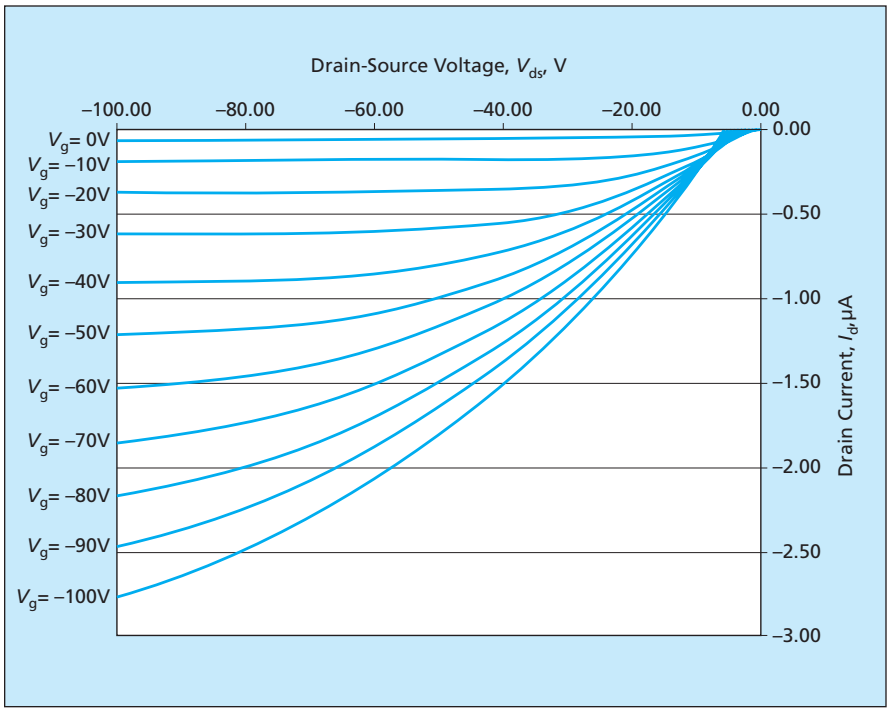

Figure 2. These **Current-Versus-Voltage Curves**, obtained from measurements on a device like that of Figure 1, are characteristic of a field-effect transistor.

paste was stencil-printed through the apertures using a metal squeegee, and the contacts were cured at 100 °C on a hot plate for 30 minutes. The P3HT material was then drop cast on the surface of the substrate, over the printed contacts. Contact was made to the cleaved wafer to form the gate. Contact was made to the drain and source carbon contacts through probes connected to micromanipulators. Device measurements were conducted on an HP 4145B semiconductor parameter analyzer, with the drain-source voltage varying from 0 to –100 V, and the gate bias varying from 0 to –100 V in –10 V steps.

As seen in Fig. 2, very good transistor curves are obtained from the devices, indicating clear field-effect phenomena, which demonstrates the effectiveness of the carbon-based contacts. In this case, a device with a channel length of 500 μm and a channel width of 5,000 μm was measured (multiple devices were characterized to verify repeatability of the data). Other device geometries are possible, as printed feature sizes down to 37 μm have been demonstrated using state-of-the-art thick-film stencil/screen printing techniques.

Enhancement of the drain-source current is clearly seen as a function of increasing gate bias in Fig. 2. In this case, an I_{on}/I_{off} ratio of 44 was determined at V_{ds} = –100 V, with V_g = 0 (I_{off}) and V_g = –100 V (I_{on}). A carrier mobility of $\mu \approx 0.007$ cm^2/V-s was also estimated from the data.

This work was done by Erik Brandon of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-40168, volume and number of this NASA Tech Briefs *issue, and the page number.*

GaAs QWIP Array Containing More Than a Million Pixels

GaAs offers advantages over InSb and HgCdTe.

Goddard Space Flight Center, Greenbelt, Maryland

A 1,024 × 1,024-pixel array of quantum-well infrared photodetectors (QWIPs) has been built on a 1.8 × 1.8-cm GaAs chip. In tests, the array was found to perform well in detecting images at wavelengths from 8 to 9 μm in operation at temperatures between 60 and 70 K. The largest-format QWIP prior array that performed successfully in tests contained 512 × 640 pixels.

There is continuing development effort directed toward satisfying actual and anticipated demands to increase numbers of pixels and pixel sizes in order to increase the imaging resolution of infrared photodetector arrays. A 1,024 × 1,024-pixel and even larger formats have been achieved in the InSb and HgCdTe material systems, but photodetector arrays in these material systems are very expensive and manufactured by fewer than half a dozen large companies. In contrast, GaAs-photodetector-array technology is very mature, and photodetectors in the GaAs material system can be readily manufactured by a wide range of industrial technologists, by universities, and government laboratories.

There is much similarity between processing in the GaAs industry and processing in the pervasive silicon industry. With respect to yield and cost, the performance of GaAs technology substantially exceeds that of InSb and HgCdTe technologies. In addition, GaAs detectors can be designed to respond to any portion of the wavelength range from 3 to about 16 μm — a feature that is very desirable for infrared imaging. GaAs QWIP arrays, like the present one, have potential for use as imaging sensors in infrared measuring instruments, infrared medical imaging systems, and infrared cameras.

This work was performed by Murzy Jhabvala of **Goddard Space Flight Center** *and K. K. Choi of the U. S. Army Research Lab and Sarath Gunapala of NASA's Jet Propulsion Laboratory. For further information, contact the Goddard Innovative Partnerships Office at (301) 286-5810. GSC-14688-1*