Multiple Embedded Processors for Fault-Tolerant Computing

Outputs of processors would be compared to detect and correct bit errors.

NASA's Jet Propulsion Laboratory, Pasadena, California

A fault-tolerant computer architecture has been conceived in an effort to reduce vulnerability to single-event upsets (spurious bit flips caused by impingement of energetic ionizing particles or photons). As in some prior fault-tolerant architectures, the redundancy needed for fault tolerance is obtained by use of multiple processors in one computer. Unlike prior architectures, the multiple processors are embedded in a single field-programmable gate array (FPGA). What makes this new approach practical is the recent commercial availability of FPGAs that are capable of having multiple embedded processors.

A working prototype (see figure) consists of two embedded IBM PowerPC®405 processor cores and a comparator built on a Xilinx Virtex-II Pro FPGA. This relatively simple instantiation of the architecture implements an error-detection scheme. A planned future version, incorporating four processors and two comparators, would correct some errors in addition to detecting them.

This work was done by Gary Bolotin, Robert Watson, Sunant Katanyoutanant, Gary Burke, and Mandy Wang of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-40575



Faults Are Detected in this prototype system by comparison of the outputs of the two processors, which are embedded in a single FPGA. The legend "FI" denotes locations where faults are inserted for testing purpose.

🗢 Hybrid Power Management

Ultracapacitors offer numerous advantages over rechargeable batteries.

John H. Glenn Research Center, Cleveland, Ohio

An engineering discipline denoted as hybrid power management (HPM) has emerged from continuing efforts to increase energy efficiency and reliability of hybrid power systems. HPM is oriented toward integration of diverse electric energy-generating, energy-storing, and energy-consuming devices in optimal configurations for both terrestrial and outer-space applications. The basic concepts of HPM are potentially applicable at power levels ranging from nanowatts to megawatts. Potential applications include terrestrial power-generation, terrestrial transportation, biotechnology, and outer-space power systems.

Instances of this discipline at prior stages of development were reported (though not explicitly labeled as HPM) in three prior *NASA Tech Briefs* articles: "Ultracapacitors Store Energy in a Hybrid Electric Vehicle" (LEW-16876), Vol. 24, No. 4 (April 2000), page 63; "Photovoltaic Power Station With Ultracapacitors for Storage" (LEW-17177), Vol. 27, No. 8 (August 2003), page 38; and "Flasher Powered by Photovoltaic Cells and Ultracapacitors" (LEW-17246), Vol. 24, No. 10 (October 2003), page 37. As the titles of the cited articles indicate, the use of ultracapacitors as energy-storage devices lies at the heart of HPM. An ultracapacitor is an electrochemical energystorage device, but unlike in a conven-